Propagation Delay Analysis of a Soft Open Defect inside a TSV

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Abstract
The propagation delay of a logic signal through a through silicon via (TSV) in a 3D IC may depend on a soft open defect inside it. The propagation delay of a defective TSV which is connected only with barrier metal, in part owing to a soft open defect, is analyzed with an electromagnetic simulator and a circuit one in this paper. The results reveal that if such a soft open defect occurs inside a TSV, the delay depends on the defect size and the IC may work without any errors. A soft open defect will change into a hard open one in operation of a 3D IC and may generate a logical error. In order to realize high reliability of the IC, the defect should be detected before it changes into a hard open defect. In this paper, test input vectors are proposed with which a soft open defect can be detected by delay testing. However, the simulation results suggest that when the input and output capacitance of a TSV is small, the defect may not be detected even if the test vectors are provided to the defective IC, since the propagation delay of the defective TSV can be smaller than a defect-free one.

Keywords: TSV, Soft Open, Propagation Delay, Electromagnetic Simulation, Fault Analysis, 3D IC, Delay Testing, Test Input Vector

1. Introduction
3D IC technology will realize size reduction, performance increase, and low power consumption in portable electronics. Thus, much attention has been paid to 3D IC fabrication.[1, 2]

TSVs are key elements for realizing 3D ICs. There are various fabrication methods for 3D ICs based on TSVs.[1, 3] Short defects and open ones can occur independently of the fabrication methods, since there are many TSVs inside a 3D IC.[3, 4]

Short defects will generate logical errors by providing complement logic values to the defective TSVs. On the other hand, it is not apparent what faulty effects are caused by an open defect in a TSV. Generally, open defects are more difficult to detect than short ones. Thus, only open defects in TSVs are targeted in this paper.

Open defects can be classified into hard open defects and soft ones. In a hard open defect, a TSV is divided into two completely separate parts which are not connected to each other. In a soft open defect, the parts are partially connected electrically to each other. A soft open defect may also be called a weak open defect.[3] The defect may be caused by a void or a crack in the TSV.[5] Since a soft open defect may affect the reliability of the IC, a guideline for preventing a crack in a TSV is proposed.[6] Also, since such defects may occur in a TSV, a redundant design for TSVs[7] and a self-repair method[8] have been proposed.

Defects that occur in TSVs are different from ones in SoCs. Furthermore, they often may occur and generate logical or timing errors. Thus, testing for TSVs is challenging[3, 5, 9] They can be classified into 2 types: pre-bond testing and post-bond testing.

Open defects that generate logical errors will be detectable by boundary scan techniques. Since there are a lot of TSVs in a 3D IC, various Design for Testability (DfT) methods and built-in test(BIST) methods have been proposed in order to test it quickly.[10–14]

Soft open defects that generate timing errors may not be detected by boundary scan techniques, but they may be detected by an electrical test method. Thus, various electrical test methods have been proposed. A test method proposed in[15] is based on the principle of oscillation tests in analog circuits. An electrical test method with an on-chip sense amplifier has also been proposed.[16]

In order to realize a high yield of 3D ICs, defective TSVs should be located. Thus, a test method has been proposed...
based on X-ray computed tomography. It takes a long time to judge whether a soft open defect occurs in a TSV by this test method. Since there are many TSVs in a 3D IC, we should develop a test method with which a defective TSV can be located quickly.

Soft open defects will reduce the reliability of an IC. It will result in some increase of propagation delay time. It will grow and can change into a hard open defect. Since a hard open defect may generate logical errors as well as timing errors, a soft open defect should be detected before it becomes a hard one.

However, it has not been apparent how long of a propagation delay time is caused by a soft open defect in a TSV. The propagation delay time of a defect-free TSV has been examined with an analytical model. It is difficult to derive the delay time using this approach owing to complexity of the analytical model derivation. On the other hand, more detailed parasitic effects may be derived and a more accurate delay time can be obtained by electromagnetic simulation, compared with the methodology based on purely circuit analysis. Thus, the delay time of a defect-free TSV has been examined by electromagnetic simulation. However, faulty effects on propagation delay time caused by a soft open defect in a TSV have not been examined by electromagnetic simulation.

We examined the faulty effects caused by a soft open defect inside a TSV by electromagnetic simulation. A TSV is made of a main and a barrier metal. It seems that soft open defects occurring in a TSV depend on the configuration, process parameters used, and so on. Now, the TSV fabrication process continues to be revised and is not fixed. It is impossible to specify what size and what configuration of soft open defect occurs inside a TSV. Thus, as a first step of fault analysis for soft open defects inside TSVs, we examined the faulty effects of a defective TSV that is connected only with a barrier metal owing to a soft open defect. In Section 2, we denote our targeted layout of TSVs. In Section 3, we describe our fault analysis method and the results.

2. Layout of Targeted TSVs

An example of a 3D IC is shown in Fig. 1. In such an IC, some dies are connected to each other by TSVs as shown in Fig. 1(a). As shown in Fig. 1(b), they are connected by many TSVs.

TSVs are close together. When a soft open defect occurs inside a TSV, the signal at the defective TSV may be changed by the logic signals of the neighboring ones, as in the case of a hard open defect in a TSV. Thus, we analyzed the layout shown in Fig. 2(a) so as to examine faulty effects caused by a soft open defect in a TSV that is adjacent to another TSV.

We inserted a soft open defect into TSV5. Generally, TSVs are made of a main metal of Cu and a surrounding barrier metal of Ta. A soft open defect is caused by a void and a crack in a TSV. We selected a soft open defect

![Fig. 1 3D IC with TSVs.](image1)

![Fig. 2 Targeted layout.](image2)
with which a TSV is connected together with a fine wire made only from barrier metal as a targeted defect.

Examples of defective TSVs are shown in Fig. 3. The cross section of the soft open defects is not rectangular. However, it can be simplified as a rectangular parallelepiped. Thus, as shown in Fig. 2(b), we assume that the cross-section of the fine wire is a square, whose edge length is $d_w$. Also, we assume that the length of the wire is $d_h$.

Targeted open defects are specified by means of $d_w$ and $d_h$. In the open defect shown in Fig. 3(b), $d_{h2}$ and $d_{w2}$ are greater than $d_{h1}$ and $d_{w1}$ in our open defect model, respectively, since the size of open defect #1 is bigger than open defect #2. We examined the faulty effects on output voltage of TSV5 shown in Fig. 2(b).

The sizes of our targeted TSVs in Fig. 2 are shown in Table 1. These are the minimum permissible sizes that are satisfied by the design rule of the fabrication process of a 3D IC.[1] whose VDD is 1.0 V.

<table>
<thead>
<tr>
<th>parameter</th>
<th>value [$\mu$m]</th>
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<tbody>
<tr>
<td>H1</td>
<td>7.34</td>
</tr>
<tr>
<td>H2</td>
<td>5.34</td>
</tr>
<tr>
<td>S</td>
<td>1.75</td>
</tr>
<tr>
<td>W</td>
<td>1.75</td>
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### 3. Fault Analysis for TSV Having Soft Open Defect

TSVs are used for making connections between dies. We selected dies fabricated with a 90 nm CMOS process as our targeted dies. A TSV is driven by a logic gate and the logic signal through the TSV is outputted to a logic gate. Thus, we examined the faulty effects caused by a soft open defect inside a TSV with an inverter gate connected to the input and output ports of each TSV.

In our fault analysis, we extracted the S-parameters of the layout shown in Fig. 2(a) with a 3-dimensional electromagnetic simulator “EMpro” produced by Agilent Technologies. We examined the faulty effects of a soft open defect inside the TSV by means of the S-parameters with a circuit simulator. The simulation circuit is shown in Fig. 4.

We added the Spice model of an inverter gate designed with a 90 nm CMOS process to the S-parameters and simulated the circuit shown in Fig. 4 with the circuit simulator “ADS” produced by Agilent Technologies. Furthermore, the capacitors $C_L$ and $C_i$ were added to the simulation circuit as shown in Fig. 4. $C_L$ and $C_i$ are the load capacitance and input capacitance of the inverter gates, respectively.

TSVs are modeled as lines of 50 $\Omega$ impedance in our S-parameter extraction. We derive the propagation delay from the waveform of TSV5 out that is obtained from the circuit in Fig. 4. Thus, impedance mismatching exists between the TSVs and inverter gates. This means that there can be some errors in our derived propagation delays. However, since the length of the TSVs, $H_t$, is extremely small, we think that the errors are small. Thus, we derived the propagation delays of the circuit shown in Fig. 4.

It seems that faulty effects will depend on the logic signals of neighboring TSVs. Thus, we inserted a soft open defect to TSV5 that was in the center of our targeted TSVs and discussed the faulty effects that appeared in the voltage of TSV5 out depicted in Fig. 4.

An FEM method is used in our S-parameter extraction. The frequency range is from 0.01 GHz to 50 GHz. The mesh precision is 0.001. The number of adaptive mesh refinements is from 5 to 50. The percentage of each of the refinement is 25%.

The simulation results for a soft open defect of $d_w = 1$ nm shown in Fig. 6 are derived by the input signals shown in Fig. 5(a). The rising time and falling time of the input signals in this paper are 0.1nsec. The amplitude of each input signal is 1 V, since the targeted layout is for a fabrication process of $V_{DD} = 1.0$ V. We assume that the logic threshold voltage is 0.5 V. A waveform of TSV5 out in the defect-free...
A signal from L to H is provided to TSV5 at 1.0 nsec. As shown in Fig. 6, when a soft open defect occurs at TSV5, a small delay will appear in TSV5out. Also, when $d_h$ is greater than 250 nm, the propagation delay becomes larger than for the defect-free circuit. Thus, the defect may be detected by delay testing.

On the other hand, when $d_h$ is smaller than 10 nm, the delay is smaller than in the defect-free case. This means that the defect can generate no faulty effects and the circuit will work as expected. Also, the delay caused by the change from L to H is almost the same as the one from H to L.

Our targeted defective TSV can be modeled as the simple circuit shown in Fig. 7. In Fig. 7, a resistor $R_b$ is made of a barrier metal whose resistance can be estimated by Eq. (1).

$$R_b = \frac{\rho}{\text{uni}} \frac{d_h}{(w^2 + d_w^2)}$$  \hfill (1)

where $\rho$ is the resistivity of the barrier metal. Capacitor $C_p$ is a parasitic capacitor whose capacitance can be estimated by Eq. (2).

$$C_p = \frac{\varepsilon \cdot (w^2 + d_w^2)}{d_h}$$  \hfill (2)

where $\varepsilon$ is a dielectric constant of the open defect.

When $d_h$ is large, an electrical signal will be propagated through $R_b$ since $C_p$ is small. On the other hand, when $d_h$ is extremely small, $C_p$ becomes large and the electrical signal will be propagated through $C_p$. Thus, the propagation delay in the defective TSV may become smaller than in the defect-free TSV as shown in Fig. 6.

The simulation results for Tst#2 are shown in Fig. 8. The propagation delay in Fig. 8 is smaller than in Fig. 6. This stems from the parasitic capacitance between the defective TSV and the neighboring ones. However, as shown in Fig. 8, almost the same phenomena can be obtained as in Fig. 6. Thus, in the rest of this paper, we discuss propagation delays only for Tst#1.

In Fig. 6 and 8, the slope of TSV5out is almost the same as the others. That is the reason why $H1$ is small and the resistance of the TSVs is small.

If a soft open defect occurs inside a TSV, logical errors will not occur as shown in Fig. 6. Faulty effects appear only as changes in the propagation delay time. The delay time depends on $d_h$ in Fig. 6. Since it may also depend on $d_w$, we examined the effects caused by this dependence. The results are shown in Fig. 9. $\Delta t_{pd}$ in Fig. 9 is defined by Eq. (3).
\[ \Delta t_{pd} = t_{pd} - t_{pdn} \quad (3) \]

where \( t_{pd} \) and \( t_{pdn} \) are the propagation delays of the circuit under test and the defect-free circuit, respectively.

As shown in Fig. 9, when \( d_h \) is small, it becomes negative. This means that the signal of TSV5\text{in} can be propagated to TSV5\text{out} more quickly than in the defect-free TSV and the soft open defect will not be detected by measuring the propagation delay time. On the other hand, when \( d_h \) is large, \( \Delta t_{pd} \) becomes large. That is the reason \( R_b \) and the propagation delay time become large as \( d_h \) becomes large. These characteristics do not depend on \( d_w \) but on \( d_h \) as shown in Fig. 9.

Such a soft open defect may be detected by measuring the propagation delay time. In order to detect the open defect, test input vectors which increase the propagation delay time, should be provided to the TSVs.

We examined the dependability of the logic signals of neighboring TSVs on the propagation delay time of TSV5 in order to derive input signals by which soft defects can be detected more easily. The waveforms of TSV\text{out}5 that are obtained by providing a Low signal to the TSVs other than TSV5 are shown in Fig. 10. For \( d_h = 1000 \) nm in Tst\#1 and this input signal, the values for \( \Delta t_{pd} \) are 3.2 psec and 2.2 psec, respectively. Since the propagation delay generated by the input signal is smaller than Tst\#1, a logic signal change whose direction is opposite to the logical change in TSV5\text{in} should be provided to TSVs other than the defective one in order for the delay to become large.

Figure 11 shows the waveforms of TSV\text{out}5 when a signal from H to L is provided to TSV10. As shown in Fig. 11, this signal generates TSV\text{out}5 waveforms that are almost the same as the ones obtained by providing L to TSVs other than TSV5. This means that the effect caused by the signal change is shielded by TSV4 and is not propagated to
Waveforms of TSV5out that are obtained by providing such a signal to TSV4 are shown in Fig. 12. As shown in Fig. 12, a larger propagation delay can be generated by the signal of TSV4 than by the signal of TSV7. Thus, a signal change whose direction is opposite to that of TSV5in should be provided to the TSVs neighboring TSV5.

Waveforms obtained by providing a logical change to TSV4 and TSV6 simultaneously are shown in Fig. 13. As shown in Fig. 13, a larger propagation delay appears than when providing a logical change only to TSV4. This means that the propagation delay can be made large by providing a logical change to as many TSVs as possible that are neighboring to TSV5. Therefore, it is concluded that Tst#1 is the test input vector with which the propagation delay can be made largest.

Generally, $C_i$ and $C_L$ are connected to each TSV. Thus, we examined the effects caused by the capacitance. Waveforms of TSV5out generated by providing Tst#1 to the TSVs are shown in Fig. 14. Comparing the waveforms to the ones shown in Fig. 6 shows that larger propagation delays appear when $C_i = C_L = 50 \, \text{fF}$ than when $C_i = C_L = 0 \, \text{fF}$.

Since the characteristics may depend on the capacitance and $d_w$, we examined their effects. The results are shown in Fig. 15. As shown, as the capacitance becomes large, the propagation delay will become large and the soft open
defect will be detected more easily. Also, as $d_w$ becomes large, the delay will become small, since $R_b$ becomes small. Thus, the soft open defect whose $d_w$ is large may not be detected by delay testing. We think that electrical testing is necessary to detect such a defect before it changes into a hard open defect.

The waveforms obtained with our simulation have not been compared to experimental results obtained with real ICs in which the soft open defects shown in Fig. 2 are inserted. There may be some differences between them, since defective TSVs are modeled only with S-parameters and there may be some effects caused by impedance mismatches between the S-parameter model and the added inverter gates. However, it can be estimated from the principle and from our simulation results that soft open defects generate only small propagation delays. Thus, a defective 3D IC in which soft open defects occur at TSVs may work as expected. This suggests to us that a more powerful test method should be developed so that defects generating small delays can be detected in order for them to be detected before they generate logical errors.

4. Conclusion

In this paper, a soft open defect inside a TSV was created by establishing a connection within the TSV using a fine wire made from only barrier metal. This defect was then targeted for study. Faulty effects caused by the defect were examined with a 3D electromagnetic simulator and a circuit simulator. The simulation results show that the propagation delay at the defective TSV may depend on the size of the defect and the defective IC may work as expected, since the delay is small. Also, we propose test input vectors which allow the soft open defect to be detected by delay testing. Furthermore, we reveal the possibility that when the input and output capacitances of a TSV are small, a soft open defect can not be detected even if the test input vectors are provided to the IC, since the propagation delay of a defective IC can be smaller than the defect-free IC.

Faulty effects caused by a soft open defect of only one type were examined in this paper. Many types of open defects can occur inside a TSV. Fault analysis should be performed for the defects. Also, we examined the faulty effects only by simulation. They should be examined with real ICs, in which soft open defects occur at TSVs. Furthermore, powerful test methods should be developed for detecting soft open defects in TSVs in order to realize high reliability of 3D ICs. These problems remain for future work.

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