[Technical Paper]

An Electrode Structure for Ferroelectric Thin Films and Its Application to the Nanotransfer Method

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Abstract

One method of miniaturizing electric boards is to reduce the capacitor area on the board. We fabricated a thin film capacitor on a Si wafer, released the capacitor from the wafer, and transferred the released capacitor onto a board. BaTiO₃ (BTO) was chosen as the dielectric material, and a capacitor was fabricated using metal-organic decomposition (MOD) onto a Si wafer with Ti and Pt as the bottom electrode. Measured electric properties included the dielectric constant, at about 640, as the I-V property, and hysteresis. When a BaTiO₃ film was deposited onto the substrate, which had only a Pt electrode (no Ti used for bonding layer) to release from the substrate after deposition, the electrode broke because of internal stress. The stress was measured quantitatively and a new electrode structure was designed to overcome the problem. ECR etching proved adequate for making the electrode structure.

Keywords: Capacitor, Embedded Substrate, BaTiO₃, Thin Film, Nanotransfer Method, Metal-organic Decomposition

1. Introduction

Recently, manufacturers have been competing to miniaturize even further the miniature electronics and components used in such devices as mobile phones. One of the methods used to miniaturize the board is to reduce the capacitor area on the board. To achieve this, a technique called the nanotransfer method is used, in which a capacitor is manufactured on a Si wafer, released from the substrate, and transferred to the board. In preceding studies, PZT has been used as a dielectric,[1] but there are environmental concerns with PZT. Awareness about environmental problems is increasing throughout the world, and switching to non-lead dielectric materials is necessary. As such, this paper reports on a capacitor using BaTiO₃ (BTO) that was manufactured on a Si wafer. BTO is a well-known non-lead dielectric, and has a crystal structure similar to PZT. However, using BTO film deposition with the MOD method as a film capacitor has a difficulty because of cracking in the BTO film.

First of all, we investigated the properties of a BTO

capacitor and whether BTO films deposited by the MOD method could be used for the dielectric in the capacitor. For this purpose, a capacitor was manufactured onto a non-releasable Si substrate.

It appears that the internal stress in BTO films deposited by the MOD method is larger than in PZT films. Because of this large stress, after the BTO film deposition onto the releasable chip, the bottom electrode is damaged. Therefore it is necessary to take measures not to damage this electrode.

A new electrode structure is proposed and the BTO film is deposited onto the releasable chip with the new electrode.

2. Capacitor Property with BTO Dielectric

2.1 Experimental procedure

First, a Si wafer was placed into a furnace and a 300 nm layer of SiO₂ was formed. Then, Ti was sputtered onto the wafer to a thickness of 5 nm, followed by Pt to a thickness of 50 nm. These became the bottom electrode, with Ti act-

ing as an adhesion layer between the Pt and SiO₂.

After sputtering, the wafer with the electrode was cut to a 20 mm chip. The cut chip was cleaned by ultrasonic cleaning using pure water, then acetone, followed by rinsing with 2-propanol.

After this cleaning, a BTO solution was deposited onto the chip using the MOD method to form the dielectric layer. First, the BTO solution was dispensed onto the substrate and spun at 2500 rpm for 20 s with a spin coater. After the deposition of the solution, the chip was annealed with rapid thermal annealing (RTA) and crystallized at 120 °C for 2 minutes, 250°C for 5 minutes and 700°C for 2 minutes. The film formation process, which consisted of solution deposition and annealing was repeated 15 times to form the BTO dielectric films.

While forming the dielectric film, we examined the growth of the crystal lattice with X-ray diffraction (XRD). After the dielectric film was fabricated, Pt with a diameter of 2 mm was sputtered as the upper electrode. A part of the dielectric film was dissolved with buffered HF, and bottom electrode cropped out for electric measurement. The I-V characteristic, capacitance, and hysteresis property were measured. In addition, the dielectric film thickness was measured with a surface roughness meter (Dektak 3).

2.2 Experimental result

The result of XRD is shown in Fig. 1.

Each peak grows with repeated deposition. These peaks show the perovskite structure except for the largest peak. The largest one, at around 40°, is the Pt peak as the bottom electrode. It can be said that the perovskite structure formed smoothly. However the peaks seem to be oriented randomly.

The I-V characteristics using the two-terminal method are shown in Fig. 2. The horizontal axis is the electric field, and the vertical axis is the current density from the size of the upper electrode. When the electric field grew large, the current density changed in the range of 10⁻⁷ A/ cm² or more.

The capacitance was measured at about 15 nF using an LCR meter. The film thickness measured using the roughness meter was 1.2 μm. From these measurements, it appeared that the BTO film thickness per deposition was 80 nm (i.e., 1.2 μm after 15 depositions). In addition, the dielectric constant was about 640 considering the area of the upper electrode (2 mm in diameter), the provided film thickness, and the capacitance.

As for the hysteresis, the remnant polarization was 3 μC/cm² and the coercive field was 37 kV/cm. The shape

Fig. 1 X-ray diffraction of BaTiO₃.

Fig. 2 I-V characteristics of BaTiO₃.

Fig. 3 Ferroelectric Hysteresis of BaTiO₃.

of the hysteresis loop is shown in Fig. 3.

3. BTO Deposition onto Releasable Wafer

3.1 Phenomena after deposition

Next, BTO was deposited onto a releasable wafer, a wafer that did not contain Ti between the SiO₂ and Pt. For this sample, four kinds of bottom electrode thickness were prepared: 100, 150, 500 and 1000 nm. However, after the film formation process the bottom electrode was broken. There are two ways to break the electrode. One is that the electrode floats and is isolated from the substrate when the BTO solution is dispensed. This phenomenon happens when the thickness of the electrode is over 500 nm, which thickness has a weak adhesion strength between Pt and

SiO₂. [1] This occurs because the solution gets between the Pt and SiO₂ from the edge of the chip. After placing the BTO solution on the chip and the electrode floating, we can see the interference fringes of the solution on the SiO₂.

The other way to break the electrode is that parts of the electrode peel away from the substrate. This phenomenon happens when the thickness of the electrode is between 100 and 150 nm, as illustrated in Fig. 4. [2]

This peeling occurs mainly because of internal stress. However, with PZT deposition on a wafer of the same electrode structure, this phenomenon does not occur. Thus, the internal stresses of PZT and BTO were measured and compared.

3.2 The measurement of internal stress

To measure the internal stress, the Stoney equation was used.

$$\sigma = \frac{E_s t_s^2}{6(1 - \nu_s) R t_f}$$

where σ is the stress, E_s is the Young's modulus of the substrate, ν_s is the Poisson's ratio of the substrate, t_s is the thickness of the substrate, t_f is the thickness of the film and R is the radius of curvature of the initial flat substrate after deposition of the film. The substrate is silicon.

We prepared two samples which had the non-releasable electrode and deposited one layer of the BTO and PZT film on each. We measured the curvature with a laser to obtain the stress measurement. The result of the stress measurement is shown in Fig. 5. The horizontal axis is the scanning distance on a 4-inch wafer, and the vertical axis is the calculated internal stress.

We found that the PZT stress was about 1000 MPa and

Fig. 4 Peeling of the electrode.

Fig. 5 Stress of the prepared films.

the BTO stress was 3000 MPa. The BTO had three times the stress of the PZT.

3.3 Electrode structure

Taking into consideration the result of the stress measurement and the two ways the electrode could break, we designed the electrode structure on the releasable wafer as shown in Fig. 6. All the thicknesses are uniform with Ti at 5 nm and Pt at 1000 nm. There are two key points in the design of the electrode structure. One point is to prepare the non-release part using Ti sputtering around the edge which increases the adhesion between the SiO₂ and Pt and prevents the solution from invading. The other point is to increase the Pt thickness to 1000 nm, as shown in Fig. 6. This improves the breaking strength and prevents the electrode from peeling off as in Fig. 4.

To fabricate this structure so that there would be no Ti at the center of the substrate, two methods were used, lift-off and electron cyclotron resonance (ECR) etching. In addition, the width of the Ti was changed as a parameter. Whether the SiO₂ surface should be cleaned or not before Ti sputtering was also investigated. The cleaning method was O₂ reactive ion etching (RIE).

3.4 Result

The results are shown in Table 1. Case 1 is the same as the sample in 3.1 with 1000 nm. In Case 2, the liftoff process was used to make the electrode structure. However after BTO deposition, this electrode was broken. We think the cause is that during patterning and removing the resist before lift off, some material remained on Ti. This remained material interfered with bonding between Ti and Pt.

In Case 3 and Case 4, the BTO films could be deposited to 17 layers without breaking the electrode. The thick-

Fig. 6 Electrode structure of the prepared films.

Table 1

Case	1	2	3	4
Width of Ti (mm)	0 (no Ti)	2	3	3
Ratio of area	0%	36%	50%	50%
Wafer cleaning	no	no	no	O ₂ RIE
Electrode fabrication process	Simple sputtering	Lift off	ECR	ECR
Result	Release	Release	No release	No release

nesses of the dielectric layers were measured and were about 1 μm each.

4. Conclusion

A capacitor with a BTO dielectric formed by the MOD method was fabricated on a non-releasable substrate and its properties were measured. The dielectric constant was about 640 and XRD, I-V, and hysteresis properties were also measured. The condition of MOD method for BTO in this paper is from the condition for PZT[1]. It is necessary to optimize the condition for BTO which will improve the properties significantly.

With the BTO film, the internal stress was so large that

if the BTO was simply deposited onto the releasable substrate, the electrode would be broken. Therefore, the BTO stress was measured and compared with the PZT stress. A new electrode structure, which has no Ti at the center area, was designed. To make the electrode structure, ECR etching was the best method at this time.

The advantage of this new structure is that all the dielectric materials can be applied.[3] There should be no problems even if a high stress material like BTO needs to be used.

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