**FEM Analysis on Mechanical Stress of 2.5D Package Interposers**

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**Abstract**

As data transmission rate increases, flip chip plastic ball grid array (FCPBGA) utilizing an interposer for multiple chips is gaining prominence because of high performance. The authors assessed interposer configurations with a set of chip and package assumptions and obtained key parameters for mechanical analysis. The authors studied warpage of interposer, first principal stress in the dielectric layer under the controlled collapse chip connection (C4) bump pad, and von Mises stress at the solder joint between interposer and organic substrate with Si, glass, and organic interposers. The analysis results indicate that the stress under the C4 bump is very low with Si or glass interposer compared to conventional FCPBGA. Also, the results indicate that glass interposer with coefficient of thermal expansion (CTE) of 6 ppm/°C has approximately 30% lower stress than Si interposer at the solder joint between the interposer and the organic substrate.

**Keywords:** Interposer, Flip Chip, PBGA, Low-k Dielectric, FEM

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1. **Introduction**

Higher integration of functionality of the semiconductor device is getting more important to fully utilize high performance of advanced semiconductor technology. One approach is integration on one chip which is called system-on-chip (SoC). SoC has a challenge of manufacturing yield due to large chip size when a substantial amount of memory is integrated on die. SoC also requires a longer and more complex fab processing to include the specific features required for memory integration. Another approach of integration is 3D chip stack using through-silicon-vias (TSV). Typical configuration of 3D package is multiple memory chips, a logic chip and an organic substrate stacked from the top. Wiring to the top memory chip comes from substrate via micro joints and TSV of both logic and memory chips.[1, 2] One of the challenges of 3D chip stack is exactly matched TSV layout between logic and memory chips that requires concurrent physical layout design of electrode terminals. Recently JEDEC published a standard of micro bump layout for wide I/O memory to address the above issue.[3, 4]

As TSV technology evolves, an intermediate configuration between SoC and 3D package has emerged, which is called 2.5D package. 2.5D package utilizes Si interposer with TSV and wiring layers built by re-distribution layer (RDL) technique, and multiple chips are mounted side by side on the interposer.[1, 2, 5–9] There are several advantages of 2.5D package against SoC or 3D package as follows:

- Ease of use of conventional separate chips from chip design point of view.
- Efficiency of active area on each chip because of no keep out area for TSV.
- Efficiency of wiring layers on each chip as the global wiring is built on the Si interposer.
- Efficiency of heat dissipation using thermal lid as compared to 3D stack.

Si has been most widely evaluated as an interposer material, but alternative materials such as glass[10–12] or organic are also proposed for interposer. The authors studied feasible package configuration based on currently applicable design rule for conventional multi-chip-module (MCM) FCPBGA and interposer FCPBGA with three different interposer materials of Si, glass, and organic assuming a logic chip and a memory chip mounted on the interposer. We investigated thermo-mechanical behavior of the micro joints at chip-to-interposer and interposer-to-substrate, and thermo-mechanical stress at the dielectric layer under the C4 bump pad of the chip by finite element method (FEM) modeling.

2. **Design Assessment**

2.1 **Basic assumptions**

We set basic assumptions of logic chip, memory chip,
I/O counts and package size as shown in Table 1. We refer to JEDEC standard MO-305A[4] for micropillar grid array (MPGA) memory chip, and we set simple numbers of I/O count for this design assessment. Custom memory with 200 μm pitch is also assumed for organic interposer and organic substrate as MPGA bump pitch is too tight for organic carrier. Table 1 summarizes the features we use in this study.

The images of bump layout for logic chip and MPGA memory chip are shown in Fig. 1. The MPGA memory chip uses a centralized layout, and there are four bump layout blocks in the center.

Table 1 Features of chip and package.

<table>
<thead>
<tr>
<th>Feature</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip size (logic)</td>
<td>15 mm × 15 mm</td>
</tr>
<tr>
<td>Chip size (memory)</td>
<td>10 mm × 7 mm</td>
</tr>
<tr>
<td>Chip thickness (logic and memory)</td>
<td>786 μm</td>
</tr>
<tr>
<td>Bump matrix (logic)</td>
<td>94 × 94</td>
</tr>
<tr>
<td>Bump matrix (MPGA memory)</td>
<td>30 × 30</td>
</tr>
<tr>
<td>Bump matrix (custom memory)</td>
<td>60 × 60</td>
</tr>
<tr>
<td>Signal I/O count (logic)</td>
<td>1,600</td>
</tr>
<tr>
<td>Signal I/O count (memory)</td>
<td>800</td>
</tr>
<tr>
<td>Direct wiring between logic and memory</td>
<td>800</td>
</tr>
<tr>
<td>Bump pitch (logic)</td>
<td>150 μm</td>
</tr>
<tr>
<td>Bump pitch (MPGA memory)</td>
<td>40 μm × 50 μm</td>
</tr>
<tr>
<td>Bump pitch (custom memory)</td>
<td>200 μm</td>
</tr>
<tr>
<td>Package size</td>
<td>42.5 mm × 42.5 mm</td>
</tr>
<tr>
<td>Package BGA pitch</td>
<td>1.0 mm</td>
</tr>
<tr>
<td>Package BGA ball count</td>
<td>1,600</td>
</tr>
<tr>
<td>Thickness of base organic substrate</td>
<td>970 μm</td>
</tr>
<tr>
<td>Thickness of MCM FCPBGA’s substrate</td>
<td>1,267 μm</td>
</tr>
</tbody>
</table>

1) (b) and (c) in Figure 2
2) (a) in Figure 2

2.2 Package configurations

Figure 2 shows package configurations in cross-sectional view. Figure 2 (a) is MCM FCPBGA that uses conventional build-up substrate. The memory chip is assumed to have RDL to convert centralized bump layout to array layout as the escape from centralized bumps to substrate is not feasible with currently available design rules of the build-up substrate. Figure 2 (b) is Si or glass interposer FCPBGA. A logic chip and a memory chip are mounted on an interposer, and the interposer is mounted on an organic substrate. The interposer has a RDL on the top side to have escape wirings from both chips and direct wirings from the logic chip to the memory chip. TSV or through glass vias (TGV) is typically laid out in a square matrix, and micro solder balls to interconnect the interposer to the substrate are placed under the TSV or TGV. Figure 2 (c) is organic interposer FCPBGA. A logic chip and a memory chip with RDL are mounted on an organic interposer, and the interposer is mounted on an organic substrate. The interposer is assumed to be coreless substrate configuration in this study.

2.3 Design ground rules and key package parameters

Table 2 shows the design ground rules of each package configuration used to assess the package key parameters which are the size of interposer and organic substrate, and layer count of build-up substrate and RDL. We set 0.375 mm clearance between logic and memory chips for Si/
glass interposers and 3.0 mm clearance for organic interposer and MCM FCPBGA.

The Si/glass interposer size can be determined by the width of direct wirings between the logic chip and the memory chip (S1 in Fig. 3), the width of wirings from logic to TSV/TGV (S2 in Fig. 3), and the logic chip size. There are four bump layout blocks on the memory chip (Figure 1). Wirings to the memory’s backside bump blocks come from top and bottom side I/O terminals of the logic chip (200 I/Os from top and bottom respectively). Also additional 200 I/Os have to be wired out to TSV or TGV around the direct wirings between the logic and the memory on the top side or the bottom side. Both S1 and S2 come up to approximately 1.6 mm with 4/4 \( \mu \text{m} \) line and space ground rule in RDL. The minimum dimension to place these wirings and the chips is approximately 22 mm. Assuming to use an industry standard solder ball pitch for 1600 micro joints for the interconnection from the interposer to the substrate, 0.65 mm pitch gives the smallest interposer size as 27 mm \times 27 mm with a 40 \times 40 solder ball matrix. The similar assessment derives 33 mm \times 33 mm with 0.8 mm ball pitch for the organic interposer.

Figure 4 shows a typical signal escape of C4 joints. Escaped trace count on one layer can be calculated by the below equation.

\[
\text{EscapedTraceCount} = \frac{P - D - L}{2L}
\]

Total number of build-up layers is defined by required build-up layer count for signal escape on the top side in case of conventional FCPBGA. Total number of build-up layers for coreless is sums of signal escape layers, a power plane layer, a ground plane layer, and BGA pad layer. In case of RDL, minimum layer count (a wiring layer and a TSV/TGV layer) is assumed in this assessment.

Table 3 summarizes the key package parameters we obtained from the design assessment, and they are used for the FEM modeling. 4-2-4 stack-up of the substrate layer indicates four build-up layers are stacked on two-conductive-layer-core at top side and bottom side respectively. 6+1
stack-up of the organic interposer indicates six build-up layers are stacked without core. '+1' denotes one additional conductive layer is formed as pad transfer layer, which is the typical structure of coreless substrate.

3. FEM Modeling and Analysis

We analyzed two phases in the process flow - (1) After flip chip reflow, before underfill resin apply, (2) After mount of the assembled interposer with chips and underfill resin on the organic substrate. Both were modeled in half of the assembled form. The reference temperature is set at 180°C.

Table 4 shows the material properties we used in the models. We assume four build-up layers without glass fiber and 3 build-up layers with glass fiber for organic interposer in this analysis. The material properties of RDL, build-up layer, build-up layer with glass fiber and core are derived according to the law of mixture. In case of build-up layer, average volumes of build-up material, Cu and solder resist are defined based on typical design assumption, and then elastic modulus, Poisson’s ratio and CTE are calculated using material properties of each component material according to the law of mixture.

3.1 After flip chip reflow

We assume two chips are mounted on a singulated interposer. The models do not contain underfill resin to simulate the state after cooling of flip chip reflow. We analyzed warpage of the assembled interposer using macro model and first principal stress in the dielectric layer under the bump pad in the logic chip using multi scale modeling technique. MCM FCPBGA was also modeled for comparison to the interposer FCPBGAs. Table 5 shows the model matrix we analyzed. Although the TSV/TGV pitch is set as 0.65 mm from the design assessment, we added different via densities which are equivalent to have full matrix of 0.5 mm pitch or 0.8 mm pitch in 27 mm × 27 mm interposer for this analysis.

3.1.1 Warpage of the interposer

Figure 5 shows the contour of Z-direction displacement for model-j. Clearance between the logic chip and the memory chip is 0.375 mm for Si/glass interposers, and the clearance is 3.0 mm for MCM FCPBGA and organic interposer. The point of zero degree of freedom (ZDOF) is fixed along the Z-axis at the center of package as shown in Fig. 5. Note that the distance between corner point A and B is 27 mm for Si/glass interposers, 33 mm for organic interposer or 42.5 mm for MCM FCPBGA.

The location of the highest Z-direction displacement for model-j is corner point B as shown in Fig. 5. Figure 6 and 7 show...
show Z-direction displacement at top left corner point A and top right corner point B respectively. Highest Z-direction displacement of each Si or glass interposer appears at top right corner. The shape of warpage of Si/glass interposers is concave. This is due to the mismatch of CTE between interposer and RDL. There is larger area where chip is not mounted on the right area compared to the left area as small memory chip is mounted on the right area. The chip mounted area reduces Z-direction displacement because of the sandwiched structure of low CTE Si/high CTE RDL/low CTE interposer, but the area where chip is not mounted has higher Z-direction displacement. This is why the peak of Z-direction displacement appears at the top right corner with Si/glass interposers. In case of MCM FCPBGA, Z-direction displacement is negative, and the warpage is convex. The organic interposer has more complicated warpage behavior. Z-direction displacement at point A is negative with high value, but displacement at point B is positive with high value. This is possibly a result of low elastic modulus of organic interposer.

There is no significant change by equivalent via pitches. The change of via area among the three conditions is less than 1% on the whole interposer area in the assumptions. It is reasonable to have very small effect by equivalent via pitch in this analysis.

Z-direction displacements obtained here are all above 100 μm. This would cause defects such as non-wet soldering and bridged soldering at mount of the assembled interposer especially when the pitch of micro solder joint becomes less than 0.5 mm. Design optimization to reduce interposer size, material selection and process technique to flatten assembled interposer are important to establish stable mount process of interposer mounting.

### 3.1.2 Stress in low-k dielectric layer under the C4 bump pad

Figure 8 shows a micro model of a flip chip joint and dielectric layers under the C4 bump pad. The dielectric layers consist of SiO₂ layer and low-k dielectric layer. First principal stress in the low-k dielectric layer was calculated using multiscale modeling technique by giving strain conditions taken from a macro model to a micro model.

Figure 9 shows a contour of first principal stress in the low-k dielectric layer under the bump point C, which is indicated in Fig. 5. Contour of model-a (MCM FCPBGA) has the highest first principal stress (tensile stress) in the farthest area from ZDOF under the bump. The stresses of model-c (Si interposer) and model-i (glass interposer) are much lower than model-a as shown in Fig. 10. Stresses of Si interposer are the lowest. Stresses of glass-A interposer

![Fig. 6 Z-direction displacement at point A after flip chip reflow.](image)

![Fig. 7 Z-direction displacement at point B after flip chip reflow.](image)

![Fig. 8 Micro model of a C4 joint and dielectric layers.](image)

![Fig. 9 Contour of first principal stress in the low-k dielectric layer under bump point C.](image)
are approximately double of Si interposer, and the stress of glass-B interposer is approximately double of glass-A interposer. CTE of the interposers can be considered as dominant factor based on this result. Stress of the MCM FCP-BGA is much higher than that of Si or glass interposer. In case of organic interposer, the stress is approximately 1.9 times higher than MCM FCP-BGA. This result indicates that stress and damage in the low-k dielectric layer under the C4 bump pad needs to be carefully evaluated in the product design with organic interposer. Stiffener could be an option for the flip chip assembly with an organic interposer, but a study with a stiffener was not performed here.

3.2 After interposer mount reflow

We evaluated stress of solder joint between an interposer and an organic substrate with model-b to model-j (Si and glass interposers only). The original model was modified by removing solder bumps and adding underfill with a composite material property of underfill resin and solder bump. The reference temperature is set at 180°C.

Figure 11 is a contour of Z-direction displacement of the assembled form for model-c. Figure 12 shows the Z-direction displacement at the corner point B. Si interposers have higher displacement than glass interposers after interposer mount although Si interposers have lower displacement after chip mount as shown in Fig. 7.

We analyzed von Mises stress of solder joint between an interposer and an organic substrate at the corner solder ball point D as shown in Fig. 13. Unlike the previous results of first principal stress in the low-k dielectric layer under the C4 bump, Si interposer has the highest von Mises stress, and glass B interposer has the lowest stress. This is due to the mismatch of CTE between interposer and organic substrate. After chip mount on the Si/glass interposers, Z-direction displacement is positive at the corner point B. But the displacement turns to be negative for all cases because of higher CTE of thick organic substrate. Data trend in Fig. 13 implies two major factors, elastic modulus and CTE, to reduce von Mises stress at solder joint. Si and glass-A interposers have similar CTE, but Si interposer has approximately two times higher elastic modulus compared to glass-A interposer. Approximately
50% reduction of elastic modulus results in about 20% reduction of von Mises stress by analyses of Si and glass-A interposer models. Glass-A and glass-B interposers have similar elastic modulus, but glass-B interposer has approximately one and half times higher CTE compared to glass-A interposer. Approximately 50% increase of CTE results in about 18% reduction of von Mises stress by analyses of glass-A and glass-B models.

Although we have not evaluated warpage of assembled interposers with chips and underfill, we presume assembled Si interposers have smaller warpage than glass interposers. This presumption implies that Si interposers have higher process yield and wider process margin at interposer mount process. On the other hand, solder joint’s reliability of Si interposers would be lower than that of glass interposers because Si interposers have higher von Mises stress than glass interposers. Manufacturability and reliability of solder joints needs to be experimentally evaluated with variable interposer materials, variable interposer sizes, and variable chip size combinations in order to optimize product design.

4. Summary

We investigated feasible interposer designs with a set of assumptions for Si, glass and organic interposers. Then we performed FEM mechanical analysis at two phases in the assembly process flow (1) after flip chip reflow, before underfill apply and (2) after mount of assembled interposer on a base organic substrate. After flip chip reflow, the highest Z-direction displacement of Si or glass interposer appears at the corner where the smaller chip (memory) is mounted nearby. This behavior is a result of CTE mismatch between interposer material and RDL. Organic interposer shows different warpage behavior from Si/glass interposer because of its material property.

First principal stress occurs in the low-k dielectric layer under the corner bump of the logic chip was investigated using multiscale modeling. The first principal stresses with Si/glass interposer are approximately 10% to 40% of the stress with MCM FCPBGA. On the other hand, the stress with organic interposer is approximately 1.9 times higher than the stress with MCM FCPBGA.

Von Mises stress was analyzed at the corner solder joint between Si or glass interposer and the base organic substrate. The analysis results indicate that Si interposer has the highest von Mises stress. We presume assembled Si interposer has the smallest warpage. There would be a trade off between manufacturability and reliability of the solder joints.

It is necessary to understand how key factors, i.e. stress in the low-k dielectric layer under C4 pad, manufacturability of interposer mount process, and reliability of solder joint, changes with variables such as interposer material, interposer size, and chip size for optimization of product design.

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References

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