[Technical Paper]

Analysis of Heat Generation from a Power Si MOSFET

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(Received August 2, 2013; accepted November 5, 2013)

Abstract

This paper describes the thermal properties of power Si MOSFETs. Recently, the thermal problems of driving devices have been gaining attention. The thermal design of semiconductor chips is important since the main heat source in a driving device is the semiconductor chips. Power Si MOSFETs, which are widely used as semiconductor devices in car electronics, have serious thermal problems, since they use high voltages. Therefore, the thermal properties of power Si MOSFETs must be studied in order to improve the reliability of the electronics. In this study, the thermal properties of power Si MOSFETs are discussed. To investigate these thermal properties, calculations are performed using electro-thermal analysis. From the calculations, a hot spot appears in the power Si MOSFET, and the hot spot temperature rises with increase in the applied voltage. Furthermore, the difference between the hot spot temperature and the average temperature becomes greater with the increase in applied voltage. The results indicate the risk of conventional thermal design with the assumption of uniform heat generation.

Keywords: Power Si MOSFET, Electro-Thermal Analysis, Thermal Management, Hot Spot, Electron Energy

1. Introduction

In recent years, electronics have been downsizing and thermal problems are becoming more serious. Therefore, the thermal design of electronics is becoming more important. Semiconductor devices are one of the main heat sources in electronics, and are very sensitive to temperature. In car electronics, power Si MOSFETs have been widely used as current controlling devices. In the conventional thermal design of power Si MOSFETs, heat generation has been assumed to be uniform.[1, 2] However, researchers have investigated the non-uniform heat generation of submicron Si MOSFETs, which are used for signal processing in Large Scale Integration (LSI) packages, and the appearance of hot spots (local high temperature points).[3–6] The differences between power and submicron Si MOSFETs are the structures, the applied voltages, and the currents used. However, since the fundamental operating mechanism of power Si MOSFETs is the same as that of submicron Si MOSFETs, there is the possibility of hot spots forming in power Si MOSFETs as well. Other studies have discussed the temperature dependence of power device characteristics.[1, 2, 7] The literature focused only on the relationship between temperature and current in the circuit model,[7] the package structure dependence of the electrical characteristics,[1] or the ther-

mal non-uniformity over large areas (wafer level) in consideration of the thermal interaction between adjacent devices.[2] However, these previous studies have not focused on the details of heat generation and temperature distribution inside the power Si MOSFET. Since the reliability of a power Si MOSFET is strongly dependent on temperature, non-uniform heat generation and the risk of hot spots is an important consideration for more accurate thermal designs of power Si MOSFETs.

In considering the heat generation and temperature distribution of a power Si MOSFET, the non-equilibrium state between the electron energy and the lattice energy becomes important.[8] In the previous studies of heat generation in semiconductors, the researchers have found that the non-equilibrium state between the electron energy and lattice energy occurs under an electric field of more than 10^7 V/m. Since the characteristic length scale of a power Si MOSFET is $1\text{ }\mu\text{m}$ and the applied voltage is more than 10 V, the electric field in a power Si MOSFET exceeds 10^7 V/m. Therefore, the non-equilibrium state between the electron and lattice energies should be considered for accurate heat generation and temperature distribution of a power Si MOSFET. Therefore, in this study, to calculate the non-equilibrium state, electro-thermal analysis is employed.

Electro-thermal analysis is also well known as a hydrodynamic model, and an attractive method for predicting the heat generation of a semiconductor device.[8] The method is derived from the Boltzmann Transport Equation (BTE). Electro-thermal analysis consists of the continuity, momentum conservation, and energy conservation equations, which are the zeroth, first, and second moments of the BTE. In electro-thermal analysis, electron flow is assumed to be a continuum, and electron and lattice energy are considered separately. Therefore, by employing electro-thermal analysis, the non-equilibrium state between the electron and lattice energies can be considered.

In this study, by employing electro-thermal analysis to consider the non-equilibrium state between electron energy and lattice energy, the thermal properties of power Si MOSFET are explored. This paper shows the fundamental temperature distribution of a power Si MOSFET and the dependence of the temperature distribution on the applied voltage. Further, the risk of thermal design with an assumption of uniform heat generation is discussed.

2. Electro-thermal Analysis

The governing equations of electro-thermal analysis consist of Poisson's equation, the continuity equation, the momentum conservation equation, the energy conservation equation for electrons, and the heat conduction equation as shown below.[8, 9]

$$\nabla^2 \phi = -\frac{q}{\epsilon_s} (N_D - n - N_A + p) \quad (1)$$

$$\frac{\partial n}{\partial t} + \nabla \cdot (nv) = 0 \quad (2)$$

$$\frac{\partial v}{\partial t} + v \cdot \nabla v = -\frac{qE}{m^*} - \frac{1}{nm^*} \nabla \cdot (nk_B T_e) - \frac{v}{\tau_m} \quad (3)$$

$$\begin{aligned} \frac{\partial W_e}{\partial t} + \nabla \cdot (v_e W_e) - q n_e v_e \cdot \nabla \phi + \nabla \cdot (v_e n_e k_B T_e) \\ - \nabla \cdot (\kappa_e \nabla T_e) = -\frac{W_e - W_{e0}}{\tau_E} \end{aligned} \quad (4)$$

$$\rho c \frac{\partial T_L}{\partial t} - \nabla \cdot (\kappa_L \nabla T_L) = \frac{W_e - W_{e0}}{\tau_E} \quad (5)$$

Equation 1 is Poisson's equation. Here, ϕ is the electrical potential, q is the elementary charge, ϵ is the permittivity of silicon, N_D is the donor density, N_A is the acceptor density, n is the electron number density, and p is the hole number density. Equation 2 is the continuity equation. Here, t indicates time and v means the electron velocity. The momentum conservation equation can be written as

shown in Eq. 3, where E is the electric field, m^* is the electron effective mass, k_B is the Boltzmann constant, and τ_m is the momentum relaxation time. Equation 4 is the electron energy conservation equation. Here, κ_e is the electron thermal conductivity, τ_E is the energy relaxation time, W_e is the electron energy, and W_{e0} is the lattice energy. W_e and W_{e0} are described below.

$$W_e = \frac{1}{2} n m^* v^2 + \frac{3}{2} n k_B T_e \quad (6)$$

$$W_{e0} = \frac{3}{2} n k_B T_L \quad (7)$$

The electron energy is the sum of the kinetic energy and the thermal energy of the electron. The right-hand side term of Eq. 4 measures the energy transfer between the electron and the lattice. This becomes the heat generation in Eq. 5. W_{e0} is the electron energy, which is equal to the lattice energy. In other words, W_{e0} is the lattice thermal energy.

In this study, the following fundamental parameters of silicon are employed: the temperature dependence of the carrier density of intrinsic silicon with the assumption of a nondegenerate semiconductor is described below.[10]

$$n_i^2 = 4 \left(\frac{2\pi k_B T_L}{h^2} \right)^3 m^{*\frac{3}{2}} m_h^{*\frac{3}{2}} \exp \left(-\frac{E_G}{k_B T_L} \right) \quad (8)$$

Here, n_i is the intrinsic carrier density, h is Planck's constant, m_h^* is the hole effective mass, and E_G is the energy band gap of silicon. From Eq. (8), if the temperature is 800 K, the intrinsic carrier density is lower than 10^{22} 1/m^3 , and this value is smaller than the doping density of this study. The electron mobility model is as follows.[11, 12] In this study, impurity scattering and phonon scattering are considered. The impurity scattering dependence of electron mobility is shown in Eq. (9).

$$\mu_e^I = 90 \times 10^4 \left(1 + \frac{2 \times 10^{24}}{CI} \left(\frac{T_L}{300} \right) \right) \quad (9)$$

Here, CI is the impurity density. The phonon scattering (temperature) dependence is given by:

$$\mu_e^L = \frac{1}{\frac{1}{0.4195 \left(\frac{T_L}{300} \right)^{-1.5}} + \frac{1}{0.2153 \left(\frac{T_L}{300} \right)^{-3.13}}} \quad (10)$$

Then, the dependence of the electron mobility on impurity and phonon scattering can be described as follows:

$$\mu_e^{LI} = \left(\frac{1}{\mu_e^I} + \frac{1}{\mu_e^L} \right)^{-1} \quad (11)$$

Further, for strong electric fields, the electron mobility strongly depends on the electric field, and the electron

velocity is saturated. This effect is given as:

$$\mu_e^{LIE} = \frac{\mu_e^{LI}}{\sqrt{1 + (\mu_e^{LI})^2 \left(\left(\frac{E}{\mu_e^{LI} A_e} \right)^2 + \left(\frac{E}{\mu_e^{LI} B_e} \right)^2 \right)}} \quad (12)$$

where A_e is 3.5×10^5 , F_e is 8.8, and B_e is 7.4×10^5 . Using the above electron mobility, the momentum relaxation time can be obtained as follows:

$$\tau_m = \frac{\mu_e m^*}{q} \quad (13)$$

In the calculation, the momentum relaxation time is applied to Eq. (3).

3. Calculation Model

In this study, to investigate the fundamental properties of a power Si MOSFET, two-dimensional steady-state analyses are performed. Figure 1 shows the structure of the modeled power Si MOSFET device used in this study, which is a normal vertical-type MOSFET.[13] On the top of the model, a source electrode and a gate electrode are set, and a drain electrode is located at the bottom of the model. The calculation domain is $7.2 \mu\text{m} \times 100 \mu\text{m}$. The electron channel length is assumed to be $1.0 \mu\text{m}$. The gate oxide thickness is set at 100 nm, the doping density of the n^+ region is set at 10^{25}m^{-3} , and the p region and n^- region are both 10^{22}m^{-3} .

The source electrode is grounded, the voltage applied to the gate electrode is changed from 5 to 20 V, and the voltage applied to the drain electrode is changed from 0 to 50 V.

Following are the boundary conditions. For the electrical potential, the voltages of the source and the drain electrode are set at the source voltage and the drain voltage. Under the gate oxide, the equation derived from Gauss'

law is applied as:

$$\epsilon_{ox} \nabla \phi_{ox} = \epsilon_s \nabla \phi_e \quad (14)$$

where ϵ_{ox} is the permittivity of silicon oxide. The rest of the boundary has a zero gradient of potential as a boundary condition. For carrier density, the constant value of the initial density is given at the source and the drain electrode interfaces. The zero gradient boundary condition of the carrier normal to the boundary is given at the rest of the boundary. For the carrier velocity, the velocity is set to zero perpendicular to the boundary except under the source and the drain electrodes. For carrier temperature, a constant temperature, $T_e = 350 \text{ K}$, is assumed at the bottom surface. The carrier temperature and the lattice temperature are assumed to be the same value at the source and drain electrode. Adiabatic boundary condition is applied to the other boundaries. For lattice temperature, it is assumed to be constant temperature of $T_L = 350 \text{ K}$ at the bottom surface, and an adiabatic boundary condition is applied to the other boundaries.

Most of the physical properties and constants are taken from the standard literature.[10]

4. Results and Discussions

To validate this calculation, Fig. 2 shows the distribution of electron number density, and Fig. 3 shows the vectors of electron flow.

In Fig. 2, the gate and drain voltages are 20 V. In this figure, the bottom surface corresponds to Fig. 1. In the bottom surface, the x- and y-axes correspond to the X- and Y-axes in Fig. 1, and the back side and front side in Fig. 2 show the upper and lower surfaces of the device in Fig. 1, respectively. Figure 2 is the enlarged view around the n^+ and p regions of Fig. 1. The x-axis shows $0\text{--}7 \mu\text{m}$, and the y-axis shows $0\text{--}10 \mu\text{m}$. As indicated in this figure, the electron number density in the n^+ type semiconductor region

Fig. 1 Modeled device structure.

Fig. 2 Distribution of electron number density in the case of $V_G = 20 \text{ V}$ and $V_D = 20 \text{ V}$.

Fig. 3 Vectors of electron flow in the case of $V_G = 20$ V and $V_D = 20$ V.

is 10^{25} m^{-3} , which is the same value as the initial electron number density. In the n^- type semiconductor region, the electron number density is almost the same as the initial value. In addition, the electron number density is high near $y = 0$, and between 2 and $7.2 \mu\text{m}$ in the x -axis, because this area is under the gate electrode. Electrons are gathered near the gate electrode, because a positive voltage is applied to the gate electrode. A part of the high electron number density near $y = 0$ in a p type semiconductor is called an electron channel. The generation of an electron channel is a fundamental MOSFET property.

Figure 3 shows the electron flow vectors for $V_G = 20$ V and $V_D = 20$ V. In this figure, the range of the x -axis shows the whole range of the modeled device. The y -axis shows $0\text{--}2 \mu\text{m}$ from the Y -axis of Fig. 1. As indicated by this figure, electrons flow from the source electrode through the electron channel to the drain electrode. This is a fundamental MOSFET property.[13] In a p type semiconductor, electrical resistance is high, because the electron number density is low. However, as indicated in Fig. 2, in a p -type semiconductor, an electron channel is generated near the gate electrode. Therefore, as indicated in Fig. 3, electrons flow from the source electrode through the electron channel to the drain electrode. In other words, current flows from the drain electrode to the source electrode. This is a fundamental MOSFET property.

The results of Figs. 2 and 3 indicate that these calculations can estimate appropriate MOSFET characteristics. In our model, a current of about 70 A/m flows at $V_G = 20$ V and $V_D = 20$ V under the temperature conditions of Fig. 4. Further, we compared the data sheet of a commercial power Si MOSFET, which has a similar structure to the modeled device, and confirmed that the tendency of the calculated drain current showed good agreement with an

Fig. 4 Temperature distribution of modeled device in the case of $V_G = 20$ V and $V_D = 20$ V.

Fig. 5 Applied voltage dependence of maximum lattice temperature.

actual one.

Figure 4 shows the temperature distribution of the modeled device. In this case, the gate voltage and drain voltage are the same as those of the previous result ($V_G = 20$ V and $V_D = 20$ V). The bottom surface of this graph corresponds to Fig. 1 in the same way as Fig. 2 does. This is an expanded temperature distribution figure of the modeled device: the x -axis and the y -axis both show $0\text{--}7 \mu\text{m}$. In this figure, a hot spot appears in the modeled device, with a temperature of about 600 K . The average temperature of the modeled device is about 541 K . Therefore, the difference between the hot spot temperature and the average temperature is about 59 K . This result indicates the risk of assuming uniform heat generation when a power Si MOSFET is driven to a steady state.

Figure 5 shows the dependence of the hot spot temperature (maximum lattice temperature) on the applied voltage. As indicated in this figure, the hot spot temperature becomes higher with an increase in the applied voltage. In this result, the hot spot temperature is more than 750 K for any gate voltage when the drain voltage is 50 V . However,

Fig. 6 Temperature difference between average lattice temperature and maximum lattice temperature.

if the temperature difference between the hot spot temperature and the average temperature maintains a constant value, it is not difficult to estimate the hot spot temperature from the average temperature. Thus, the difference between the hot spot temperature and the average temperature should be discussed.

Figure 6 shows the difference between the maximum temperature (hot spot temperature) and the average temperature. In this figure, the temperature difference rises with the increase in applied voltage, and the temperature difference is more than 100 K in any gate voltage when the drain voltage is 50 V. Therefore, when the modeled device is driven to a steady temperature state, the risk of thermal design problems with the assumption of uniform heat generation becomes higher with increasing applied voltages. Further, since the temperature difference depends both on the drain and gate voltages, and the dependence is not linear, estimating the hot spot temperature from the average temperature is difficult.

5. Conclusion

The thermal properties of power Si MOSFETs were discussed using an electro-thermal analysis. The calculation results showed a hot spot appearing in a power Si MOSFET. The hot spot appears between the p and n⁻ type semiconductors, near the electron channel. Furthermore, details of the effect of the applied voltage on the hot spot temperature and the temperature difference between the hot spot and the average temperature were discussed. The results indicate that the hot spot temperature rises with increasing applied voltages, and the temperature difference between the hot spot temperature and the average temperature becomes greater with the increase in the applied voltage. The result indicates the risk of conven-

tional thermal design with the assumption of uniform heat generation.

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