[Tutorial Paper]

Measuring Method for TSV-based Interconnect Resistance in 3D-SIC by Embedded Analog Boundary-Scan Circuit

Shuichi Kameyama*, Masayuki Baba*, Yoshinobu Higami**, and Hiroshi Takahashi**

*Fujitsu Limited, 4-1-1 Kamikodanaka, Nakahara-ku, Kawasaki-shi 211-8588, Japan

**Graduate School of Science and Engineering, Ehime University, 3 Bunkyo-cho, Matsuyama-shi 790-8577, Japan

(Received July 24, 2014; accepted November 5, 2014)

Abstract

In this paper, we introduce a method to measure the resistance of high density post-bond Through Silicon Via (TSV) including serial micro-bumps and bond resistance in Three Dimensional Stacked IC (3D-SIC). The key idea of our technology is to use Electrical Probes embedded in stacked silicon dies. It is a measuring circuit based on Analog Boundary-Scan (IEEE 1149.4). The standard Analog Boundary-Scan structure is modified to realize high measuring accuracy for TSVs in 3D-SIC. The main contribution of the method is to measure the resistance of high pin count (e.g. >10,000) post-bond TSVs accurately. Electrical Probes correspond to the high density of TSV (e.g. < 40 μm pitch) and work like Kelvin probe. The measurement accuracy is less than 10 m Ω . We also introduce the preliminary results of small scale measuring experiments and the results of SPICE simulation of large scale measuring circuits.

Keywords: 3D-SIC, TSV, Interconnect, Analog Boundary-Scan, Resistance Measurement

1. Introduction

Manufacturing defects related to TSVs (e.g. voids or pinholes of TSV, contamination or height variation of micro-bumps, misalignment during bonding etc.) cause interconnect failures between dies in 3D-SIC.[1] Boundary-Scan Test (IEEE 1149.1) is normally used to detect interconnect failures of post-bond dies in 3D-SIC (See Fig. 1).[2] The Boundary-Scan Test is useful for detecting complete open/short faults, but it is not able to detect resistive open/short faults. Furthermore, it is not able to measure

Fig. 1 Manufacturing defects and Boundary-Scan Test in 3D-SIC.

the value of the resistance. However, it is very important to measure the post-bond TSV-based interconnect resistance (TSV, micro-bumps/Cu-pillars, bonding resistance) individually for the evaluation of manufacturing processes. If it is possible to measure the value of each TSV-based interconnect resistance individually, we can find the outliers of a standard deviation (see Fig. 2). By eliminating the cause of the outliers, we can improve the manufacturing process, and then we can get a high yield of 3D-SIC.

In general, it is impossible to measure the value of each post-bond TSV-based interconnect resistance individually by conventional measuring methods such as Daisy Chain measurement or Kelvin measurement with mechanical probing. To overcome this problem we proposed a new

Fig. 2 Outlier of TSV-Based interconnects.

measuring method by using Electrical Probe embedded in silicon.[3, 4]

This paper introduces a new method for measuring the resistance of high density post-bond TSV-based interconnects in detail.

The remainder of this paper is organized as follows. Section 2 explains conventional methods and the new idea for measuring TSV resistance. Section 3 describes the resistance measuring method using conventional Analog Boundary-Scan technology. This section also describes the problems of conventional Analog Boundary-Scan in measuring the small resistance value of TSVs. Section 4 proposes methodologies to solve the problems. Section 5 presents the results of a small-scale experiment to confirm the feasibility of the methodologies and their accuracy of measurement. It also provides the results of an analog simulation for application to large-scale 3D-SIC. Finally, section 6 concludes this paper.

2. Conventional Methods and the New Idea for Measuring TSV Resistance

Several measuring methods for TSV-based interconnect resistance have been presented.[5, 6] The most well-known is Daisy-chain measuring method showed in Fig. 3 (a). In this method, many ($N = 100 - 1,000$ or $>1,000$) TSVs are connected serially by Re-Distribution Lines (RDLs) as a daisy chain, then the total resistance is measured once from both ends of the chain. The single TSV-based interconnect resistance can be determined by dividing the measured value by N . This method makes it very easy to measure the TSV-based interconnect resistance. However, although it provides an average value, it cannot provide an individual resistance value. As a result, it is impossible to find the outlier of TSV-based interconnects. The other method is Kelvin measurement (otherwise known as 4-wire measurement) with mechanical probes showed in Fig. 3 (b). When a very low resistance like a single TSV is

measured, the measurement error introduced by the resistance of the measurement path will be substantial. In the Kelvin method, the voltage sensing path is separated from the current forcing path so that we can measure the voltage across the target resistor at the nearest points avoiding error affected by the voltage drop on the current forcing path. The voltage measured by the voltmeter through the sensing path is essentially the same as the voltage across the resistance to be measured, because the voltage drop of the sensing path is very small due to the miniscule sensing current. Therefore the TSV-based interconnect resistance that is milliohm order can be measured accurately by the Kelvin method with mechanical probes. However the Kelvin method needs four large scale probing pads and two additional TSVs per one TSV, additionally it takes quite long time to probe many TSVs mechanically. Therefore it is useful to measure a small number of TSVs, but it is difficult for high density (<40 μm pitch) and high pin-count ($>10,000$) post-bond TSVs.

In order to overcome the above challenges of using the conventional methods, we have proposed a new method to measure the resistance of high density post-bond TSV-based interconnects (Fig. 4). The scope of the resistance measurement in this paper includes TSV, micro-bumps/

Fig. 4 Internal Probing of a 3D-SIC.

Fig. 3 Conventional TSV resistance measuring method.

Cu-pillars and bonding. BEOL (Back End Of Line) and RDL (Re-Distribution Line) are not included in this paper because they are already mature technologies. The proposed method is to use Electrical Probes embedded in the stacked silicon dies. The Electrical Probe is a measuring circuit based on Analog Boundary-Scan (IEEE 1149.4). We modified the standard Analog Boundary-Scan structure to realize high measurement accuracy for TSVs in 3D-SIC.

By using the proposed method the TSV-based interconnect resistance can be measured individually, so that it is able to find the outlier of TSV-based interconnects. The Electrical Probe is a small silicon circuit, so that it is able to be disposed for the high density (<40 μm pitch) and high pin-count (>10,000) post-bond TSVs.

The proposed method is very useful for yield learning of 3D-SICs, since it allows us to measure the resistance of the high density (<40 μm pitch) and high pin-count (>10,000) post-bond TSV-based interconnects in order to be able to find the outliers of TSV-based interconnect. Furthermore it is not only useful for yield learning, but also is useful for monitoring changes of the TSV-based resistance in the field.

3. Problems of Conventional Analog Boundary-Scan for TSV Resistance Measurement

This section describes the resistance measuring method using conventional Analog Boundary-Scan technology and then describes problems in measuring TSV-based interconnect resistance.

3.1 Analog Boundary-Scan

Analog Boundary-Scan IEEE 1149.4[7] is a standard that is extended to analog circuits on the basis of digital Boundary-Scan IEEE 1149.1.[8] Analog Boundary-Scan has the capability of not only interconnection test of analog nets, but also measuring the L, C or R value of components connected between ICs.[9] Figure 5 shows the overall architecture of Analog Boundary-Scan. An ABM (Analog Boundary Module) is implemented between an analog I/O (Input/Output) pin and the Analog Core. ABMs and a TBIC (Test Bus Interface) are connected by an internal analog BUS (AB1, AB2). Analog signals on AB1 and AB2 pass through the TBIC to an external analog BUS (AT1, AT2). AT1 and AT2 are connected to external analog measurement equipment. Figure 6 shows the Standard ABM circuit which consists of six analog switches (A-SW) and one comparator.

Fig. 5 Analog Boundary-Scan Circuit.

Fig. 6 ABM Circuit.

Fig. 7 Standard resistance measuring method.

3.2 Standard resistance measuring method by 1149.4

Figure 7 shows the measurement circuit configuration and principles of the IEEE 1149.4 Standard. Measuring procedure is as follows:

Step1: All A-SWs of the ABMs and TBICs are set as shown in Fig. 7-(a), and the ground-referenced voltage $V1$ at the left side of resistance Z is measured by voltmeter V while constant current I_S is applied to Z by a constant current source.

Step2: All A-SWs of the ABMs and TBICs are set as shown in Fig. 7-(b), and the ground-referenced voltage $V2$ at the right side of resistance Z is measured by voltmeter V while constant current I_S is applied to Z by a constant current source.

Step3: A control computer calculates by Equation (1), and provides the resistance value of Z .

$$Z = (V1 - V2) / I_S \quad (1)$$

It is important to note that $V1$ and $V2$ measurements are referenced to ground level.

3.3 Problems of conventional Analog Boundary-Scan for TSV resistance measuring

IEEE 1149.4 Standard document[7] at chapter 9 describes as “An objective of this standard is to facilitate measurement of complex impedances with accuracy better than $\pm 1\%$ when measuring impedances between $10\ \Omega$ and $100\ k\Omega$ ”. However, the TSV-based interconnect resistance value is several tens or hundreds of milliohms, which is far smaller than the expectation of the Standard. Therefore, if we try to measure the small TSV-based interconnect resistance using the conventional 1149.4 Standard as is, the measurement accuracy will be unacceptable or the resistance will be immeasurable in the worst cases due to the following problems.

A) Problem of the ground-referenced voltage measuring method

The TSV-based interconnect resistance value (several tens or hundreds of milliohms) is less than one-thousandth of the resistance value of A-SWs in the ABMs and TBICs (several hundreds or thousands of ohms). Therefore a voltage drop across the resistance Z by applying constant current I_S is less than one-thousandth of the voltage drop across the A-SWs. If the accuracy of measurement for $V1$ and $V2$ in Fig. 7 is 0.1% (one-thousandth), the voltage measurement error and the voltage drop across the resistance Z will be almost the same. As shown in Fig. 8, if the measurement error (ϵ_1, ϵ_2) of the ground-referenced voltages $V1, V2$ are equal or larger than the difference between $V1$ and $V2$, the calculation results by the Equation (1) for the resistance Z will have a large error or does not make sense (e.g. negative resistance). Hence the ground-referenced voltage measuring method is not practical for measuring

Fig. 8 Measurement error in ground-referenced voltage measuring method.

Fig. 9 Measuring effect caused by line resistance (BEOL & RDL).

the typically very small values of TSV-based interconnect resistance.

B) Problem of line resistance in the die

Line (BEOL and RDL) from an ABM circuit to a micro-bump (or TSV) in the die has a resistance whose value might be several tens or hundreds of milliohms (Fig. 9). This causes large errors in measuring the TSV-based interconnect resistance value (several tens or hundreds of milliohms), because the resistance of the line is added to the value of the measured resistance Z . If an ESD-protection resistor exists in the line, the measurement error is further increased.

C) Problem of leak current of A-SWs in case of a large number of TSVs

In case of measuring resistances of a large number of TSVs (e.g. tens of thousands), the ABMs same as the number of TSVs are connected to the internal analog BUS (AB1, AB2), and the effect of the leak current of A-SWs increases, then the measurement error increases.

4. Proposed Measuring Method

As shown above, the relatively high value of A-SW resistance in ABMs makes it impossible to accurately measure extremely small TSV-based interconnect resistances using conventional Analog Boundary-Scan methods. Therefore, we propose a new method to enable measuring TSV-based interconnect resistance accurately by modifying the conventional Analog Boundary-Scan method.

A) Floating measuring method

The conventional measuring method causes significant measurement error by measuring ground-referenced voltage. We propose a new measuring method utilizing float-

ing measurements to minimize the error. The circuit configuration and setting of A-SWs to realize this method is shown in Fig. 10. In this way, both constant current application and voltage measurement are enabled to float from ground. This enables direct measurement of the voltage drop ΔV across resistance Z . The small voltage drop across resistance Z can, thus, be measured with high resolution. It also enables highly accurate measurement since it is not affected by ground noise. Furthermore, it needs to measure only one time, and then the test time is shortened.

B) Complete separation of the current path and the voltage path

As mentioned in section 3.3 B), the resistance of the line (BEOL and RDL) from an ABM circuit to a micro-bump (or TSV) causes large measuring errors. In order to avoid the line resistance influence, the voltage across the resistance Z should be measured at the closest sensing position. The proposed method separates the current path and the voltage path completely until the closest point of the resistance Z . One of the specific routing methods is to separate one measuring line in the ABM circuit to two lines (current and voltage), and connect these lines to the terminal of resistance Z through BEOL and RDL in the die. The other method is to use two ABMs for one terminal of resistance Z , and to wire the line from each ABM to the Z terminal through the BEOL and RDL in the die (Fig. 13). In case of the latter, re-design of the ABM macro is not required, and the ESD protection resistance is not a factor. The proposed method allows measuring Z accurately without measuring error caused by the resistances of BEOL, RDL or the ESD protector.

An example circuit of 3D-SIC implemented the proposed method A) and B) is shown in Fig. 11. Note that TBIC and control logic circuits are omitted.

In this way, the Kelvin measuring method is realized in the silicon. The voltage sensing path is separated from the current forcing path so that we can measure the voltage

Fig. 10 Floating measuring method for TSVs.

across the TSV-based interconnect resistance at the nearest points avoiding error affected by the voltage drop on the current forcing path. The voltage measured by the voltmeter through the sensing path is essentially the same as the voltage across the TSV-based interconnect resistance, because the resistance value of the sensing path (A-SWs in the ABMs and TBICs and so on) is several hundreds or thousands of ohms, whereas the input impedance of the voltmeter is more than 10 Giga ohms, consequently the voltage drop of the sensing path is negligible due to the difference of more than 10^6 times. Therefore the TSV-based interconnect resistance that is milliohm order can be measured accurately by the proposed method.

C) Segmenting the internal analog BUS (AB1, AB2)

In order to avoid the influence of A-SW leak currents, a number of the ABMs (thousands or tens of thousands) connected to the internal analog BUS (AB1, AB2) are grouped and the internal analog BUS is segmented. Then a TBIC circuit is used in each segmented internal analog BUS. An example of an internal analog BUS divided into m segments is shown in Fig. 12. By the segmentation, the penalty of leak current to measurement error decreases to $1/m$. The desired number of segments is determined by

Fig. 11 Floating measurement and V/I path isolation.

Fig. 12 Grouping the internal analog buses.

the leak current characteristic of the A-SW in the die.

As mentioned above, the proposed method can decrease measurement error caused by A-SW leak currents.

In addition, by this new method, the insulation resistance between neighboring TSVs or a TSV to ground can be measured as well as the TSV-based interconnect resistance. In case of the insulation resistance measurement, the 2-wire measurement is used instead of the 4-wire (Kelvin) measurement, and the VSIM (Voltage Source and Current measure) method is used instead of the ISVM (Current Source and Voltage measure) shown in Fig. 10.

5. Experimental Result

In order to evaluate the feasibility of the proposed method, 1) A small circuit experiment was done for theoretical verification and to verify the measurement accuracy, and 2) A SPICE simulation of large circuits was done.

5.1 Small circuit experiment

A small circuit experiment was performed for theoretical verification and evaluating measurement accuracy. Figure 13 and Fig. 14 show the experimental set up. Analog Boundary-Scan ICs (MB87V722, 0.18 μ m CMOS) were used for this experiment. The resistance of the A-SW is approximately 100 ohm. KEITHLEY 2612 was used as a current source, and flowed 1 mA (0.02% + 2.5 μ A) at mea-

Fig. 13 Experimental circuit block diagram.

Fig. 14 Experimental equipment.

surement. KEITHLEY 2182A A was used as Digital voltmeter, its input impedance is >10 G Ω . A conventional resistor was used as a pseudo TSV, its resistance value having been accurately measured by conventional means using KEITHLEY 2612 & 2182A before incorporation in the experimental circuit. This measured resistance value was used as a reference for evaluating the accuracy of the value measured using the new method.

Table 1 shows the experimental result. From the result, the measuring error in the 100 m Ω range is 3% or 3 m Ω . This result means the proposed method is capable of measuring the small resistance of TSV-based interconnects within practical accuracy. The result also indicates the accuracy is lower at lower range. From the experimental result, we show the lower resistance is easily affected from external noise or current drift since the voltage drop is smaller. If a constant current of 1 mA is applied to a resistor 100 m Ω , the voltage drop of the resistor is 100 μ V, which is quite small.

5.2 SPICE simulation for large circuit

As mentioned in section 3.3 C), A-SW leak currents cause measurement errors when measuring resistances of large numbers of TSVs. We evaluated the relation between the measurement error and the number of ABMs (= number of TSVs) connected to the internal analog BUS (AB1, AB2). We used SPICE analog simulator for the evaluation. Then we verified the effect of our proposal for the leak current of A-SWs shown in section 4. C).

Table 2 shows the result of the simulation with conditions that the measurement error is caused by a leak current of A-SWs using a specific simulation model and does not include the effects of noise, etc. that may exist in real environments. The rightmost column of Table 2 presents the effect of our proposal for the leak current. The measurement error at 2,000 ABMs was reduced to 0.05% from

Table 1 Experimental results.

Range	Reference	Measured value	Absolute error	Relative error
1,000 m Ω	1,000 m Ω	990 m Ω	10 m Ω	1%
200 m Ω	219 m Ω	215 m Ω	4 m Ω	2%
100 m Ω	101 m Ω	98 m Ω	3 m Ω	3%

Table 2 Result of SPICE simulation for large circuits.

Number of ABM (=TSV)	10	200	2,000	200 $\times$ 10 (10 TBIC)
Relative error	0.00%	0.05%	0.48%	0.05%

0.48% (1/10) by the measure that 2,000 ABMs were grouped to ten 200 ABMs and 10 TBICs were deployed to each group. It certified that segmenting into 10 internal analog BUS circuits causes the leak current to decrease by a factor of ten. In this way, measuring of the tens of thousands of TSVs will be practical.

6. Conclusion

In this paper, we have presented a highly accurate measuring method for the small resistance value of TSV-based interconnects between dies in post-bond 3D-SIC. The proposed method uses embedded Analog Boundary-Scan circuits. Furthermore, we have provided an experimental result that confirms the proposed method can accurately measure within 3% at 100 mΩ. We also indicated the possibility to apply to tens of thousands of TSVs by SPICE simulation.

Tom DeMarco said, "You can't control what you can't measure." [10] In order to improve the yield of 3D-SIC, it is necessary to measure TSV-based interconnect resistances accurately. We hope the proposed method will allow accelerating the development of 3D-SIC.

Acknowledgment: Two of the authors (Y. Higami and H. Takahashi) were supported by JSPS KAKENHI 25330063.

References

- [1] E. J. Marinissen, "Testing TSV-Based Three-Dimensional Stacked ICs," Proc. DATE2010, pp. 1689–1694, 2010.
- [2] E. J. Marinissen, "Challenges and emerging solutions in testing TSV-based 2.5D- and 3D-stacked ICs," Proc. DATE2012, pp. 1277–1282, 2012.
- [3] S. Kameyama, M. Baba, Y. Higami, and H. Takahashi, "Precision Resistance Measurement method of TSVs in a 3D-SIC by Analog Boundary-scan," Vol. J97-D. No. 4, pp. 887–890, IEICE, 2014.
- [4] S. Kameyama, M. Baba, Y. Higami, and H. Takahashi, "Accurate Resistance Measuring Method for High Density Post- Bond TSVs in 3D-SIC with Electrical Probes," International Conference on Electronics Pack-aging (ICEP2014), TA4-4, pp. 117–121, 2014.
- [5] H. Chung, C. Y. Ni, C. M. Tu, Y. Y. Chang, Y. T. Haung, W. M. Chen, B. Y. Lou, K. F. Tseng, C. Y. Lee, and B. J. Lwo, "The Advanced Pattern Designs with Electrical Test Methodologies on Through Silicon Via for CMOS Image Sensor," Proc. ECTC2010, pp. 297–302, 2010.
- [6] M. Stucchi, D. Perry, G. Katti, and W. Dehaene, "Test structures for characterization of through silicon vias," Proc. CMTS2010, pp. 130–134, 2010.
- [7] IEEE Std 1149.4-1999, "IEEE Standard for a Mixed-Signal Test Bus," ISBN 0-7381-1755-2 SH94761, March 2000, IEEE.
- [8] IEEE Std 1149.1™-2001 (R2008), "IEEE Standard Test Access Port and Boundary-Scan Architecture," ISBN 0-7381-2944-5 SH94949, July 2001, IEEE.
- [9] K. Parker and S. Kameyama, "Boundary-Scan Handbook 3rd Edition, Japanese Version," Seizansha, Sagamihara, Japan, 2012.
- [10] T. Demarco, "Controlling Software Projects: Management, Measurement, and Estimation," Prentice Hall/Yourdon Press, 1982.

Shuichi Kameyama graduated from Oyama National College of Technology, Tochigi, Japan, in 1972. He joined Fujitsu Limited in 1972. Since then, he has been engaged in the development of test technologies. He received his Ph.D. degree from Ehime University, Ehime, Japan, in 2014.

Masayuki Baba
Yoshinobu Higami

Hiroshi Takahashi received the Dr. degree from Ehime University, Japan in 1996. Since 2010, he has been a Full Professor at Ehime University. From May 2000 to March 2001, he was a research fellow at the University of Wisconsin-Madison, USA. He received the IEICE Best Paper Award in 2011. His research interests are test generation and fault diagnosis for digital systems. Dr. Takahashi is a senior member of the IEEE and IEICE. He served as the Program Chair of the 2012 IEEE Asian Test Symposium.