1. Introduction

Recently, thermal problems of electronics become more serious, because electronics have been downsizing. Therefore, more accurate thermal design is required. The temperature distribution of a semiconductor chip, which is the main heat source in electronics, is generally assumed uniform in thermal design. However, because semiconductor chips have non-uniform temperature distribution, the temperature distribution should be considered for more accurate thermal design. One or more semiconductor devices are mounted in the semiconductor chip, and the thermal properties of these semiconductor devices are important for consideration of the temperature distribution of the chips.

Submicron Si MOSFET (metal-oxide-semiconductor field-effect-transistor) and power Si MOSFET are widely used in the chips. Submicron Si MOSFET is a transistor for signal processing, and power Si MOSFET is a transistor for control of amount of current. Both Si MOSFETs have the same operating principle, however, the structures are not same. Moreover, applied voltage for power Si MOSFET is larger than that for submicron Si MOSFET. Therefore, power Si MOSFET has large thermal problems. [1] Then, we focus on power Si MOSFET.

Because power Si MOSFET is a transistor to control amount of current, the behavior of electrons is very important. However, the behavior of electron depends on various factors (electrical filed, electron density, temperature and so on). When voltage is applied to semiconductor devices, electron flows from high to low electric potential. At this time, electron transfers the energy to lattice, and lattice temperature becomes higher. Electron mobility decreases with increase in lattice temperature, and electron velocity decreases. Therefore, the amount of current decreases. In other words, electron behavior changes when temperature changes. Thus, intensity of electric field is also changed by variation of temperature. The characteristics of semiconductor devices have a complex relationship with temperature. Therefore, to control amount of current accurately, the thermal properties of power Si MOSFET should be investigated. Then, we investigate the thermal properties of power Si MOSFET in this study.

We performed calculations to investigate the thermal properties of power Si MOSFET, because it is very difficult to measure temperature of the device. In previous calculations, the properties of semiconductor devices are investigated by electrical analysis or thermal analysis. [1–3] However, as described above, electron behavior...
interacts with lattice temperature. Therefore, to investigate accurate thermal properties of power Si MOSFET, we should consider not only lattice energy but also electron energy. Then electro-thermal analysis is an attractive method. In this study, we employ electro-thermal analysis for the calculation of the temperature distribution.

In previous study, we investigate the variation of hot spot temperature and the sifting of hot spot by changing applied voltages, and the effect of heat removal from the surface covered with resin of the device on the temperature distribution of power Si MOSFET.[4–6] In these calculations, we assumed a general bottom boundary conditions. In general thermal boundary condition, the bottom surface of the device is assumed constant temperature at 350 K.[7] However, in fact, it is difficult to keep the bottom temperature of power Si MOSFET at 350 K, because the bottom temperature of power Si MOSFET depends on the cooling performance. Additionally, the bottom temperature of the device has an effect on the electrical properties of power Si MOSFET, and has large effect on the temperature distribution. Therefore, the heat removal from the bottom of the device by cooling should be considered.

Then, in this study, we investigate the effect of cooling performance at the bottom surface on the bottom temperature, and the effect of the variation of the bottom temperature on the temperature distribution of power Si MOSFET using electro-thermal analysis. First, to investigate the effect of the cooling performance on the bottom temperature, we assume several heat transfer coefficients at the bottom of the device as a boundary condition. Then, to investigate the effect of the cooling performance on the temperature distribution of power Si MOSFET, the relationship between the hot spot temperature of the device and the bottom temperature is discussed using the calculation results with the boundary condition of the heat transfer coefficient.

2. Analysis Object and Model

Figure 1 shows the schematic view of the power Si MOSFET, which is the analysis object of this study. A vertical type power Si MOSFET package is focused on in this study. In this device, the source and the gate electrodes are on the top of the device, and the drain electrode is on the bottom of the device. And, as shown in this figure, this device has the iteration structure in the horizontal direction. In the perpendicular direction to the paper, the structure is uniform.

Figure 2 shows the analysis model of this study. As shown in Fig. 1, power Si MOSFET has iteration structure in the horizontal direction, and the structure is uniform in the direction normal to the paper. Therefore, we focus on a part of power Si MOSFET. And we perform two-dimensional analysis, because the structure is uniform in the perpendicular direction to the paper. In this calculation model, the analysis domain is $100 \times 7.2 \mu m^2$, and the characteristic length (gate length) is $1 \mu m$. And, we assumed the doping density of $n^+$ is $10^{25}$, $n^-$ is $10^{22}$, and $p$ is $10^{22}$ $1/m^3$. Then, the gate oxide thickness is 100 nm.

The model is divided into 52 (in x direction) $\times$ 116 (in y direction) meshes. Non-uniform meshes are applied with consideration for abrupt change of electron density around p-n junction.

3. Electro-thermal Analysis

The governing equations of electro-thermal analysis consist of Poisson’s equation, continuity equation, momentum conservation equation, energy conservation equation for electron, and heat conduction equation as shown below.[4–9]

$$\nabla^2 \phi = - \frac{q}{\varepsilon_s} (N_D - n - N_A + p) \quad (1)$$

$$\frac{\partial n}{\partial t} + \nabla \cdot (nv) = 0 \quad (2)$$

$$\frac{\partial v}{\partial t} + v \cdot \nabla v = \frac{qE}{m} - \frac{1}{nm^2} \nabla (nk_BT_e) - \frac{v}{\tau_m} \quad (3)$$
\[
\frac{\partial W_e}{\partial t} + \nabla \cdot (vW_e) - qnv \cdot \nabla \phi + \nabla \cdot (vnk_BT_e) - \nabla \cdot (\kappa_e \nabla T_e) = -W_e - W_{eo} \quad (4)
\]

\[
\rho \varepsilon \frac{\partial T_e}{\partial t} - \nabla \cdot (\kappa_e \nabla T_e) = \frac{W_e - W_{eo}}{\tau_e} \quad (5)
\]

Equation 1 is Poisson’s equation. Here, \( \phi \) is electrical potential, \( q \) is elementary charge, \( \varepsilon \) is permittivity of silicon, \( N_D \) is donor density, \( N_A \) is accepter density, \( n \) is electron number density and \( p \) is hole number density. In this calculation, \( \varepsilon \) is assumed constant. Equation 2 is continuity equation. Here, \( t \) indicates time and \( v \) means electron velocity. Momentum conservation equation can be written as shown in Eq. 3. Where, \( E \) is electric filed, \( m^* \) is electron effective mass, \( k_B \) is Boltzmann constant, \( T_e \) is electron temperature. \( \tau_m \) is momentum relaxation time, which is described in Eq. (6).

\[
\tau_m = \frac{\mu_em^*}{q} \quad (6)
\]

Equation 4 is energy conservation equation of electron. Here, \( \kappa_e \) is electron thermal conductivity and \( \tau_e \) is energy relaxation time. \( \kappa_L \) is lattice thermal conductivity, and described in Eq. (7).

\[
\kappa_L = 154.86 \times \left( \frac{T_L}{300} \right)^{\frac{3}{2}} \quad (7)
\]

Where, \( T_L \) is lattice temperature. \( W_e \) is energy of electron and \( W_{eo} \) is energy of lattice. \( W_e \) and \( W_{eo} \) are described as below.

\[
W_e = \frac{1}{2}nmv^2 + \frac{3}{2}nk_BT_e \quad (8)
\]

\[
W_{eo} = \frac{3}{2}nk_BT_L \quad (9)
\]

Electron energy is a sum of kinetic energy and thermal energy of electron. Right hand side term of Eq. 4 means energy transfer between electron and lattice. This becomes heat generation in Eq. 5. \( W_{eo} \) is electron energy, which is equal to lattice energy. In other words, \( W_{eo} \) means lattice thermal energy. Table 1 shows employed parameters in this calculation.

### 4. Calculation Flow
To calculate the temperature distribution of power Si MOSFET, we employ our own code using FORTRAN. For diffusion terms, central difference scheme is applied. For advection term, first order upwind scheme is applied. Only Eq. 4 is discretized using power method. Figure 3 shows calculation flow. Poisson’s equation (Eq. (1)) is solved to obtain electrical field \( \phi \). And, momentum conservation equation (Eq. (3)) is solved for obtaining electron velocity \( \nu \). Then, electron density is obtained by solving continuity equation (Eq. (2)). And, energy conservation equation (Eq. (4)) is solved for obtaining electron temperature \( T_e \). When \( \nu, n \) and \( T_e \) reach steady state, the lattice temperature is calculated by solving heat conduction equation (Eq. (5)). The above procedure is repeated until the steady distributions are obtained.[10]

### 5. Boundary Conditions
Table 2 shows boundary conditions.[11] For electrical potential, the voltages of the source and the drain electrodes are set at the source voltage and the drain voltage. Under the gate oxide, the equation derived from Gauss’ law is applied as

\[
\varepsilon_w \nabla \phi_{ox} = \varepsilon_s \nabla \phi_s \quad (10)
\]

where \( \varepsilon_w \) means permittivity of silicon oxide. The rest of the boundary has zero gradient of potential as the boundary condition. For carrier density, the constant value of the initial density is given at the source and the drain electrode interfaces. Zero gradient boundary condition of carrier normal to the boundary is given at the rest of the boundary. For carrier velocity, the velocity is set to zero in the perpendicular direction to the boundary except under the source and the drain electrodes. For carrier temperature,
the carrier temperature and the lattice temperature are assumed to be the same value at the source and the drain electrodes. Adiabatic boundary condition is applied to the other boundaries.

Considering vertical type power Si MOSFET packages, for example TO (Transistor Outline) – 220 type package, the drain electrode side (the bottom surface in Figs. 1 and 2) is directly attached at a cooling plate, and the source electrode side (the top surface in Figs. 1 and 2) is packed by resin materials.[12] Therefore, we assumed the cooling effect from the top of the device is very small, we apply thermal insulating condition to the top of the device for the boundary condition of lattice temperature.[13] Additionally, to investigate the cooling effect at the bottom surface on the bottom temperature and the temperature distribution of the device, the following equation is employed to assume heat transfer from the bottom of the device.

$$q = h(T_L - T_a) \quad (11)$$

In Eq. 11, $T_a$ means ambient temperature. $h$ means heat transfer coefficient. The adiabatic boundary condition is applied to the other boundaries.

### 6. Analysis Conditions

In this calculation, the source is grounded (0 V), applied voltage to the drain electrode ($V_D$) shifts from 5 to 15 V, and the gate voltage ($V_G$) is fixed at 20 V. Moreover, to investigate the cooling effect at the bottom of the device on the bottom temperature and the temperature distribution of the device, the heat transfer coefficient at the bottom surface of the device is varied from $10^5$ to $10^8$ W/(m²·K). The maximum heat transfer coefficient of this calculation range corresponds to the cooling performance of boiling cooling.[14] Ambient temperature is assumed as 300 K. Most of the physical properties and constants are taken from the standard literature.[15] Before all discussions, the calculation results are compared with the data sheet of a commercial power Si MOSFET, which has similar structure of modeled device, and confirmed that tendency of calculated drain current showed good agreement with actual one.

### 7. Result and Discussion

Figure 4 shows temperature distributions of the modeled device when heat transfer coefficient at the bottom surface is $10^5$ and $10^8$ W/(m²·K). In this case, the gate voltage is 20 V, and the drain voltage is 15 V. In this figure, the upper temperature distribution is the case that heat transfer coefficient is $10^8$ W/(m²·K), and the lower temperature distribution is the case of $10^5$ W/(m²·K). And, the bottom surface of this figure corresponds to Fig. 2. In this figure, the x axis shows X direction of Fig. 2, and the y axis shows Y direction of Fig. 2. As shown in this figure, the side of the source and the gate electrode ($y = 0$) is high temperature. When the heat transfer coefficient is $10^8$ W/(m²·K), the maximum temperature (the hot spot temperature) is about 497 K, and the bottom temperature of the modeled device is about 303 K. The temperature difference between the hot spot temperature and the bottom temperature is about 194 K. Additionally, when the heat transfer coefficient is $10^5$ W/(m²·K), the hot spot temperature is about 823 K, and the bottom temperature is about 748 K. The temperature difference is 75 K. From this result, when the heat transfer coefficient is higher, the temperature difference between the hot spot and the bottom temperature ($y = 100 \mu m$) is larger. In other words, temperature distribution becomes inhomogeneous, when the cooling performance is higher.

Figure 5 shows the relationship between the bottom temperature of the device and heat transfer coefficient at the bottom surface. In this calculation, gate voltage is 20 V, and drain voltage is 5 – 15 V. In this figure, diamond plot indicate the case that the drain voltage is 5 V, square plot is 10 V, and triangle plot is 15 V. The horizontal axis shows the heat transfer coefficient, and the vertical axis shows...
the bottom temperature of the device. As show in this figure, the bottom temperature becomes lower with increase in the heat transfer coefficient of the bottom surface, and is about 300 K in any drain voltage case when the heat transfer coefficient is more than $5 \times 10^7$ W/(m$^2$·K). Therefore, when the cooling performance at the bottom surface is high, the bottom temperature can be assumed ambient temperature. Additionally, when the heat transfer is $5 \times 10^6$ W/(m$^2$·K), the bottom temperature is lower than 350 K within this calculation condition. However, when the heat transfer coefficient is $10^5$ W/(m$^2$·K), the difference between the bottom temperature of the case of 5 and 15 V in the drain voltage is about 270 K. Hence, the bottom temperature should be changed when the cooling performance is not high, if the constant temperature is assumed as the boundary condition of the device bottom temperature.

Figure 6 shows the variation of the hot spot temperature with a change in the bottom temperature. In this figure, the horizontal axis shows the bottom temperature, and the vertical axis shows the hot spot temperature of the device. The value of the horizontal axis of this figure corresponds to the value of the vertical axis in Fig. 5. The slopes are almost liner, and the hot spot temperature is high when the applied voltage is large. When bottom temperature is about 300 K, the temperature difference between the hot spot temperature in the case of $V_D = 5$ V and 10 V is about 70 K. And, the temperature difference between the hot spot temperature in the case of $V_D = 10$ V and 15 V is about 104 K. Therefore, even when the applied voltage to the drain increases at a regular interval, the temperature rise of the hot spot is not a regular interval, and the ratio of the temperature rise of the hot spot becomes larger with increase in the drain voltage. From this result, the variation of the hot spot temperature with respect to the bottom temperature is confirmed. Therefore, this result indicates the capability of the prediction of the hot spot temperature using the bottom temperature.

8. Conclusion

In this study, we investigate the effect of the cooling performance on the bottom temperature of power Si MOSFET and the effect of the bottom temperature on the temperature distribution of the device using electro-thermal analysis. From these results, the effect of cooling performance on the bottom temperature is large, and high cooling performance is required to cool the device bottom at about 300 K. Additionally, even when the bottom temperature is same, the hot spot temperature is higher with increase in drain voltage. And, when the cooling performance is high, the temperature distribution is non-uniform.

References


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