[Technical Paper]

Reliability Evaluation for Integrated Glass Interposer

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Abstract

In this paper, we investigate reliability testing for a glass interposer. The test vehicle includes a glass interposer with a chip substrate and a bismaleimide triazine (BT) substrate. The structure of a glass interposer with two redistribution layers (RDLs) on the front-side and one RDL on the back-side has been evaluated and developed. Key technologies, including via fabrication, front-side RDL formation, microbumping, temporary bonding, glass thinning, and back-side RDL formation, have been developed and integrated for high performance. The BT substrate design for electrical characterization of reliability tests is reported in this paper. The results indicate that this glass interposer can be effective for the assembly of thin substrates. The data shows the feasibility of this glass interposer for electronics applications.

Keywords: Glass Wafer, Glass Interposer, BT Substrate, Assembly, Reliability

1. Introduction

Through glass via (TGV) interposer fabrication processes are critical techniques in three-dimensional integrated circuit (3D-IC) integration, providing short interconnections among different stacked chips and substrates. Currently, silicon is a mature material in semiconductor technology, but glass, a dielectric material, provides an attractive option because its intrinsic characteristics offer the advantages of electrical isolation, better RF performance, flexibility with CTE, and most importantly, low cost. Numerous papers have demonstrated Si interposers with 2.5D or 3D stacking integration because Si has a CTE match with Si ICs. Furthermore, silicon infrastructure, including foundry wafer processes and the support for Si equipment, is widely available. A silicon interposer is also an effective solution for high pin-count IC applications based on mature Si technologies such as advance via formation and fine line Cu damascene multilevel interconnection processes. However, silicon interposers have several problems that glass interposers do not have: (1) Si is a semiconductor and not a good conductor or insulator; (2) large CTE difference between Cu and Si obstruct through silicon via (TSV) formation processes; (3) silicon is costly due to the need for electrical insulation around the via sidewall; and (4) the wafer size is limited based on the constraints of the silicon industry. Mass production requires

cost reduction; the consensus regarding the cost of ownership is “the cheaper, the better.” Instructive examples of such low aspect ratio applications include CMOS Image Sensors for wafer-level processes.[1–6]

A striking challenge of 3DIC engineering is thermal throttling when multi chips are stacked together. The signal performance is limited by a chip to chip thermal coupling effect. It is a challenge to decrease that coupling effect because chip features are small. One promising solution is to use a substrate with low thermal conductivity, such as glass. Because of the very low thermal conductivity of glass, the equivalent thermal conductivities, k_{xy} and k_z , of a TGV interposer are both much lower than those of a TSV interposer. Simulation work for the thermal characteristics of a glass interposer has been studied extensively in Ref.[7] Comparisons of the electrical designs, simulations, and measurement analyses regarding thermal performance have been studied in Ref. [8] and Ref.[9] This paper considers glass interposer characterization, wafer-level integration, assembly, and fabrication, and also electrical and thermal properties.

2. Experimental

2.1 Prepare of glass interposer

An interposer includes a substrate and two metal layers disposed on the opposite sides of the glass substrate. The

Fig. 1 Assembly module for test vehicle.

interposer (100 μm) is fabricated on a 12" glass substrate. The original thickness for glass substrate is 700 μm and the TGVs are formed directly on a glass wafer by Corning Incorporated. After the Ti barrier and Cu seed layer processes, Cu plating is applied with a bottom-up mechanism to minimize the overburden on the wafer surface. The Cu overburden and Ti barrier are removed by a chemical-mechanical polishing process. For the top redistribution layer (RDL) (line-width/space = 3 $\mu\text{m}/3 \mu\text{m}$), the semiadditive process (SAP) is applied. A polymer-lithographic material is used for passivation, the highest temperature of the curing process is 200°C. Top UBM (22 μm in diameter; 6- μm -thick Cu with electroless PdAu) is formed with a top passivation opening (12 μm). Wafer thinning starts with a temporary bonding with a carrier at the front-side (glue thickness = 60 μm). Grinding/CMP is used to reveal the Cu. The bottom RDL is then formed by Cu plating after lithography patterning. The bottom UBM (85–120 μm in diameter) is formed with a polymer passivation opening of 85–120 μm .

2.2 Assembled with chip, BT substrate

The bismaleimide triazine (BT) substrate design for electrical characterization of reliability test is included in this work. The reliability test vehicle is shown in Fig. 1. We checked the electrical properties of the assembly module step by step; then, we finished the assembly of the chip with a glass interposer and a BT substrate.

3. Result and Discussion

3.1 Fabrication of glass interposer

The glass interposer was composed of 100- μm -thick glass with two RDLs on the front-side and one RDL on the back-side. The major differences between the glass process and the Si interposer process were the methods of via formation and isolation. Glass material is composed with SiO_x , which provides insulation for electrical currents. A polymer-based dielectric layer was used for insulation and

Fig. 2 Top view of glass via.

Fig. 3 (a) Front-side via after Cu overburden has been removed; (b) Back-side via after thinning by grinding/CMP.

Fig. 4 Fine line (L/S = 3 $\mu\text{m}/3 \mu\text{m}$) design on glass.

passivation; the equipment and process for polymer-based dielectric layer isolation were more cost-effective than oxide or nitride inorganic-based isolation. Glass interposers with 30 μm vias of the glass interposer were provided by Corning Incorporated. The diameter of each via was reduced to 25 μm from 30 μm . The performance of the top via was shown in Fig. 2.

Cu overburden and Ti barrier were removed by a CMP process (Fig. 3a). The process used to remove Cu overburden from silicon interposers was used for each glass wafer. The dishing was below 0.5 μm . The polymer material was used for passivation, and the RDL/UBM was formed by an optimal process. Wafer thinning started with the temporary bonding of a carrier to the front-side (adhesive thickness = 60 μm). Grinding/CMP was used to reveal the Cu and was shown in Fig. 3b. Because the glass has favorable isolation, the Cu revealing and glass thinning processes were applied directly with a grinder. The dishing was also below 0.5 μm .

Figure 4 shows the fine line design (L/S = 3 $\mu\text{m}/3 \mu\text{m}$) on the glass; the thickness of Cu was 1 μm . After the wet process of Ti/Cu barrier/seed layer etching, no metal residue was found between the Cu traces. A photograph of the interposer, taken using an optical microscope, is shown in

Fig. 5 Optical microscope photo of glass interposer.

Fig. 6 Photo for (a) single glass interposer and (b) 12" glass interposer after debonding and dicing.

Fig. 5; the back-side pads of glass interposer are clearly visible from the front-side. A real interposer with two RDLs on the front-side is shown in Fig. 6.

3.2 Assembly of chip-to-glass interposer on organic substrate

The chip was stacked on the BT substrate by a two-step assembly process. The first step was the joining of the glass interposer and substrate by a reflow process. Assembly of the glass interposer on the substrate was conducted in a five-zone reflow oven. The glass interposer with flux dipping was properly aligned onto the substrate and subsequently reflowed for soldering. The reflow profile had a peak temperature of 245°C and a dwell time of 60 seconds above liquids; this ensured that the soldering between glass interposer and substrate would meet quality criteria.

Once the glass interposer module was completed on the BT substrate, the second step consisted of microbump soldering between chip and glass interposer by a flux-enhanced thermocompression bonding process. The lower thermal budget for the thermocompression bonding process was applied to the microjoints between the chip and the glass interposer. The usage of flux was very important in this stage. Water-soluble flux was applied. Because solder bumps and microbumps had been fabricated onto the back-side and front-side of the glass interposer respectively, the microbumps were reflowed for a short time and an oxidation layer formed on those microbumps. Therefore, to construct interconnections between the chip and glass interposer, thermocompression bonding with flux

Fig. 7 Assembled substrate module and its X-ray image.

Fig. 8 Cross-sectional views of microstructures of microbump joints and TGVs.

was required. Cross-sectional analysis of the microstructures of the chip-stack substrate module was conducted to determine bonding conditions. Bonding conditions of 250°C/10 sec under gap-height control mode were used.

Figure 7 shows the real assembled substrate module and an X-ray image of its solder-bump joints and microbump joints, which have different pitch values. Figure 7 shows that the edge solder-bump joints and microbump joints were correctly aligned, which was necessary for the success of this two-step chip-stack substrate module assembly process.

Figure 8 shows cross-sectional images of the chip-stack, the BT substrate, and the microstructures of the solder joints. These images show that the microbump interconnections were joined securely even though voids existed within the microjoints. As can be seen from these images, 100- μm -pitch and 150- μm -pitch interconnects were aligned and joined properly. These photographs confirm that flux-enhanced thermocompression bonding produced high-quality microbump joining. The contact resistance levels of the microjoints were measured on the glass interposer module. Figure 9 shows a plot of contact resistance distributions obtained by measuring various sets of microjoints. Spots with 150 μm bump pitch on the glass interposer were connected with 26 I/O bumps, TGV, 2 RDL on the front-side and 1 RDL on the back-side; spots with 100 μm bump pitch on the glass interposer were connected with 38 I/O bumps, TGV, 2 RDL on the front-side, and 1 RDL on the back-side. The measured contact resistance of the

Fig. 9 Plot of contact resistance distribution obtained by measuring various sets of microjoints. Spots with 150 μm and 100 μm bump pitch on the glass interposer were connected with 26 I/O and 38 I/O bumps, respectively.

Fig. 10 Cross-sectional view of glass interposer after TCT test.

microjoints included the resistance of the metal traces. Figure 9 shows measurements of contact resistance levels between chip, glass interposer, and BT substrate. The resistance of a daisy chain for 150 μm bump pitch with TGV was approximately 10 Ω ; for 100 μm pitch with TGV was approximately 16 Ω . The large difference of contact resistance for a 100 μm pitch was caused by a small number of joint defects that arose during the assembly process. This difference can be optimized by controlling the assembly procedure.

3.3 Reliability test

The reliability levels of the glass interposer were assessed by Thermal Cycling Test (TCT). The TCT conditions for each cycle were $-55^{\circ}\text{C} - 125^{\circ}\text{C}$; Dwell time = 5 min; Ramp rate = $15^{\circ}\text{C}/\text{min}$. With optical microscopic observation and cross-sectional analysis from scanning electron microscopy (SEM), no cracks or delamination were found in any interface of the glass interposer (Fig. 10) during TCT testing (of up to 2,000 cycles). For the assembled module that of the glass interposer with chip, and BT assembled by thermocompression bonding (TCB), the relevant testing is still ongoing.

4. Conclusion

A wafer-level 300 mm glass interposer scheme with top-side RDL, Cu TGVs, back-side RDL, Cu/Sn microbumps, and polymer passivation has been implemented. A device has been assembled with a chip and BT substrate.

1. In this investigation, an optimized process was applied for the glass interposer. A polymer-based dielectric material was used for passivation. The top diameter of TGV was 25 μm . Cu overburden and Ti barrier were removed by a CMP process.
2. A top UBM (22 μm in diameter; 6- μm -thick Cu with electroless PdAu) was formed with a top passivation opening (12 μm). The structure was analyzed and investigated by SEM analysis.

For a reliability test vehicle, the glass interposer was assembled with a chip, and a BT substrate. The bonding process was optimized and properly connected solder microbump joints can be formed between chip, glass interposer, and BT substrate. The average resistance of a daisy chain for 150 μm bump pitch with TGV was about 10 Ω ; for 100 μm pitch with TGV was approximately 16 Ω .

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