HIGH SPEED ON-LINE COUNTERS AND ANALOG TO DIGITAL CONVERTERS FOR NEUROPHYSIOLOGICAL DATA PROCESSING

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In the fields of neurophysiology it is a routine necessity to process a great amount of data, such as impulse trains and electroencephalogram (EEG) waveforms. Spike trains analysis (RODIECK *et al.*¹⁾ 1962, PERKEL *et al.*²⁾ 1967, NAKAHAMA *et al.*³⁾ 1968) is the most typical case. Often thousands of interspike intervals are dealt with. Therefore, the first necessary step in analysis is the digitization of interspike intervals (GLASER⁴⁾ 1962).

Recent laboratory digital computers (CLARK *et al.*⁵⁾ 1965) employ many analog input and output devices: analog to digital (A-D) and digital to analog (D-A) converters, CRO displays, relay circuits for controlling external apparatus, and so on. However, very few of these computers can, with satisfactory accuracy, count interspike intervals from several input channels in real time. This is because they do not have high speed electronic counters directly coupled to them. It is for this reason that high speed on-line counters have been constructed in our laboratory. They are connected to a digital computer with a minimum of modification of the input systems of the computer.

ORGANIZATION OF COMPUTER

New input devices have been attached to a standard type of small scale general-purpose computer (JRA-5). Briefly, the computer is a one-address, fixed word length, serial machine using a word length of 16-bits. Cycle time of the 4096-word random address magnetic core memory is 10 μ s. It carries a 8192-word magnetic drum memory as an external memory as shown in FIG.

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FIG. 1. Block diagram of the system. This system consists of a small scale general-purpose computer and specially designed analog input devices for processing impulse trains and analog waveforms.

1. It also employs a photo-tape reader and a tape punch which are the digital input and output devices. All analog data are converted to 8-bits or 16-bits binary numbers which are punched out and preserved on paper tape.

SPECIFICATION OF COUNTERS

Major points which were especially considered for the design of the on-line counters were as follows:

- 1) A maximum clock frequency of 100 kHz was chosen so that a counting accuracy of 1% should be guaranteed for measuring an interspike interval of 1 ms.
- 2) Dead-time of counting is much less than about 1 ms, which is considered to be the shortest limit of the interspike intervals.
- 3) In neuronal activity the interspike intervals often range from 1 ms to several tens of seconds. Therefore there is a possibility of miscounting the long interspike intervals due to overflow of the counter. To avoid this, overflow signals from the counters are transferred to the core memory of the computer.
- 4) To process two impulse trains and two analog waveforms such as EEGs at the same time, two input counter channels and two input A-D converter channels function in parallel with each other.

CIRCUIT BLOCK DIAGRAM

FIG. 1 shows the block diagram of the overall system. As is shown in the block surrounded by chain lines, 2 channels of A-D converter and 2 channels of electronic counter are connected to the computer as analog input devices. All information in the counters and A-D converters are stored temporarily in 3 registers so as to process signals which are arriving simultaneously. Thereafter they are transferred into the core memory through the arithmetic register. As each A-D converter has 8 bits full scale, the analog information of two channels is coded into a word of 16 bits length in the register following the A-D conversions.

FIG. 2 shows the detailed block diagram of the part surrounded by chain lines in FIG. 1. This part is divided into 3 portions, each separated by chain lines: 2 channels of A-D and D-A converters, 2 channels of counters and the channel control unit. The channel control unit shown in the lowest portion in FIG. 2 selects the channel whose information is to be transferred to the arithmetic register of the computer. This unit consists of flip-flops (FF) and gate circuits (G).

When a signal from clock pulse generator reaches an A-D converter, an A-D conversion is made and the value is sent to the A-D register. When a signal (or an impulse) reaches the input of the counter channel A or B with the closing of a switch, SW 1A or SW 1B, the content of the counter A or B is sent to register A or B, respectively. At the same time, one of the flip-flops which are indicated in FIG. 2 as FF(b), FF(e) and FF(h) is transiently brought to the "set" state via several flip-flops and gate circuits. Thus the input information corresponding to the flip-flop FF(b), FF(e) or FF(h) is led to the arithmetic register from the corresponding register through a switch SW 2AD, SW 2A or SW 2B. The computer then starts to process the information in the arithmetic register. During this period the gates G3, G4 and G5 are all closed until the computer returns to the "stand-by" state. When another "start" signal occurs, the corresponding flip-flop FF(a), FF(d) or FF(g) is set until gates G3, G4 and G5 open. When these gates open, the corresponding flip-flop, FF(b), FF(e) or FF(h) is transiently set, permitting the input information to pass to the arithmetic register. When two or three signals arrive simultaneously, gates G1 and G2 determine which information of the channels is to be processed preferentially. It should be noted that all the flip-flops transmit a signal to the following stage every time they are set, being brought back to the reset state by the signal fed back from the following stage.

To process the information in the arithmetic register, the control circuits of the computer are driven by the "start-stand-by" register, and the next step of the program then proceeds. The program step is determined by the

FIG. 2. Block diagram of the analog input device. This consists of 2 channels of A-D and D-A converter, 2 channels of counter, and the control units.

content of the instruction counter of the computer, which is modified by a jump pulse. This pulse is generated by the output of flip-flop FF(b), FF(e) or FF(h), according to the sequence of processing information in the channels.

In the case of A-D conversion channels only one flip-flop, FF(a), is sufficient for retaining a signal temporarily. This is due to the fact that the analog input information is processed at a constant sampling interval determined by the clock pulse. There is no need to be concerned here with

unexpected time intervals. In the instrument described in this paper, the minimum sampling interval is set to be 1 ms, and 50 instructions can be executed during this interval. However, it is possible to reduce the sampling interval, if the number of the instructions is diminished.

In connection with the hardware modification of the computer, a new special instruction is prepared. It makes it possible to process the information in the appropriate channel according to a priority assignment. This new instruction consists of four words. The first sends information to the arithmetic register. The second, third and fourth involve the information processing of the A-D converter, counter A and counter B, respectively, specifying the jump address to which the program proceeds.

Each counter circuit, A or B, is made of 16 transistorized flip-flops. An "overflow flip-flop" is employed in each channel, as shown in FIG. 2, to check an overflow signal from the most significant bit of the counter. Every time the counter overflows, the flip-flop is set. This overflow signal is processed in almost the same way as the input signal. At the moment the flip-flop is set, the content of the counter is "zero". Accordingly, this "zero" is transferred to register A or B. When there is no overflow signal, the least significant bit of the register is always set to the "1" state. Thus, only when an overflow occurs, there is a "zero" in the counter.

FF(c) and FF(f) play a role when an overflow signal is being processed. These flip-flops retain any input signal which may arrive immediately after the overflow. When the overflow signal is transmitted to FF(e) and FF(h), FF(d) and FF(g) are reset. Thereafter the signal retained in FF(c) and FF(f), is sent to FF(d) and FF(g).

Clock pulses to be counted are generated from the computer clock. The clock frequency is variable from 100 kHz to 1 Hz. Input signals of the spike trains are reshaped by double slicers. This circuit can reject artifacts and signals of too large or too small an amplitude.

The A-D conversion circuits are not special and operate on the principle of successive approximation. They are made of integrated NAND elements. Tunnel diodes serve as components of the comparator. The conversion time is 4 μ s. This makes it possible to execute an A-D conversion within the cycle time of this computer (10 μ s). The D-A converter is designed as an element of the A-D converters.

EXAMPLES OF APPLICATION

With the use of on-line counters, A-D converters and their parent computer, several programs have been written for on-line data processing. Some examples are shown below.

A. On-line Processing of Spontaneous Impulse Trains and EEG Signals

1) *Digitization of Impulse Train.* Spontaneous discharges have long been a matter of interests to neurophysiologists. To analyze them it is important to select the sections of data in a long run which are to be digitized. In some cases, it is necessary to choose the sections recorded during the times that the general state of the brain is stationary (NAKAHAMA *et al.*⁶⁾ 1966). For this purpose a monitor of EEG recordings is needed. According to whether EEG recordings show low voltage fast wave activity or high voltage slow wave activity, spike trains are to be separately analyzed. To do this, the flow chart as indicated in FIG. 3 is programmed. The flow chart is also designed to stop the counting operation when, spike amplitude becomes low compared with noise level, mis-triggers arise in the waveform reshaping circuits, or the base line is fluctuating.

FIG. 3. Flow chart for the digitization of an impulse train. In this program, the state of EEG recording and the slicing level of the spike train are monitored.

To execute the program of the flow chart in FIG. 3, our counters are used as follows. A spike train is led to counter A. Counter B simultaneously checks the zero-crossing time intervals of the EEG (RICE⁷⁾ 1945) to detect their

changes in real time. The frequency component of EEG is roughly evaluated by calculating the zero-crossing rates in the fixed running time intervals (usually 3-10 s). To detect a mis-trigger and base line fluctuation, 2 channels of A-D converter are used: one is for the conversion of the voltage of slicing level, and the other is for the base line in the spike train. The two of these voltages are continuously compared at every 2 ms. So long as the slicing level is higher in voltage than the base line of a spike train, the computer is permitted to continue digitizing the interspike intervals. On the contrary, when the base line continually exceeds the slicing level, the computer stops the counting operation. Since there are less than 50 program steps for the execution of one loop of the flow chart in FIG. 3, dead time to count an interspike interval is not more than 1 ms.

FIG. 4. Punched out result of interspike intervals. Each interval is digitized into a word length of 16 bits, and is punched out with 4 characters on paper tape. The number of overflow signals is shown by that of "zero".

FIG. 4 shows an example of the punched out results of the counted interspike intervals. Each interval is quantized with 16 bits and is represented by 4 characters on the paper tape. An overflow is indicated by a "zero".

2) *Simultaneous A-D Conversion of EEG and Spike Frequency.* To investigate the cross-correlation between EEG and a spike train (FROST *et al.*⁹⁾ 1966), it is necessary to quantize the spike frequency in a fixed time interval rather than the interspike interval itself. When the on-line counter is used in a gating mode, spike frequencies are measured instead of interspike intervals. In 1 word of memory is stored each digitized value of two kinds of information: the upper 8 bits are for EEG, and the lower 8 bits for spike frequencies.

B. Calculation of Spike to Spike Correlation and Spike to Continuous Wave Correlation

1) *Spike to Spike Correlation.* Simplified calculation of correlation function (PERKEL *et al.*⁹⁾ 1967, DE BOER *et al.*¹⁰⁾ 1968) between 2 impulse trains were made possible with the use of 2 channels counters. The principle of the program is shown in FIG. 5.

FIG. 5. Illustration of the program for calculating pulse to pulse correlation. The correlation histogram is computed by using 2 channels on-line counter.

Successive interspike intervals in A channel are continuously stored in a ring memory of the working space until a spike in B channel interrupts the store. After this interruption, a "one" is successively added to the corresponding bin in the memory to an interval between the time when a spike enters into B channel and the time when successive spikes appear in A channel. This operation stops when the interval exceeds a fixed value. Thereafter a similar operation mentioned above is performed for the intervals stored in the ring memory before. After finishing these processes, the computer returns to the initial state of storing intervals into the ring memory and again waits for a spike in B channel. Repeating these processes many times, the cross-correlation histogram between the two trains in A and B channels is computed. An example of the results is given in FIG. 6(a). It should be noticed that a spike other than the first spikes in B channel are ineffective during one cycle of the operation and that, therefore, the computed function might be slightly different from the "exact" correlation function.

FIG. 6(b) shows an example of the calculations in which the pulses in B channel are synchronized with the onset of regularly presented stimuli and the impulses in A channel are the responses evoked by the stimuli. As is clear in this figure, the calculation gives a pre- and post-stimulus time histogram (PSTH).

In the execution of the program mentioned above, a working space of 256 words is used for the ring memory, and that of 2048 words for the bins in memory of the PSTH. In the case of 20 kHz clock, the bin width becomes 50 μ s. Therefore, the length of pre-stimulus time histogram becomes 12.8 ms; and that of post-stimulus time histogram is 89.6 ms. Thus a PSTH of high

FIG. 6. Some examples of the results obtained in cat with the on-line counters and A-D converters.

(a) A cross-correlation histogram between unit discharges of a cell in midbrain reticular formation (MRF) and those in the pulvinar nucleus (Pul). These unit discharges are simultaneously recorded from MRF and Pul. The channel A of counters is for unit discharges in MRF and B for those in Pul. Bin width is 50 μ s. Recycle of accumulation is 776. Total points in abscissa is 1024.

(b) A pre- and post-stimulus time histogram. It is obtained from the unit discharges of a single neuron in the lateral geniculate body induced by the stimuli of light spot (100 ms in duration) to the receptive field of the retina. Bin width is 4 ms. Recycle of accumulation is 21. Total points of abscissa is 1024.

(c) A cross-correlation function between spike discharge and EEG. It is obtained from an impulse train of a cell in the suprasylvian gyrus of the cerebral cortex and from EEG recorded from this area. A sampling interval of EEG is 2 ms. Recycle of accumulation is 100. Total points of abscissa is 512.

accuracy is obtained.

2) *Correlation Between Spike and Continuous Waves.* A cross-correlation function between continuous wave such as EEG and a spike train is computed by using an A-D converter and the B channel counter. For this computation, spikes in B channel are used for triggers and the digitized values from continuous waves are accumulated into the bin in memory as mentioned in B 1). An example of the results is given in FIG. 6(c). When 2 channels of A-D converters are used, 2 different continuous waves are processed at the same time. Thus 2 correlation functions are obtained.

SUMMARY

A digital computer input device has been developed for processing neurophysiological data in real time. It consists of two high speed electronic counters and two A-D converters. They make it possible to deal simultaneously with four different signals. Some examples of the application of this apparatus have been presented: a program for the high speed digitization of interspike intervals, simultaneous analog to digital conversion of EEG and spike frequency, cross-correlation functions between 2 spike trains and between the EEG and a spike train, finally, pre- and post-stimulus time histograms.

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