Mechanical Problems in the Production Process of Semiconductor Devices*

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Mechanical problems of semiconductor devices are reviewed. The emphasis is placed on the problems relating to deformation and strength of the device component, which are incurred in the production process. The case examples describe single crystal growth, wafer processing, wafer bonding, interconnections and packaging. Thermal stress due to different thermal expansion among the materials which constitute devices plays an important part in the deformation and strength of the devices. The object of the problems is a miniature and multi-thin-layered material system which consists of different materials. Phase transition from liquid to solid often occurs in the constituent materials during device processing. Mechanical stress is mainly induced by temperature change in the manufacturing and operating processes. Interfacial strength among bonded dissimilar materials is crucial to device reliability. In conclusion, the characteristic factors common to the mechanical problems are summarized.

Key Words : Semiconductor Device, Deformation, Strength, Crystal Growth, Wafer, Deposition, Interconnection, Bonding, Package, Quality Test

1. Introduction

Semiconductor devices are widely used in many kinds of electronic equipment. High device reliability is expected because of their sophisticated applications. The semiconductor device consists of a chip with integrated circuit, substrate, interconnections and packaging. The chip is mounted on the substrate and the interconnections made between the integrated circuit and the external electrodes. After the process, the chip is packaged and is then usable as an electronic device.

The reliability of a semiconductor device is closely related to the mechanical properties of the constituent materials. This means that the deformation and strength of the material used in the device significantly affect device performance and function.

Crystal defect and internal stress in the chip accelerate the device degradation. Low bonding strength between interconnections shortens the device life. Improper packaging damages the chip and the interconnections. These are purely mechanical problems concerning deformation and strength of materials; solutions are essential for the high reliability of electronic devices.

The semiconductor device is an interesting object for mechanical problems. The device is made of various kinds of materials such as ceramics, metals and polymers. The structure is sophisticated in its geometrical configuration and material constitution. There are complex material interfaces in the device. Even simple load produces complex deformation of the device due to the coupling effect of dissimilar materials.

This article describes some typical mechanical problems in semiconductor devices, which are related to the deformation and strength of the constituent materials. The examples are explained by using the problems which arise in the production process as well

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as the operational process. The features common to the problems are examined to obtain guidelines for device design.

2. Production Process of Semiconductor Devices

The production process of semiconductor devices begins with the single crystal growth and ends with the estimation of device quality. The process consists of the following stages as schematically illustrated in Fig. 1⁽¹⁾.

(1) Preparation of wafers

An ingot of silicon single crystal is obtained from silicon polycrystal through the melting process. Thin layers of silicon single crystal are cut from the ingot. The cut layers are finished into wafers by polishing processes.

(2) Processing of wafers

Thin film layers are deposited on the wafer surface and electronic circuit patterns are integrated by the photochemical process. The chips for the device are completed.

(3) Assembling of device

The chips are bonded to their base plates and the bumps of the chips are connected to the outer electrodes. The chips become electron components.

(4) Packaging of device

The chips are encapsulated by resin or metal containers. They protect the chips from external force or thermal shock.

(5) Quality estimation

The complete devices are subjected to mechanical loads under various environmental conditions. The reliability of the device is confirmed.

The production process of semiconductor devices contains various kinds of mechanical treatment as well as thermal and chemical treatment. The mechanical problems relating with deformation and strength

of devices occur in the process.

3. Preparation of Wafers

3.1 Growth of single crystal

In many electron devices, silicon wafers are used. Silicon wafers are made from an ingot of silicon single crystal which is grown from melting silicon polycrystal. There are two kinds of methods for the growth of silicon single crystal. The schematic figures of the methods, denoted as the floating zone method and Czochralski method, are illustrated in Fig. 2. In the floating zone method of Fig. 2(a), the ends of the feed and seed rod of silicon crystals are drawn close and melted by heating. A melting zone is formed between the rods of single crystal and polycrystal. The single crystal is grown by transferring the melting zone. The method is used for the growth of single crystal of small diameter, because the floating zone is maintained by the surface tension of the silicon liquid. The principle of the pulling of single crystals by Czochralski method is shown in Fig. 2(b). A melting silicon of polycrystal is held in a crucible and a seed crystal dipped into the melt. Then the single crystal slowly withdrawn vertically to the melt surface. The single crystal is grown by the seed crystal. The ingot diameter obtained by this method is currently from 160 mm to 200 mm.

In both methods, the phase transition from liquid state to solid state occurs. The mechanical properties of the silicon are significantly affected by the crystallizing process. During the growth of crystal from the melt, the temperature distribution creates thermal stresses in the crystallized ingot. The thermal stresses cause the propagation and multiplication of dislocations in the crystals. The dislocation growth reduces the life time or increases the degradation rate of devices.

Fig. 1 Production process of semiconductor devices

Fig. 2 Principles of single crystal growth

Fig. 4 Temperature (a) and stress distribution (b) in growing GaAs crystal

Fig. 3 Temperature distribution in growing Si crystal

Figure 3⁽³⁾ shows the temperature distribution in a growth crystal of silicon single crystal 80 mm long with a diameter of 80 mm. The results are calculated by the finite element method. The largest temperature gradients occur near the root of the crystal. The axial temperature gradients are appreciably larger than the radial gradients.

Figure 4⁽⁴⁾ represents the temperature and stress

distributions in the ingot of GaAs crystals which is drawn from the melt. The diameter and length are 50 mm and 100 mm, respectively. The stress is indicated by the equivalent stress values. The large temperature gradient occurs near the root of the ingot. The maximum stresses are reached near the surface of the ingot root. This corresponds to the position of the steepest temperature gradient.

3.2 Production of wafers

The wafers are made from thin layers which are cut from an ingot of single crystal. The thickness is about 0.7 mm and the diameter depends on the ingot diameter. The thin layers of silicon crystal are cut by a slicing machine. Diamond blade, band saw and wire saw are used for slicing. The diamond saw is commonly used to cut large silicon ingots. A strained surface layer remains on the surface of silicon layers after the cutting process. After cutting the thin layers, rapping processes are adopted to reduce the strained surface layer and to finish the thickness and surface conditions, and then the wafers are polished. The polished wafers are again subjected to a micro-polishing process to finish the flatness and thickness precisely; mirror wafers are completed.

The bow in wafers occurs during the cutting and polishing process. Figure 5⁽⁵⁾ shows the example of the wafer bow. The patterns of the electronic circuit are integrated on the wafer surface by photochemical processes repeatedly and patterns are formed in

multilayers of thin films. The wafer bow causes the mismatching of circuit patterns. The bow has significant effects on the yield of chips. To obtain a high yield of chips, the bow must be as small as possible. The bow of a circular wafer is related to the radius of curvature of the wafer under the assumption of uniform curvature, as shown in Fig. 6⁽⁶⁾. The relations among those magnitudes are illustrated in Fig. 7⁽⁶⁾. The radius of curvature $R=100$ m is necessary to get less than the bow of $1\text{ }\mu\text{m}$ for the wafer diameter of 150mm .

4. Processing of Wafers

The patterns of electronic circuit are integrated on the mirror surface. The process consists of ion sputtering, thin film deposition and electronic circuit etching. The wafer is repeatedly subjected to thermal cycles between high temperature and room temperature. The bow of wafers is increased by the thermal cycles. When a row of regularly spaced circular wafers is quickly brought out of a high-temperature furnace into a room-temperature state, a drastic radial temperature variation is induced in each wafer. This produces a different temperature gradient in the radial direction according to the spacing distance and the velocity at which the wafers are brought out. Figure 8⁽⁶⁾ gives an example of the temperature gradients in wafers of the front and middle of row, when the row of processing wafers is brought out of the furnace. The temperature gradient is larger in the front wafer than in the middle wafer due to the different cooling rate. The thermal stresses are

Fig. 5 Bow and warpage of silicon wafers

Fig. 6 Magnitude of bow with uniform radius of curvature

produced by the temperature gradient. Figure 9⁽⁷⁾ shows the thermal stresses in the radial and circumferential direction of a circular wafer during the cooling process of an infinite row of wafers. The stress values are given by nondimensional forms. The stresses are zero just after the wafer row is brought out and they increase to the maximum values with time duration. The stresses are not produced under uniform temperature condition. The maximum of the circumferential stress occurs at the rim of the wafer, while the maximum of the radial stress occurs at the center of the wafer. It is also noted that the circumferential stress is equal to the radial stress at the center of the wafer.

Silicone-oxidized (SiO_2) glass film is used on the substrate of the device as insulating film in an integrated circuit. The chemically deposited film has internal stress which causes the cracking or debonding of the film. The film has viscoelastic properties

Fig. 7 Relation among bow magnitude, wafer diameter and radius of curvature

Fig. 8 Temperature distribution within wafers in wafer stock

and the values are changed by the heat treatment as seen in Fig. 10⁽⁸⁾. The internal stress in the film of SiO₂ on a silicon substrate reduces according to the temperature of heat treatment.

A substrate deposited by thin films is deformed by the internal stresses of the films and, in the substrate, the internal stresses are also produced. Figure 11⁽⁹⁾ represents a model of a substrate deposited by thin film of square shape. Points D, E, F and G are the midpoints of edges OL, LM, MN, and NO of the rectangle OLMN, respectively. The film dimension is 3×3 mm square and tensile edge forces are applied to the film. The film deformation produces the internal stresses in the substrate. Figure 12⁽⁹⁾ shows the stress distribution in the substrate which is illustrated by the lines of equistress contours. The stress concentration occurs at the edge of the film and affects the substrate to a great depth.

5. Assembly Devices

The wafers deposited by integrated circuits are scribed into each chip. A chip is mounted on a substrate by bonding. Then the bumps of the chip are connected to the outer electrode of the substrate.

5.1 Wafer scribing

The wafers with integrated circuits are scribed by mechanical or chemical processing, in which a diamond point scribe, a laser scribe and a diamond blade are used. The scribing process induces residual

stresses in the chip. The stress affects the electrical properties of the chip. The scribing by diamond blade saw results in the smallest residual stress. Removal of the layer damaged by scribing and annealing of the scribed chip reduce the residual stress⁽¹⁰⁾.

Fig. 10 Effects of heat treatment on stress in SiO₂ film

Fig. 11 Model of a rectangular film deposited on a substrate

Fig. 9 Distributions of radial and circumferential stresses in a cooling wafer

Fig. 12 Equistress contours due to deposited film

5.2 Die bonding

A separated chip is bonded on a substrate by adhesive resin, Au-Si eutectic or Pb-Sn solder. The bonding induces the internal stress in the chip and substrate due to the solidification of the bonding material and the thermal mismatch between chip and substrate. Figure 13⁽¹¹⁾ shows the internal stress distribution of a silicon chip bonded to a Kovar frame. The chip becomes upward convex after bonding. Sufficient bonding strength is necessary to bear the deformation. The defects in a chip cause cracking or delamination of the chip, as shown in Fig. 14⁽¹²⁾. The effects of die length and adhesive thickness on thermal stresses in the chip are illustrated in Fig. 15⁽¹²⁾. The stress is proportional to the ratio L/x . As the die length increases, a corresponding increase in adhesive thickness prevents stress increase. The dotted lines of Fig. 15 correspond to the stresses predicted to initiate fracture in the die with scratches 1, 2 and 4 μm in depth. The results are calculated by using a fracture criterion based on the fracture toughness of silicon. The criterion is a function of the depth of the scratches or other flaws on the surface of the chip.

5.3 Chip interconnections

There are four main methods for the interconnections between the integrated circuit of a chip and the external circuit of a substrate. The principles of the method are illustrated in Fig. 16⁽¹³⁾. The connecting strength between the terminals of the circuits is important for the reliability of devices.

5.3.1 Wire bonding The metallized pads on the surface of the chip are connected to the circuit terminal on a substrate by aluminum or gold wire with a diameter of about 25 μm . The connections are made by ultrasonic thermocompression or thermosonic welding. There are two techniques for wire bonding, which are wedge bonding and ball bonding. The principle of wedge bonding is shown in Fig. 17 (a)⁽¹⁴⁾. A wire is flattened by a wedge-shaped tool and welded under the tool face by ultrasonic thermocompression. The heavy thermocompression gives a wide welded area as well as flattened thin wire. The connecting strength is dominated by the delaminating

Fig. 13 Stress distribution in a die after mounting on a frame

strength at the welded part or the breaking strength at the flattened wire. Figure 18⁽¹⁵⁾ represents the relation between the strength of wedge bonding and welded width. An aluminum wire 25 μm in diameter is welded on a silicone-oxidized layer coated by aluminum film. Tensile load is applied to the wire in the direction of 30° with respect to the welded surface. It is found that there is an optimum welded width where the connecting strength has the maximum.

In ball bonding, a ball forms on the end of the wire by a hydrogen flame or by a spark discharge. This ball is then ultrasonically or hot pressure welded to the pad on the silicone chip using a capillary bonding tool. The procedure is illustrated in Fig. 17 (b)⁽¹⁴⁾. The shear strength against the ball deformation is shown for different wires in Fig. 19⁽¹⁶⁾. The balls are ultrasonically bonded to the aluminum electrodes by varying the ball strain defined by the value in the inserted figure. The shear strength is examined by the shear test using a knife edge. The bonding strength increases for every wire and changes significantly

Fig. 14 Thermal deformation of die and frame

Fig. 15 Effect of die length and adhesive thickness on thermal stress, and flaw length on initial failure stress

with wire materials.

5.3.2 Flip chips This is a direct connecting method of wire bonding. The connection by flip chips is achieved by bonding the device to the external circuit through connection bumps plated on to the pads of the silicon circuit or the substrate circuitry. The number of intermediary bonds is reduced and all device connections are made simultaneously. The thermal expansion of the chip and the substrate differs according to temperature change. This causes the stresses in the soldered joints. The thermal cycles produce the stress cycles to the joints and the fracture occurs in the joints. Figure 20⁽¹⁷⁾ shows the strain distributions in soldered joints with different solder shape under temperature change. The strains are indicated by equivalent values. The maximum strain

Fig. 16 Principles of various silicon chip interconnection methods

is produced at the joint root for both cases of different solder shapes. The maximum strain value depends on the solder shape. Convex soldering is more effective in reducing the strain than concave soldering.

5.3.3 Beam lead chip In beam chips, the leads of the beam shape are plated on the chip. The lead is about 150 μm long, 50 μm wide and 12 μm thick. The

Fig. 17 Principles of wire bonding

Fig. 18 Effects of welded width of wedged wire on bonding strength

Fig. 19 Effects of ball strain on bonding shear strength

Fig. 20 Distributions of effective strain in soldered joint

Fig. 21 Plastic regions in beam lead

leads are welded on the circuit of the substrate by thermocompression. When the beam lead chip is subjected to thermal cycle, thermal stress is produced in the leads. The beam leads are plastically and elastically deformed in a sophisticated manner due to the curvature by the thermal stress. The initial failure occurs at the beam anchors or at the thermocompression bonds. The regions of plastic deformation of a gold beam lead are illustrated in Fig. 21⁽¹⁸⁾. The lead is about 0.5 mils thick and 3 mils wide. The free beam length is about 4 mils. The plastic strain occurs in three distinct parts of the beam lead. One region is at the center and a second is at the heel of the lead bond; the third plastic region is near the middle of the beam. During the temperature cycle of the device, the cyclic plastic strain occurs in the plastic region of the beam lead. The magnitude of cyclic strain depends on the mechanical properties of the beam lead which is changed by annealing. Figure 22⁽¹⁸⁾ shows that the plastic strain occurs at the outer beam lead fibers in the three plastic strained regions, when the temperature cycles rise above the annealing temperature of

the beam lead.

5.3.4 Tape automated bonding The interconnection in tape automated bonding is achieved by an intermediary tape with a suitable pattern for an electric circuit etched from a clad metal film. The etched pattern is matched to the bonding pads on the chip surface and the substrate circuitry. The tape is attached at both ends by solder or hot pressure bonding. Connection pillars are used to ensure bonding at all sites around the chip. The hot pressure for bonding produces mechanical stresses as well as thermal stresses in the connected bumps. The stress can fracture the bumps and the substrate. The bump dimension and material constitution affect the stress distribution in the bump and substrate. Figure 23⁽¹⁹⁾ is a schematic figure of an interconnection by the tape automated bonding. The thermal stresses for the two bumps of different shapes are illustrated in Fig. 24⁽¹⁹⁾. The results show the distribution of the maximum and minimum principal stresses after 10 μ s when the bump is heated to 350°C. The large stress concentration is

produced at the bump root of the type A. In the type B, the stress concentration is reduced by the stepped configuration bump.

5.4 Packaging

The chip bonded with a substrate is sealed in a package for ease of handling and to afford protection from external force or thermal shock. The packaging process is achieved by packing a device in a small container or by coating a device with resin as shown in Figs. 25 and 27; they are denoted as hermetic sealing and plastic packaging, respectively. The container used in hermetic sealing consists of lid and base which are made of metal and ceramic. The seal is excellent in terms of gas tightness. Plastic packaging is widely used for high productivity. With increasing circuit density, small packages are in great demand.

5.4.1 Hermetic seal Figure 25⁽²⁰⁾ shows a model of a hermetic seal. Annular glass-to-metal seals are used in microelectronic devices to hermetically seal the internal components which are connected to the outside through electrical leads. The bond at the interface between the glass and the metal is made through the interpenetration of the glass into a layer of intergranular metal oxide. The resistance of this interface to thermal shock is critical since any failure leads to loss of hermeticity, which in turn causes failure of the internal components. The seal is

Fig. 22 Schematic figures of cyclic plastic strain induced by thermal cycles

Fig. 23 Schematic figure of material constitution in bump

modeled by considering one lead, one glass annulus and an annular portion of the base material.

The seal is subjected to a thermal shock which consists of heating the seal from room temperature to 400°C and suddenly immersing it in a fluid at room temperature. The radial stresses in the seal under the thermal shock are illustrated as a function of time in Fig. 26⁽²⁰⁾. The stress and time are indicated by non-dimensional values, respectively. It is found that small initial residual stresses develop, followed by large transient maximum stresses. The largest transient radial stress occurs at the upper surface of the glass where large temperature gradients exist. A comparison of the radial stresses at midheight of the glass-base and lead-glass interfaces shows that the maximum stress at the lead-glass interface is much larger than that at the glass interface. The failure in the seal usually occurs by separation of the interface between the glass and the lead.

5.4.2 Plastic packaging Encapsulation of a chip in resin is widely used for plastic packaging. The encapsulated resin suffers heat cycles both in molding and operating processes. The temperature change in

Fig. 24 Distributions of thermal stresses in bumps with different shapes

Fig. 25 Schematic figure of hermetic seal

the process creates internal stresses in an encapsulated device due to different thermal expansion between resin and chip. Shrinkage of packaging resin also produces internal stresses. The stress causes cracking in molded resin, delamination in the interface between resin and chip, and breakage of the interconnected wire bonding.

A cross section of a device encapsulated by resin is shown in Fig. 27⁽²¹⁾. A silicon chip is mounted on a lead frame of copper with Ag-paste bonding and encapsulated by epoxy resin. Fig. 28⁽²¹⁾ shows the calculated thermal stress distribution in the resin over the chip under thermal shock by cooling from 150°C to -55°C. The stress components are indicated by the principal stress and the maximum shear stress. The stresses have the maximum values near the edge of the chip; resin cracking can be expected at this position. The stress concentration in the resin near the chip corner is calculated as shown in Fig. 29⁽²²⁾. The stress distributions are illustrated by nondimensional values of their radial and circumferential components in a polar coordinate. The radial stress is concentrated in the direction of 35° from the chip edge, while the circumferential stress is large in the vertical interface of the chip and also in the direction of 140° from the chip edge.

The surface mounting method of Fig. 30⁽²³⁾ is adopted for the plastic package. This is achieved by reflow soldering an encapsulated chip on printed circuit boards. The packaged chip is heated by the reflow soldering. Moisture absorbed in the encapsulated resin is evaporated by the heating process and the vapor pressure causes the fracture in the interface between chip pad and resin. Figure 31⁽²³⁾ shows the deformed state of plastic package by vaped pressure. The thick lines indicate the shape after deformation. The magnitude of the deformation is enlarged ten times compared with the model dimension. Large strain concentration is found near the bottom edge of the

chip pad. Cracking of resin is expected to be initiated from this position.

The prediction of crack initiation and propagation in the interface between encapsulated resin and chip pad is important to the estimation of device reliability. The criterion for the initial cracking in the interface between dissimilar materials is suggested by using the stress singularity at the interface⁽²⁴⁾. The intensity and order of the stress singularity are main parameters to determine the criterion. Figure 32⁽²⁴⁾ is the delamination condition based on the stress singularity criterion for the interface of models which consist of epoxy resin and Fe-Ni alloy with different dimensions.

Fig. 27 Schematic figure of plastic package

Fig. 28 Thermal stress distribution in plastic package

Fig. 26 Change of thermal radial stresses in hermetic seal

(a) Radial stress (b) Circumferential stress

Fig. 29 Thermal stress concentration at chip edge

Fig. 30 Schematic figure of surface mounted device

Fig. 31 Deformation of plastic package by vapor pressure

6. Quality Tests

The finished semiconductor device is subjected to mechanical and environmental tests for the screening and qualification. The main test items are as follows.

- (1) Heat resistance at 150°C
- (2) Cold resistance at -65°C
- (3) Impression of the maximum voltage at 125°C
- (4) Thermal shock from -65°C to 150°C in liquid
- (5) Thermal cycle between -65°C and 150°C in air
- (6) Heat resistance for soldering at 260°C
- (7) Humidity resistance at 85°C and 85% RH at maximum voltage
- (8) Pressure cooker at 130°C and 85% RH at maximum voltage
- (9) Spraying with salt water of 5% at 35°C
- (10) Acceleration at 20 000 G
- (11) Vibration at 2 000 Hz
- (12) Bending leads
- (13) Gas tight at 5 atm in helium gas
- (14) Fire resistance for gas flame

The testing items are related with mechanical, thermal, chemical, physical and electrical conditions, which give rise to coupled effects in the device. The effects are more severe than those caused by mechanical tests alone. Only the devices which pass the quality test can be used in electrical components.

7. Conclusions

There are many mechanical problems in the

Fig. 32 Delamination criterion based on stress singularity

production process of semiconductor devices. The characteristic factors common to these problems are summarized as follows.

(1) Miniature structure and laminated thin layers

A semiconductor device consists of minute parts with dimensions of less than a millimeter, as seen in wafers and interconnections. The integrated circuit on a chip is deposited by laminating thin layers. The material characterization of miniature and thin layered material systems is difficult as far as mechanical properties are concerned.

(2) Combination of dissimilar materials

Material combinations are found among ceramics in chip and substrate, metals in bumps and interconnection wire, and plastic in the package. There are many kinds of interfaces between dissimilar materials. The deformation and strength at the interface have significant effects on device performance.

(3) Bonding between dissimilar materials

There are many laminated or bonded portions in the device. Dissimilar films are laminated to deposit integrated circuits. Bonding between dissimilar materials is found in die bonding, interconnection and packaging. Bonding strength is important for device reliability.

(4) Phase transition

Wafers are prepared from single crystals which undergo phase transition from liquid to solid. The transition also occurs in the bonding materials between chip and frame, in the interconnecting portion and in packaging materials.

(5) Thermal cycle

Semiconductor chips are subjected to thermal

cycles in wafer processing, the interconnecting process and the packaging process. Thermal cycles also occur in the device due to equipment start-up and shut-down, load variations and climatic variations.

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