SINGLE CHANNEL PULSE HEIGHT DISCRIMINATION CIRCUIT IMPLEMENTED BY DUAL MONOSTABLE MULTIVIBRATOR

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1. INTRODUCTION

Current pulse height discriminator (PHD) is derived from universal double voltage comparators by adding several different function circuit units, including time-delaying and pulse width-expanding, which is quite complex and deteriorates PHD's performance. A novel, simple and practical method is presented.

2. Basic structure of PHD circuit

Basic PHD consists of upper level discriminator (ULD), lower level discriminator (LLD) and anti-coincidence circuit. It is simple, but in practice it cannot work properly.

A direct solution is to delay LLD output to a certain period, ensuring that it falls behind leading edge of ULD output. Meanwhile, ULD output is extended, ensuring that it is wider than that of LLD and can cover LLD output entirely.

3. Practical structure of a conventional SCA

Wang(1989) reveals schematic block of a practical PHD of a nuclear instrument module (NIM), which consists of ULD, LLD, monostable multivibrator, added circuit, R-S flip-flop and NOR gate. Researchers have made great efforts to improve PHD's performance with new methods(Chen, 2000, Yi, 2004).

4. Novel method and structure

Figure 1 presents schematic block of a novel PHD by means of dual monostable multivibrator, in which just one IC chip is included except comparators. Figure 2 shows the sketch waveforms.

5. Experiments and analysis

Concrete circuit is built based on the above method and tests are carried out. Main testing instruments are signal generator (Agilent 33220A) and digital storage oscilloscope (DSO) (Tektronics DPO 2024, 200MHz bandwidth, 4 channels). Testing input signals are sine wave, exponent falling wave and impulse wave. The circuit can work properly and reliably as predicted until the input signal frequency increase up to 1MHz on a universal board.

6. Conclusion

A novel, simple and practical method is proposed and its schematic is presented, which contains only a monolithic IC (dual monostable multivibrator) except comparators. Waveforms directly captured from DSO prove that the new method is feasible. The upper limit frequency is above 1MHz when the schematic is carried out on a universal board. It can be boosted up to 3MHz around if the schematic is put into

printed circuit board and faster comparator(National, 2001, Maxim, 2009) and monostable multivibrator are adopted.

Fig. 1 Schematic block of PHD implemented by dual monostable multivibrator

Fig. 2 Sketch waveforms of PHD implemented by dual monostable multivibrator

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ABSTRACT

In nuclear radiation measurement, pulse height discriminator (PHD) and single channel analyzer (SCA) are widely used to select pulses whose amplitude is within user's interesting range. PHD is derived from universal double voltage comparators by adding additional anti-coincidence circuits. Simple anti-coincidence method will generate false result, for the leading edge of upper comparator output falls behind that of lower comparator and pulse width of upper comparator output is narrower than that of lower comparator output. Anti-coincidence circuits in a conventional PHD and SCA often contain quite a few different circuits or components, such as monostable multivibrator and/or bistable flip-flop, NOR or NOT gate, etc. Such complex structure and manifold components deteriorate PHD's and SCA's response time and reliability. Great efforts have been made to simplify its structure and improve its reliability. Based on analyzing time sequence of the outputs of upper and lower voltage comparators, a novel, simple and practical structure is presented that contains only monolithic circuit (dual monostable multivibrator). Concrete circuits are fabricated and waveforms captured from digital storage oscilloscope (DSO) prove that it works properly and reliably till the input signal frequency increases up to 1MHz, regardless of sine wave, exponent falling or impulse signal. It can be utilized in the field of nuclear radiation measurement.

1. INTRODUCTION

In the field of radiation measurement, the output pulse amplitude of voltage sensitive preamplifier and spectrum amplifier is often proportional to the energy absorbed by the sensitive volume of the detector. Therefore, rays or particles, whose energy is within certain range, can be selected by selecting those pulses whose amplitude is within corresponding range. It can be achieved by PHD or SCA. Current PHD is derived from universal double voltage

comparator by adding several different function circuit units, including time-delaying and pulse width-expanding, which is quite complex and deteriorates PHD's performance. A novel, simple and practical method is presented by carefully analyzing time sequence of outputs and inputs of the universal double voltage comparators. Concrete circuit is implemented and waves captured from DSO prove that it works properly and reliably till the input signal frequency increases up to 1MHz, regardless of sine wave, exponent falling or impulse signal.

PHD circuit is a necessary unit in nuclear radiation measurement, such as scaler and nuclear detection instrument. Its basic function is to distinguish certain pulses from others whose amplitude satisfies user's requirement. PHD circuit has two working means: integral discrimination and differential discrimination (also called single channel height discrimination). In integral discrimination mode, those pulses are identified whose amplitude is above a certain voltage, called lower level discrimination threshold (LLDT). While in differential discrimination mode, pulses are identified whose amplitude is between two different voltages, LLDT and upper level discrimination threshold (ULDT). When a pulse is identified, a standard digital pulse, whose width and amplitude are regular and meet requirements of next stage circuit, is generated and delivered to next stage circuit. The following focuses on differential discrimination, unless otherwise noted.

2. Basic structure of PHD circuit

In terms of theory, basic PHD consists of upper level discriminator (ULD), lower level discriminator (LLD) and anti-coincidence circuit. The output of LLD connects to coincidence input port and ULD to anti-coincidence input port. If input pulse amplitude falls below LLDT, both LLD and ULD have no output and PHD has no output. If input pulse amplitude exceeds ULDT, both LLD and ULD have

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outputs. The anti-coincidence input is effective and PHD has no output. Only when input pulse amplitude falls between LLDT and ULDT, LLD has output and ULD has no output. PHD will generate output pulse.

But unfortunately, both rising edge and falling edge of input pulse have a certain slope other than ideal vertical. Therefore rising edge exceeds LLDT first and ULDT later. Furthermore, falling edge falls below ULDT earlier and LLDT later. Consequently, LLD output is generated earlier than that of ULD and width of ULD output is narrower than that of LLD. As anti-coincidence input, ULD output can not cover LLD output entirely and two output pulses are generated, showing in figure 1, which is completely wrong.

Fig. 1 Work waves of basic PHD

Fig. 2 Work waves of modified PHD

Direct solution to this conflict is to delay LLD output to a certain period, ensuring that it falls behind leading edge of ULD output. Meanwhile, ULD output is extended, ensuring that it is wider than that of LLD and can cover LLD output entirely, as shown in figure 2. Though the solution is simple, its shortcoming is almost fatal. Rising time and width of input pulses vary in different circumstances. It is impossible to pre-determine delaying time and extending width. It should be improved before it is applied in practice.

3. Practical structure of a conventional PHD

Figure 3 reveals schematic block of a practical PHD of a nuclear instrument module (NIM), which consists of ULD,

LLD, monostable multivibrator, added circuit, R-S flip-flop and NOR gate (Wang, 1989). Time-delaying of LLD output is implemented by triggering monostable multivibrator at trailing edge of LLD output. Thus delayed LLD output starts at trailing edge of LLD output. Its width depends on RC constant of monostable multivibrator. On the other hand, added circuit and bistable flip-flop fill the role of extending ULD output. Extended ULD output starts at leading edge of ULD and ends at trailing edge of delayed LLD output. Therefore, extended ULD output could cover delayed LLD wholly. NOR gate acts as anti-incidence circuit. Delayed LLD output operates as incidence input and extended ULD output as anti-incidence input, which is high level when the input amplitude falls below ULDT.

Fig. 3 Schematic block of a practical PHD

This circuit can discriminate those actual pulses that have certain leading edge time. But it contains quite a few different circuits, as stated above. This will increase circuit cost and at the same time its complexity, which would deteriorate its response time and reliability. Furthermore, for each circuit has a certain delay time, and the more units the circuit contains, the longer time the circuit will delay.

Researchers have made great efforts to improve PHD's performance with new methods. A new anti-coincidence circuit is developed which adopts direct logic discriminance to reduce resolving time (Chen, 2000). But the anti-coincidence circuit contains four different components: a dual D flip-flop, an inverter, a buffer and a counter. A single channel pulse height analyzer based on FPGA is built (Yi, 2004), whose outputs from LLD and ULD are counted by two counters in FPGA and SCA's output pulses is obtained from difference between two counters. Its hardware circuit is rather simple, thus its reliability is enhanced by reducing number and category components. On the other hand, extra clock synchronization is inserted to avoid wrong readings due to asynchronous operations of two counters.

4. Novel method and structure

Carefully analyzing the time sequence of ULD and LLD outputs, though leading edge of ULD output falls behind that of LLD output, it starts earlier than trailing edge of LLD output. The delaying unit can be omitted if leading edge of anti-incidence input is generated by leading edge of ULD output. The extending unit can be omitted if trailing edge of anti-incidence input is generated by trailing edge of LLD output.

Figure 4 presents the schematic block of a novel SCA by means of dual-monostable multivibrator. Both monostable multivibrators are triggered at falling edge. ULD outputs negative pulse to monostable multivibrator 1 and LLD outputs positive pulse to monostable multivibrator 2. Meanwhile LLD output acts as reset pin of monostable multivibrator 1.

Output of monostable multivibrator 1 operates as reset pin of multivibrator 2. Figure 5 shows the sketch waveform.

Fig. 4 Schematic block of PHD implemented by dual monostable multivibrator

Fig. 5 Work waves of PHD implemented by dual monostable multivibrator

Many companies manufacture variable comparators and monostable multivibrators that have different performance for diverse purposes. It is easy to construct concrete circuit to implement the above schematic. For convenience to test on a bread board or universal board, two individual comparators (LM311) and one dual monostable multivibrator (MC14528B) are chosen to build the circuit, with a few capacitors and resistors acting as auxiliary components. Figure 6 shows the schematic circuit diagram.

Fig. 6 Schematic circuit diagram for novel method

5. Experiments and analysis

Main testing instruments are signal generator (Model: Agilent 33220A) and digital storage oscilloscope (Model: Tektronics DPO 2024, 200MHz bandwidth, 4 channels). Testing input signals are sine wave, exponent falling wave and impulse wave. Figure 7 shows waveforms directly

captured from DSO. The signals are tagged as 1, 2, 3 and 4 from top to down, which denote input signal, ULD output, LLD output and SCA output. When the input amplitude exceeds ULDT, LLD outputs a positive pulse and ULD outputs a negative pulse. When the input amplitude falls between LLDT and ULDT, LLD outputs a positive pulse and ULD remains high. The SCA outputs a logic pulse, whose width is determined by RC constant of monostable multivibrator. The PHD logic output can be negative or positive as demanded. The circuit can work properly and reliably as predicted until the input signal frequency increase up to 1MHz on a universal board. When the frequency exceeds 1.2MHz, the circuit cannot work reliably.

(a) Sine wave, amplitude between ULDT and LLDT

(b) Sine wave, amplitude exceeding ULDT

(c) Exponent falling, amplitude between ULDT and LLDT

(d) Exponent falling, amplitude exceeding ULDT

(e) Impulse, amplitude between ULDT and LLDT

(f) Impulse, amplitude exceeding ULDT

Fig. 7 Actual working waves of PHD by means of dual monostable multivibrator

There are two main reasons limiting the available frequency. Firstly, LM311's response time is rather long, typically 200ns (National, 2001), and its output rise time exceeds 100ns. So total time for LM311 output amplitude reaching MC14528B's trigger threshold will exceed 300ns. If the input signal frequency is too high, or the ULDT and LLDT are very close to the input signal maxima amplitude, there will be not enough time for LLD and ULD to response. Hence, the circuit cannot operate as expected.

Secondly, the monostable multivibrator response time is another cause. MC14528B's typical propagation delay from reset signal to the output is between 100ns and 1000ns (under recommended condition), which determines the minimum interval between the LLD output and ULD output. This minimum interval implies that the input pulse width could not be too narrow. For example, some commercial Sacs, such as ORTEC SCA 550A and timing SCA 551 (ORTEC, 2008), demand that the minimum input pulse width should be 100ns.

If the above schematic is carried out on a printed circuit board and faster components are applied, the upper limit frequency can be well improved. If LM311 is replaced with MAX998, whose typical response time and output rise time are 28 ns and no less than 2 ns respectively (Maxim, 2009), the upper limit frequency may be 3MHz around.

6. Conclusion

Because rising edge and falling edge of an actual pulse have a certain slope other than ideal vertical, leading edge of ULD output falls behind that of LLD output and width of ULD output is narrower than that of LLD output. It is necessary to delay LLD output and extend ULD output to implement SCA function, which several different ICs are involved in a conventional SCA circuit. On the basis of analyzing time sequence of LLD output and ULD output, a novel, simple and practical method is proposed, in which leading edge of the anti-incidence pulse is generated by

leading edge of ULD output and trailing edge of the anti-incidence pulse by trailing edge of LLD output. Thus the delaying unit and extending unit can be omitted.

Schematic is presented, containing only a monolithic IC (dual monostable multivibrator) except comparators. Waveforms directly captured from DSO prove that the new method is feasible. The upper limit frequency is above 1MHz when the schematic is carried out on a universal board. It can be boosted up to 3MHz around if the schematic is put into printed circuit board and faster comparator is adopted.

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