PAPER

Low-Power Single-Slope Analog-to-Digital Converter with Intermittently Working Time-to-Digital Converter

Daisuke Uchida¹, Masayuki Ikebe¹, Junichi Motohisa¹ and Eiichi Sano²

¹Graduate School of Information Science and Technology, Hokkaido University

Kita 14, Nishi 9, Sapporo 060-0814, Japan

²Research Center for Integrated Quantum Electronics, Hokkaido University

Kita 13, Nishi 8, Sapporo 060-8628, Japan

E-mail: uchida@impulse.ist.hokudai.ac.jp, {ikebe, motohisa}@ist.hokudai.ac.jp, esano@rciqe.hokudai.ac.jp

Abstract We propose a single-slope analog-to-digital converter (ADC) with an intermittently working time-to-digital converter (TDC). Applying an n -bit TDC reduces the conversion time by a factor of 2^n , and using multiphase clock signals achieves timing consistency and realizes robust metastability. We focus on the operation time of the TDC. Since a TDC must operate continuously, it requires a large dissipation power. We propose generating the pulse-width modulation (PWM) signal of a single-slope ADC and apply a scheme for limiting the TDC operation period in order to reduce the TDC power dissipation. We designed and fabricated a 12-bit ADC, which consists of a 6-bit TDC and a 6-bit single-slope ADC, by using a $0.18\ \mu\text{m}$ CMOS process. The ADC operated at $100\ \text{kS/s}$ consumed $5.5\ \mu\text{W}$ from a $1\ \text{V}$ supply. Its INL and DNL were $+1.9/-1.9\ \text{LSB}$ and $+0.5/-0.8\ \text{LSB}$, respectively.

Keywords: analog-to-digital converter (ADC), single-slope ADC, time-to-digital converter (TDC), low power, intermittently working

1. Introduction

A single-slope ADC (SS-ADC) is well known as one of the simplest and smallest ADCs; thus, it is widely used in compact devices such as column parallel ADCs for complementary metal-oxide-semiconductor (CMOS) imagers and some sensing circuits. Figure 1 shows the operation of an SS-ADC; when an input analog signal and a ramp signal are given to a comparator, the comparator outputs a pulse-width modulation (PWM) signal. The ADC digitizes the analog signal by counting the number of “high” periods of the PWM signal by using a clock signal. Although the SS-ADC has the advantage of a small size, it has the disadvantages of a long operation time and high power consumption at a high conversion resolution. Whenever the accuracy of the ADC doubles, so does the operation time, and the power consumption also increases. Therefore, a multistage ADC with multiramp signals or high-speed operation with a high-frequency clock signal was proposed to solve this problem [1, 2]. However, it is difficult to operate at a low power with a high-frequency clock signal. Also, the multiramp signal generator requires complicated signal control and digital calibration for

Fig. 1 Operation of SS-ADC

consistency between ADC stages.

To realize a simple high-speed SS-ADC, we previously proposed a hybrid ADC configuration, which is an SS-ADC with a time-to-digital converter (TDC) using multiphase clock signals. This configuration can reduce the number of operation cycles of the ADC without a high-frequency clock signal [3, 4] and maintain consistency between the ADC and the TDC using simple circuits.

In this study, we focus on the SS-ADC with the TDC configuration; by applying intermittent operation to the TDC, we develop a high-speed and low-power SS-ADC. This paper is organized as follows. Section 2 describes the SS-ADC/TDC with multiphase clock signals. The details

Fig. 2 Block diagram of ADC with TDC

Fig. 3 (a) Operation of single-slope ADC with TDC, (b) 3-bit TDC code with multiphase clock

and analyses of the SS-ADC with the intermittently working TDC for low-power use are presented in Sect. 3. In sect. 4, experimental results for the proposed architecture are demonstrated.

2. Single-Slope ADC with TDC

2.1 Operation scheme of single-slope ADC with TDC

Figure 2 shows a block diagram of the SS-ADC+TDC configuration. It has two stages. The first is a TDC with multiphase clock signals, a number of D-FFs and an encoder. The second is an SS-ADC with a ripple counter, a comparator and a ramp-signal generator. The ramp-signal generator, which is connected to a comparator, generates a reference saw-wave signal. Figure 3(a) shows the operation of the ADC with the TDC. This circuit performs coarse and fine A/D conversions. When V_{in} and V_{ramp} are given to the comparator, the SS-ADC starts coarse A/D conversion and the counter outputs upper bits. Then, the comparator generates a quantization error between the PWM signal and clock signal. The quantization error is given to the TDC and digitized as lower bits so that fine A/D conversion is performed.

Figure 3(b) shows the TDC code with 3-bit resolution. The master-clock ($clk[0]$) period is denoted as T_{clk} . The code shows the time shift of the multi-phase clock ($clk[0:3]$). The TDC measures the quantization error of the SS-ADC within one clock period. Applying a TDC with n -bit resolution to the SS-ADC, the conversion time is reduced by a factor of 2^n . Therefore, the SS-ADC with the

Fig. 4 Circuitry of synchronized TDC

Fig. 5 Transient characteristic of meta-stability

TDC can operate faster without high-speed clock signals.

2.2 Consistency between ADC stages

In the combined usage of the SS-ADC and the TDC, special care should be taken to ensure the consistency between the TDC and the counter. By ‘consistency’ we mean that the lower bits (TDC output) have to be coupled with the upper bits (counter output). In other words, the settled TDC state completely decides the counter state with synchronization. Generally, a shared clock is given to a TDC and a counter for consistency. However, when the falling edge of the stop signal (comparator output) is close to the clock signal timing, metastability occurs and these circuits operate with individual timings. Thus, even using a shared clock, the consistency degrades owing to the metastability. An adjustment to the delay also cannot fundamentally handle the metastability. Exact consistency is important for robustness against metastability.

Figure 4 shows a block diagram of our synchronized TDC. Only a master clock without a phase shift is used for the counter through the first D-FF of the TDC (CLK_count). In this configuration, the settled state of CLK_count induced by the PWM signal completely fixes the counter state. Consistency between the TDC and the counter can be achieved by using this scheme. However, when the PWM signal is close to the clock signal, metastability occurs on CLK_count and miscodes may be generated. We therefore applied a Schmitt trigger between the TDC and the counter to remove the metastability of CLK_count . Using a node- A signal, which is the CLK_count signal through the Schmitt trigger, we obtain

Fig. 6 Circuit delay with meta-stability

Fig. 7 Intermittent operation of TDC

exact consistency/synchronization between the TDC and the counter.

We designed the circuit by using a 0.18 μm CMOS process and analyzed the circuit characteristics through Cadence Spectre simulation software. Figure 5 shows the transient characteristic of the metastability. When the falling PWM signal approached the rising clock signal, large signal delays and signal distortion were confirmed. However, these signals passed through the Schmitt trigger, and the D-latch output was stabilized. A signal delay through the D-latch has no effect on the counter accuracy. Figure 6 shows the circuit delay including the metastability under operation various process conditions (slow, typical or fast transistor operation). The delay of our circuit was less than 1.5 ns. The signal before passing through the Schmitt trigger caused both rising and falling delays. In comparison, the signal after passing caused only a rising delay. This is because the Schmitt trigger suppressed the falling delay and stabilized the D-latch output.

A stand-alone SS-ADC with a delay-line TDC was proposed for low-voltage use [2]. An additional circuit

Fig. 8 Block diagram of proposed ADC

Fig. 9 Circuitry of NAND inverter delay chain

was required to avoid metastability. Moreover, since there is no consistency between the ADC and the TDC, digital calibration was also needed.

3. Low-Power Scheme of SS-ADC with TDC

3.1 Intermittently working TDC

An SS-ADC with a multiphase clock TDC can reduce the number of operation cycles and maintain consistency between the ADC and TDC. However, continuous operation of the multiphase clock TDC is required for the consistency between the ADC stages. Multiphase clock signals are the fastest switching signals in the ADC with the TDC, which are input on each inverter-delay cell and each D-FF, and they alternately switch between the numbers “high” and “low” continuously. The major factors contributing to the power consumption are the supply of switched signals to these circuits and ensuring that these signals operate continuously [5, 6]. Therefore, the TDC with the multiphase clock signal consumes too much power, making it difficult to provide flexibility in the resolution of the TDC. To increase the resolution, it is necessary to reduce the power consumption. Here, we focus on the delay cells generating the multiphase clock signals and propose an intermittent TDC operation scheme. This technique can greatly reduce power dissipation.

Figures 7 and 8 show the proposed intermittent operation. The previous TDC configuration operates continuously until the PWM signal falls. A “high” period of the PWM signal is denoted as T_{PWM} . Here, we focus on the timing of the T_{PWM} falling edge and consider the delay

Fig. 10 Transient characteristics of intermittent TDC

Fig. 11 (a) Conventional NAND inverter cell, (b) rising delay plotted against control voltage

Fig. 13 Rising delay of proposed NAND inverter cell

Fig. 12 (a) Proposed NAND inverter cell, (b) voltage-controlled NAND cell

Fig. 14 Duty ratio of proposed NAND inverter cell

signal $T_{PWM} + \Delta T_{PWM}$, which is generated from T_{PWM} through a delay signal and an enable generator composed of normal delay cells. Then, we can produce a time window signal, *enable*, and restrict the TDC working during ΔT_{PWM} . In other words, we can achieve intermittent TDC operation by using the time window ΔT_{PWM} . Also, as shown in Fig. 9, the *enable* signal is given to each NAND inverter delay cell. The delay cells operate in the same way as the inverter only when the *enable* signal is “high.” The delay cells output multiphase clock signals in the

period of ΔT_{PWM} and supply them to the D-FFs. Except for in ΔT_{PWM} , the output signals of the delay cells and the D-latch in the D-FFs are not switched. As a consequence, the working time is much lower than that of a conventional TDC.

In this architecture, the SS-ADC digitizes the period of $T_{PWM} + \Delta T_{PWM}$ so that the output code of the ADC has some value that is offset along with ΔT_{PWM} . Since the power dissipation of the TDC is only for a short period, we can set the resolution of the TDC to a higher value and

Fig. 15 Power consumption and area ratio of SS-ADC with TDC

realize a higher A/D conversion rate in the SS-ADC stage.

Figure 10 shows the transient characteristics of the proposed ADC. A/D and T/D conversions were performed in 7 μ s using a 10 MHz master clock. We confirmed the digitizing of the quantization errors and intermittent operation. We set the time of ΔT_{PWM} to 372 ns.

3.2 NAND inverter delay element

The correct amount of delay is required to make accurate measurements in the TDC with a multi-phase clock. It is necessary to maintain a constant delay in PVT variation. A voltage- or current-controlled delay element is commonly used for correcting the amount of delay [7-9]. However, delay control is difficult because the delay changes nonlinearly with the control voltage or current, and the range of the control voltage or current is restricted because the delay cell will not operate if the control voltage or current is too high. In addition, multiphase clock signals require not only a constant delay but also a symmetric duty. The usual methods used to maintain a constant delay control only positive- or negative-edge timing. Figures 11(a) and 11(b) show the conventional NAND inverter cell and the characteristics of rising delay with the control voltage respectively. By applying a step signal to the node *Master clock*, we observed the rising delay of the output signal. This rising-delay characteristic had strong nonlinearity, making it difficult to control the delay of the circuit.

Therefore, to generate the correct multiphase clock signals, we proposed a novel delay cell. Figure 12(a) shows the proposed delay element. This element consists of two NAND circuits and an inverter. One NAND circuit

Fig. 16 Die micrograph of proposed ADC

is a voltage-controlled delay cell, as shown in Fig. 12(b), and the other is a normal NAND circuit. In the voltage-controlled delay cell, the negative-edge timing is better controlled by applying V_{ctrl1} to M1, which is connected between V_{dd} and NAND circuit. The positive-edge delay is better controlled by applying V_{ctrl2} to M2, which is connected between ground (GND) and the NAND circuit. The normal NAND circuit sets a coarse amount of delay and the voltage-controlled NAND circuit adjusts the fine delay linearly using V_{ctrl1} and V_{ctrl2} . By combining them, the delay cell always behaves the same as the NAND circuit operation with a linear and tunable delay.

Figure 13 shows the characteristics of the rising delay of the delay cells with control voltages V_{ctrl1} and V_{ctrl2} . Compared with the conventional delay element (Figs. 11(a) and 11(b)), the proposed delay cell always performed correct operations and the linearity of the cell was improved. We confirmed that the timing of the rising edge was more affected by V_{ctrl2} than by V_{ctrl1} . Also, the timing of the falling edge was more affected by V_{ctrl1}

Fig. 17 Nonlinearity of proposed ADC

Table 1: ADC performance summary

Process	0.18 μm CMOS 1P6M
Area	$310 \times 563 \mu\text{m}$
Voltage supply	1 V
Resolution	12 bits
Sampling rate	100 kS/s
Total power	5.5 μW
DNL	+0.5/-0.8
INL	+1.9/-1.9

Table 2: Comparison of our ADC with those in other works

Ref.	Technology	Area(mm^2)	Resolution	Samp. Rate	INL	DNL	Power
[2]	90 nm	0.06	9 bits	1 MS/s	+1.5/-1.5	+1.2/-0.5	14 μW
[10]	90 nm	0.05	5 bits	250 MS/s	+0.18/-0.18	+0.14/-0.12	800 μW
[11]	0.18 μm	0.63	12 bits	100 kS/s	+0.5/-0.4	+1.1/-0.1	25 μW
[12]	0.5 μm	0.5	8 bits	1 MS/s	+0.66/-0.56	+0.58/-0.66	2.56 mW
Ours	0.18 μm	0.17	12 bits	100 kS/s	+1.9/-1.9	+0.5/-0.8	5.1 μW

by Vctrl2. Figure 14 shows the duty ratio of the proposed NAND inverter cell output. When Vctrl1 was 0.4 or 0.65 V, the delay cell achieved a 50% duty ratio; the ideal delay is derived from the following conditions:

- Duty ratio of delay cell < 0.5 LSB range.
- Delay time < 0.5 LSB range.

Using the former condition and the TDC resolution, an acceptable duty ratio can be determined. For example, a duty ratio from 48 to 52% was derived from the TDC code with 6-bit resolution. Using the latter condition and the master-clock period, an acceptable delay time can be determined.

When the clock period is 100 ns, the ideal delay time is limited in the range of $1.56 \text{ ns} (=100 \text{ ns} / 2^6) \pm 0.78 \text{ ns}$. In this study, we designed the circuits to obtain the ideal delay, then we manually set the control voltage for fine tuning of the delay.

3.3 Comparison of TDC performance in terms of resolution

In the hybrid ADC configuration, it is important to define the resolution of each ADC stage. The resolution of the previous TDC with continuous operation was limited by its power consumption and circuit area. When the resolution of the TDC doubles, the circuit area doubles because of the increased number of delay cells and D-FFs; the power consumption also increases because of the increased size of the TDC.

Figure 15 shows the power consumption and area ratio between the TDC and the whole circuit along with the

TDC resolution. We confirmed that the total power consumption was greatly reduced by the use of the intermittently working TDC. A 75% reduction in power consumption with 3-bit TDC resolution and a 50% reduction with 9-bit resolution were achieved compared with those for a continuous TDC scheme. Thus, the allowable circuit area mainly limits the TDC resolution with intermittent operation.

4. Experimental Results

The proposed 12-bit ADC was fabricated using 0.18 μm 1P6M CMOS technology. A die micrograph is shown in Fig. 16. The total area was $0.56 \times 0.31 \text{ mm}^2$. Figure 17 shows the nonlinearity of the ADC. The measured DNL and INL were +0.5/-0.8 LSB and +1.9/-1.9 LSB, respectively. The nonlinearity effect was observed in the ramp-signal generator characteristics.

Table 1 summarizes the performance of the proposed ADC. A comparison with ADCs in related works is given in Table 2 [2], [10-12].

5. Conclusion

We proposed a low-power SS-ADC with an intermittently working TDC that uses multiphase clock signals. Our ADC reduced the number of operation cycles by 98% (from 4096 to $64 + \alpha$ cycles) at the same resolution as a SS-ADC and achieved timing consistency between the ADC and TDC. The intermittently working TDC reduced the power consumption greatly. The entire

ADC consumed 5.5 μ W from a 1 V supply.

Acknowledgments

This work was partially supported by the Strategic Information and Communications R&D Promotion Program (SCOPE) and by the VLSI Design and Education Center (VDEC) at the University of Tokyo in collaboration with Cadence Design Systems, Inc.

References

- [1] S. Lim, J. Lee, D. Kim and G. Han: A high-speed CMOS image sensor with column-parallel two-step single-slope ADCs, *IEEE Trans. Electron Devices*, Vol. 56, No. 3, pp. 393-398, 2009.
- [2] S. Naraghi, M. Courcy and M. P. Flynn: A 9 bit, 14 μ W and 0.06 mm² pulse position modulation ADC in 90 nm digital CMOS, *IEEE J. Solid-State Circuits*, Vol. 45, No. 9, pp. 1870-1880, 2010.
- [3] M. Shin, N. Sakuraya, M. Ikebe, J. Motohisa and E. Sano: Column parallel single-slope ADC with time to digital converter for CMOS imager, *Proc. ICECS 2010*, Dec. 2010.
- [4] K. Kim, M. Ikebe, J. Motohisa and E. Sano: A 11 b 5.1 μ W multi-slope ADC with a TDC using multi-phase clock signals, *Proc. ICECS 2012*, Dec. 2012.
- [5] A. Alvandpour: Separation and extraction of short-circuit power consumption in digital CMOS VLSI circuits, *Proc. 1998 Int. Symp. Low Power Electronics and Design*, pp. 245-249, 1998.
- [6] A. Wiltgen and K. Escobar: Power consumption analysis in static CMOS gates, *Proc. Symp. Integrated Circuits and Systems Design*, pp. 1-6, Sept. 2013.
- [7] N. R. Mahapatra, S. V. Garimella and A. Tareen: An empirical and analytical comparison of delay elements and a new delay element design, *IEEE Computer Society Workshop on VLSI*, pp. 81-86, 2000.
- [8] M. Keskin: A rail-to-rail delay line for time analog-to-digital converters, *Proc. Int. Symp. Circuits and Systems (ISCAS)*, pp. 461-464, Aug. 2006.
- [9] H. Farkhani, M. Meymandi-Nejad and M. Sachdev: A fully digital ADC using a new delay element with enhanced linearity, *Proc. ISCAS*, pp. 2406-2409, May 2008.
- [10] P. J. A. Harpe, C. Zhou, K. Philips and H. de Groot: A 0.8-mW 5-bit 250-MS/s time-interleaved asynchronous digital slope ADC, *IEEE J. Solid-State Circuits*, Vol. 46, No. 11, pp. 2450-2457, 2011.
- [11] N. Verma and A. P. Chandrakasan: A 25 μ W 100 kS/s 12 b ADC for wireless micro-sensor applications, *ISSCC Dig. Tech. Papers*, pp. 222-223, Feb. 2006.
- [12] Y. Yafei, L. Liyuan, L. Fule, L. Dongmei and W. Zhihua: An 8-bit 1MHz successive approximation register (SAR) A/D with 7.98 ENOB, *Int. Conf. Anti-Counterfeiting, Security and Identification (ASID) 2011*, pp. 139-142, Jun. 2011.

Daisuke Uchida received his B.E. and M.E. degrees in electrical engineering from Hokkaido University, Sapporo, Japan, in 2012 and 2014, respectively. He is currently pursuing his Ph.D. degree in electrical engineering at Hokkaido University. His current research interests are the design of CMOS image sensors and analog

circuits.

Masayuki Ikebe received his B.S., M.S., and Ph.D. degrees in electrical engineering from Hokkaido University, Sapporo, Japan, in 1995, 1997, and 2000, respectively. During 2000-2004, he worked at the Electronic Device Laboratory, Dai Nippon Printing Corporation, Tokyo, Japan, where he was engaged in

the research and development of wireless communication systems and image processing systems. Presently, he is an Associate Professor at the Graduate School of Information Science and Technology, Hokkaido University. His current research includes CMOS RF circuits and analog circuits.

Junichi Motohisa received his B.S., M.S., and Ph.D. degrees from the University of Tokyo, Tokyo, Japan, in 1986, 1988, and 1993, respectively. He became a Lecturer at the Research Center for Interface Quantum Electronics (currently, Research Center for Integrated Quantum Electronics), Hokkaido University, Sapporo, Japan, in 1993, and an Associate Professor in 1994. Since 2008, he has been a Professor at the Graduate School of Information Science and Technology, Hokkaido University. His current research interests include the formation and char-

acterization of compound semiconductor nanostructures utilizing metal-organic vapor phase epitaxial growth and their application to electronic devices, photonic devices, and integrated circuits.

Eiichi Sano received his B.S., M.S., and Ph.D. degrees from the University of Tokyo, Tokyo, Japan, in 1975, 1977, and 1998, respectively. From 1977 to 2001, he was with NTT Laboratories, where he worked on MOS device physics, mixed analog/digital MOS ULSIs, ultrafast MSM photodetectors, electrooptic sampling, and high-speed electronic and optoelectronic ICs. In 2001, he joined the Research Center for Integrated Quantum Electronics, Hokkaido University, Japan, as a Professor. His current research interests include high-speed devices and circuits. He has published more than 200 papers in major journals and conference proceedings related to these research areas. Dr. Sano is a member of IEEE and JSAP and a Fellow of IEICE.

(Received May 20, 2015 ; revised August 11, 2015)