We are developing technology for camera systems to monitor humans using an intermittent-sensing scheme. In this system, to reduce power consumption, a CMOS image sensor is powered on and captures optical images when humans are detected using a low-power IR array sensor. A low-power analog front end (AFE) circuit that reads the small output voltage of an IR array sensor is required to create the system. Therefore, we examined the circuit for the IR array sensor using methods of a dual-slope integrating analog-to-digital converter (ADC). Consequently, a power reduction of approximately 83% compared with existing IR array sensor devices is expected. Another expected achievement is a battery life of about 12 months, which would be 4.7 times longer than that of the previous system using an existing IR array sensor device for the whole system.

2. Proposed Sensor Node

We have already developed a prototype GSSE. This chapter describes the power saving techniques that are introduced in the GSSE and the current issues with the sensor node.

2.1 Intermittent-sensing image sensor node

The prototype GSSE is composed of an IR array sensor, an image sensor, and a micro controller unit (MCU). We have introduced two low-power-consumption driving technologies for a long operating time. The first is intermittent operation; the image sensor is only powered on when an event is detected by the IR array sensor, as shown in Fig. 1(a). The other is the hardware design of the controller unit. The process that was performed by the MCU is now performed by dedicated hardware. These power savings greatly reduced the power consumption from 262 mW to 3.6, enabling our proposed system to extend its operable time to 76 days with two AA batteries [5].

However, further power saving is required for effective use of the sensor network. We have analyzed the power consumption of the present sensor node and found that the power consumption of the IR array sensor is 94.8% of the total power, as shown in Fig. 1(b). In this study, we aimed to extend the drive time of the sensor node to one year by saving power in the IR array sensor.
2.2 IR array sensor

The IR array sensor that was used in the prototype sensor node was a Grid-EYE from Panasonic. Fig. 2 shows a block diagram of the Grid-EYE.

Thermopile elements do not consume power, so most of the power consumption is from the circuit portion of the AFE. In particular, careful design is needed for the first stage of the AFE because thermopile elements show high resistance and very weak output voltage, the order of which is as small as hundreds of microvolts. Accordingly, the AFE circuit of the Grid-EYE has to amplify the signal with a precision operational amplifier in the first stage and digital conversion with an ADC in the second stage. Therefore, the circuit scale is large, and power consumption increases.

3. Dual–Slope Integrating ADC

High-precision and low-power circuits are needed to design an AFE circuit for thermopile elements. In this design, the temperature detection range was limited from 0 to 50 degrees for human detection, and its resolution was set to 8 bits for AFE circuit for simplicity. Regarding the signal processing speed, the number of pixels was set to 16x16, and the operation of one frame per second was assumed without performing high-speed processing such as that done by a CMOS image sensor. In addition, all pixels were read out by one of the circuit system. Regarding high precision, measures should be taken for the offset voltage and noise. These measures are described in Chapter 4. In considering them, we adopted a dual-slope integrating ADC method.

3.1 Operation of the examination circuit

Fig. 3 and 4 show the basic dual-slope integrating ADC and the output waveform of integrator. In this section, we describe the operation of the circuit. The A/D conversion for one sample is completed in three phases, reset phase $T_r$ (switch $r$ is turned on), integration phase $T_1$ (switch $a$ is turned on), and inverse integration phase $T_2$ (switch $b$ is turned on). First of all, the charge of the integrating capacitor is set to 0 in phase $T_r$. Next, sensor signal $sV$ is changed to current with a V/I converter and to voltage again with an I/V converter in phase $T_1$. At the end of this phase, the output voltage of I/V converter $1_{oV}$ is a value obtained by time integration with the slope $CGmVs/cV$. Then, in phase $T_2$, $1_{oV}$ is integrated with slope $CGmVr$ to the reverse direction starting from the final voltage of phase $T_1$. Where $Gm$ is the transconductance of the V/I converter. $V_{o2}$ obtained is compared with $V_{c}$ using a voltage comparator of the next stage. As a result, the timing of the increase changes depending on the $sV$. Therefore, the digital value can be obtained proportional to the sensor output by measuring time with the counter until voltage $V_{o2}$ becomes high (e.g., 3.3V).

3.2 Chip design and evaluation of element circuit

We designed and fabricated a V/I converter, I/V converter, operational amplifier, phase changeover switch, and functional circuit block composed of them.
Fig. 5 shows the waveforms obtained from the circuit block by setting predetermined voltages for each terminal. The input voltage of $V_c = 1V$, $V_s = V_c + 0.5mV$, $V_r = V_c - 0.5mV$. The output voltage waveforms $V_{ol}$ and $V_{o2}$ are obtained successfully by adjusting the offset voltages at the input terminals $V_s$ and $V_r$.

However, these waveforms such as $V_{ol}$ and $V_{o2}$ are degraded when the offset is not adjusted. This is caused by output voltage in the sensor element that is too small. In other words, the offset voltage due to the mismatch of transistors, for example, is substantially larger than the input voltage difference of $V_s$, $V_r$, and $V_c$. Although we had taken measures to increase transistor sizes against offset and flicker noise, the influence of the offset was still larger than the predicted level.

Therefore, a high precision V/I converter using another technique should be used at the front stage. However, the method increases the circuit area and leads to increased power consumption. Thus, we solved this problem by embedding a simple mechanism for canceling the offset voltage.

4. AZ Mechanism with Dual-Slope Integrating ADC Introduced

An auto zero (AZ) mechanism can be used as a means to cancel the offset voltage [6]. This mechanism can be created by providing capacitance and changeover switches. Our circuit cancels the offset voltage of the V/I converter and other operational amplifiers by embedding the AZ mechanism.

4.1 Operation of the circuit

Fig. 6 shows the dual-slope integrating ADC with the AZ mechanism. The operation of our circuit consists of three phases as with the circuit in Fig. 3.

In phase $T_1$, both input terminals of the V/I converter are shorted for extracting the input referred offset of V/I converter $V_{o10}$ as a form of the output referred offset voltage. Specifically, the output of the V/I converter is fixed at $V_c + A_0 V_{o10}$, where $A_0$ is the voltage gain.

Moreover, a feedback loop is formed with amp2 for extracting the input referred offset voltage of amp2 operating as a voltage comparator. Therefore, capacitance $C_{az}$ charges the output referred offset voltage of the V/I converter at the input terminal and input referred offset voltage of amp2 at the output terminal. In addition, the output of the I/V converter is fixed at $V_{o1} = V_c + V_{o10} - V_{o20}$, and the output of the voltage comparator is fixed at $V_{o2} = V_c + V_{o20}$, where $V_{o1}$ is the input referred offset voltage of amp2 in the I/V converter and where $V_{o2}$ is the input referred offset of the voltage of the comparator.

In phase $T_2$, integrated waveform $V_{ol}$ and the output waveform of comparator $V_{o2}$ can be shown using the following equations.

\[ V_{o1} = (V_c + V_{o10} - V_{o20}) - \frac{Gm}{C} V_s T_1 \]  
\[ V_{o2} = \left[ (V_c + V_{o10} - V_{o20}) - \frac{Gm}{C} V_s T_1 + V_{o20} \right] - (V_c + V_{o10}) A_2 = -\frac{Gm}{C} V_s T_1 A_2 \]  

where the term $(V_c + V_{o10} - V_{o20})$ of equation (1) is the reference voltage for starting integration. Although they include the offset voltages $V_{o10}$ and $V_{o20}$, they do not cause significant error in the signal processing. The reason is this term is just a reference DC level and not related to the processing of the integration. Also, the last term $- (Gm/C) V_s T_1$ is multiplied by the time and slope of integration when applying $V_s$. The input referred offset of the V/I converter $V_{o10}$ remains in the last term of the equation (1) if the AZ scheme is not used. However, the offset does not affect the slope of the integration to cancel the offset using an AZ mechanism. Equation (2) means that offset $V_{o10}$ and $V_{o20}$ are canceled.

In phase $T_2$, $V_{ol}$ and $V_{o2}$ can be shown using the following equations.

\[ V_{o1} = (V_c + V_{o10} - V_{o20}) - \frac{Gm}{C} V_s T_1 + \frac{Gm}{C} V_s T_2 \]  

\[ V_{o2} = \left[ (V_c + V_{o10} - V_{o20}) - \frac{Gm}{C} V_s T_1 + V_{o20} \right] - (V_c + V_{o10}) A_2 = -\frac{Gm}{C} V_s T_1 A_2 \]  

where the term $(V_c + V_{o10} - V_{o20})$ of equation (1) is the reference voltage for starting integration. Although they include the offset voltages $V_{o10}$ and $V_{o20}$, they do not cause significant error in the signal processing. The reason is this term is just a reference DC level and not related to the processing of the integration. Also, the last term $- (Gm/C) V_s T_1$ is multiplied by the time and slope of integration when applying $V_s$. The input referred offset of the V/I converter $V_{o10}$ remains in the last term of the equation (1) if the AZ scheme is not used. However, the offset does not affect the slope of the integration to cancel the offset using an AZ mechanism. Equation (2) means that offset $V_{o10}$ and $V_{o20}$ are canceled.
Equations (3), (4) also indicate all offset voltages are canceled. Therefore, the offset voltage of each operational amplifier is canceled according to this mechanism, and the operation of the dual slope integration is achieved without adjusting the input voltage. In addition, low-frequency flicker noise can also be canceled using this mechanism.

### 4.2 Evaluation results

We designed and fabricated the circuit shown in Fig. 6 excluding a digital controller. Fig. 7 shows the experimental results. We applied the predetermined voltage to each terminal. The operating frequencies of the analog and digital circuit are 1 kHz and 1 MHz, respectively. In addition, the input terminal $V_s$ is changed based on the assumption that the output voltage of the sensor is changed by the temperature. The functions of the dual-slope integration and the voltage comparison without adjusting the offset voltage are clear from waveforms $V_{o1}$ and $V_{o2}$ of Fig. 7(a), and the effect of the AZ mechanism was found to work. Also, the monotonicity of the dual-slope ADC in level of about 0.1 mV can confirm, as shown in Fig. 7(b).

In addition, although it cannot be a fair comparison because a selector, digital controller, and the like were not used in the proposed circuit, the power consumption of the circuit was estimated to be about 0.577 mW, which is 83% lower than that of existing devices. Fig. 8 shows the comparison. The whole power consumption can be reduced to about 0.764 mW, and the operable time of the sensor node is expected to increase from 76 days to 360 with two AA batteries.

### 5. Conclusion and Future Work

An AFE circuit supporting an IR array sensor was designed to save power in our proposed sensor node. The sensor can operate for about 12 months without battery replacement, which is 4.7 times longer than the previous system using a Grid-EYE. In the future, we will introduce an intermittent operating mechanism to the AFE circuit for further power saving.

**References**


