RESEARCH NOTE

Automated Synthesis of Simple Nonlinear Analog Circuits by Means of Genetic Algorithm

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Abstract The synthesis of analog electronic circuits involves the design of their input-output characteristic and the selection of suitable elements. The design of analog electronic circuits is difficult, and in general, there has been no general automated synthesis procedure. Therefore, a number of automated synthesis procedures of analog circuits have been proposed. Koza et al. proposed an automated synthesis procedure using genetic programming. The automated synthesis procedure can automatically create parameterized topologies of the desired analog circuit. However, this synthesis procedure uses an infinite number of devices, and therefore the scale of the generated circuits is very large in many cases. In a real design process, only the finite number device can be used. Also, the generated circuits are only evaluated by a numerical simulation, namely, SPICE. The generated circuit is required to have stability and reproducibility. In this paper, we propose a novel automated synthesis procedure for a two-port circuit which has a simple nonlinear characteristic, by means of a genetic algorithm. The proposed method generates a suitable circuit which uses minimum resources.

Keywords: genetic algorithm, analog circuit, SPICE, simulation, emergence, automated synthesis procedure

1. Introduction

The synthesis of analog electronic circuits involves the design of their input-output characteristic and the selection of suitable elements. The design of analog electronic circuits is difficult, and in general, there has been no general automated synthesis procedure[1]-[3]. Koza et al. proposed an automated synthesis procedure that used genetic programming[1],[2]. The synthesis procedure can automatically create parameterized topologies of the desired analog circuits without circuit design theory. The procedure, however, uses an infinite number of devices, and therefore the scale of the generated circuits is very large in many cases[1],[2]. In a real design process, only the finite number device can be used.

In order to emerge a desired analog circuit that uses the minimum number of resources of actual discrete devices, we propose a novel automated synthesis procedure that uses a genetic algorithm for a two-port

circuit which has simple nonlinear characteristics. The genetic programming procedure proposed by Koza et al. requires a powerful computational capacity[1],[2]. In comparison with the genetic programming, the genetic algorithm does not require such a large computational capacity. Therefore, the genetic algorithm is applied in our system. In our procedure, each gene of the genetic algorithm corresponds to a device in the analog circuit. The circuit is composed of E24 series resistors, Bipolar Junction Transistors (BJTs), and diodes. These devices are applied to the proposed system because they are widely used in actual implemented analog circuits, and they are easily obtainable. Note that we assume that the input to the circuit is DC. Therefore, the emerged circuit is not composed of inductance and capacitance to simplify the circuitry.

In this paper, each device is regarded as a gene. The expression of the gene describes SPICE netlist. The circuit consists of multiple devices, therefore, multiple genes are connected and these are called a chro-

mosome in this paper. The chromosome represents the SPICE netlist which corresponds to the generated circuit. The number of genes in a chromosome is variable, but there is an upper limit because only the finite number device can be used. The proposed method generates a suitable circuit which consists of the minimum amount of resources. In order to evaluate the generated circuits, we analyze their characteristics by means of SPICE simulation. By using the simulation results, we calculate an evaluation value for the chromosome. The genetic algorithm generates new chromosomes based on the evaluation value.

We will show an experimental result of a sigmoid function circuit which can be regarded as an activation function in an artificial neuron. The experimental result indicates good agreement with the characteristic that was obtained by SPICE simulation.

2. System

The simple nonlinear analog circuit is represented by a two-port circuit which is composed of two voltage input terminals and two voltage output terminals, as shown in Fig.1. In this paper, we assume the two-port

Fig. 1 Two-port circuit

circuit contains Bipolar Junction Transistors (abbr. BJTs). Because the BJT is operated by a current, the input voltage must be converted into the input current. In Fig.1, "V-I" denotes a voltage controlled current source (VCCS). "I-V" denotes a current controlled voltage source (CCVS). In this paper, we adopt the VCCS and the CCVS circuits shown in Fig.2 and Fig.3, respectively.

Fig. 2 VCCS

Fig. 3 CCVS

Since the input-output characteristic of $f(I_{in})$ in Fig.1 is the most important, we propose an automated synthesis procedure of the function which satisfies a desired input-output characteristic. The automated synthesis procedure is based on a genetic algorithm. The genetic algorithm is one of the most effective tools for searching for an optimal solution[4]. The genetic algorithm produces a desired analog circuit topology which has a desired input-output characteristic of $f(I_{in})$. The conceptual diagram of the proposed genetic algorithm system is illustrated in Fig.4.

In order to emerge an appropriate circuit by the genetic algorithm, the devices making up circuits are converted into genetic information.

Fig. 4 Conceptual diagram of the proposed GA system

We define the genetic arrangement as shown in Fig.5. The gene consists of four parts, and these parts

Fig. 5 The genetic arrangement of a device

represent the read only attribute, the type of the device, the node number which corresponds to the number of terminals of the device, and the value of the device. If the read only attribute is true, proposed system does not change the properties of the gene. This attribute is used for the description of the external circuit.

Since the generated circuit is simulated on SPICE in order to evaluate the circuit properties, the circuit

must be described by the SPICE netlist. The SPICE netlist specifies the kind of device, the node number, and the device characteristics. Therefore, the gene describes the SPICE netlist. The device information can be described by a binary code as shown in Table 1. In this study, we assume that the input of the emerged

Table 1 Kinds of devices and their corresponding genetic codes

device	code
Resistor	0001
Diode	0011
Transistor	0100
Power source	0101

analog circuit is DC. Therefore, the emerged circuit is not composed of inductance and capacitance.

The node number converts to a binary expression as shown in Fig.6(a). In the case of resistors, their values are explained by a floating point expression which consists of a mantissa part and an exponent part, as shown in Fig.6(b). Note that the values of the resistors are applied to the E24 series. In the cases of

Fig. 6 Expression of the node number

diodes and transistors, the gene expression denotes its SPICE model.

The circuits consist of multiple devices, therefore, multiple genes are connected as shown in Fig.7, and this is called a chromosome. A chromosome corre-

Fig. 7 Expression of a chromosome which consists of multiple connected genes. This sequence corresponds to a circuit.

sponds to a circuit. In order to simulate the circuit with the SPICE simulator, it is necessary to provide SPICE with a netlist describing the circuit to be analyzed. The devices discussed in this paper, are widely used in actual implemented analog circuits, and they are easily obtainable. We apply the diode to IN4002. BJTs are applied to 2SA1015Y and 2SC1815Y. The netlists of these devices in our simulation are shown in Fig.8. Also, the resistors are applied to the E24 series.

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2SA1015Y
.model Q2 PNP(Is=295.1E-18 Xti=3 Eg=1.11 Vaf=100
+ Bf=140 Ne=1.5 Ise=0 Ikf=0 Xtb=1.5 Br=10.45
+ Nc=2 Isc=0 Ikr=0 Rc=15 Cjc=66.2p Mjc=1.054
+ Vjc=.75 Fc=.5 Cje=5p Mje=.3333 Vje=.75
+ Tr=10n Tf=1.661n Itf=0 Vtf=0 Xtf=0)

2SC1815Y
.model Q1 NPN(Is=2.04f Xti=3 Eg=1.11 Vaf=6 Bf=140
+ Ne=1.5 Ise=0 Ikf=20m Xtb=1.5 Br=3.377 Nc=2
+ Isc=0 Ikr=0 Rc=1 Cjc=2p Mjc=.3333 Vjc=.75
+ Fc=.5 Cje=5p Mje=.3333 Vje=.75 Tr=10n
+ Tf=311.1p Itf=0 Vtf=0 Xtf=0)

IN4002
.model D1 D(Is=1.411000e-008 RS=0.033890 N=1.984000
+ TT=4.761000e-006 CJO=5.117000e-011
+ VJ=0.390500 M=0.276200 EG=1.110000
+ XTI=3.000000 KF=0.000000 AF=1.000000
+ FC=0.500000 BV=100.100000 IBV=10.000000)

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Fig. 8 The netlist of BJTs and diodes

3. Synthesis Procedure

In this section, we demonstrate the automated synthesis procedure. First, we decide on the number of chromosomes, and the initial configuration of the chromosomes is set randomly. First, to emerge the topology of the circuit, the initial value of all resistors is set as 1[kΩ]. If there are many chromosomes, it is possible to search efficiently. However, the system requires a large computational capacity in the numerical simulation. Therefore, the number of chromosomes in the following simulation is 10.

Next, we implement the alternation of generations. In the alternation of generations, the system computes the evaluation value of each chromosome. Each chromosome corresponds to a circuit which is described by the netlist of SPICE. Therefore, we analyze the characteristics of the circuit by using a SPICE simulator, and the evaluation value is computed based on the simulation results. The chromosomes with high evaluation values are left and the chromosomes with low evaluation values are eliminated. The new generation is generated from the left chromosomes. A mutation operation occurs in some of the generated chromosomes. In this paper, mutations are classified into three types. One is the operation to change the length for an elastic chromosome. This operation is equivalent to fluctuating the number of devices in the circuit. When an elastic chromosome is stretched, it randomly chooses the gene which is added. When the elastic chromosome is shortened, it randomly selects the gene which is deleted. Note that the maximum and minimum lengths of the elastic chromosome are given, so that the above operations occur within the range of possible length. In this paper, the maximum length of the elastic chromosome is set to be 21.

The second mutation operation is changing the kind of gene which indicates the device. The gene to be changed is chosen randomly. If the changed gene represents the resistor, the value of the resistor is set to

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V1 2 1 12.000000V dc (V1=Vin=Input voltage)
V2 8 0 0.000000V dc (Node 8 denotes Iout)
V3 1 0 8.000000V dc
V4 3 0 15.000000V dc
V5 7 0 2.000000V dc
R1 2 5 100
R2 3 4 1.00K
R3 4 0 1.00K
Q1 6 4 5 QMODEL001 (Node 6 denotes Iin)

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Fig. 9 Netlist of the external circuit used to evaluate the generated circuit

be 1[KΩ]. The third mutation operation is to change the value of the device. This operation is applied only to the resistor. It changes the resistor value randomly in the range from 0 times to twice, and it chooses the nearest value within the E24 series.

In order to evaluate the generated circuit, we use the external circuit shown in Fig.9. To prevent interference with the generated circuit, the some of the nodes in the external circuit are prohibited from connecting. The nodes connections which are prohibited are 1, 2, 3, 4, 5, and 7. In this external circuit, V1 denotes the input voltage V_{in} . V2 is used as the current probe for measuring the output current I_{out} .

We define an evaluation function for the generated circuit. The function consists of three parts. First, $Score_{char}$ measures the characteristics of the generated circuit. This index signifies whether the generated circuit has the desired characteristics. If the circuit has the desired characteristics, this index indicates a high point. $Score_{char}$ is defined as

$$Score_{char} = -\frac{1}{\frac{V_{End}-V_{Start}}{V_{step}} + 1} \sum_{V_{in}=V_{Start}}^{V_{End}} \left| 1 - \frac{V_{out}(V_{in})}{V_{desired}(V_{in})} \right| \quad (1)$$

where V_{in} denotes an input voltage, and $V_{out}(V_{in})$ denotes an output voltage when the input voltage V_{in} is given. $V_{desired}(V_{in})$ denotes a desired voltage when the input voltage V_{in} is given. V_{Start} and V_{End} denote the variable range of the input voltage V_{in} , and V_{step} means the sweep step.

Second, $Score_{num}$ indicates the number of devices. If the circuit is composed of a few devices, the circuit is said to be an optimising circuit. $Score_{num}$ is defined as

$$Score_{num} = -\frac{N}{N_{max}} \quad (2)$$

where N denotes the number of devices in the generated circuit, and N_{max} denotes the maximum number of devices. In this paper, we define the maximum number as $N_{max} = 21$.

Since the characteristics of BJTs and diodes depend on the temperature, $Score_{temp}$ measures the temperature characteristic of the circuit. If this index

indicates a high point, the circuit is said to be stable under temperature change. $Score_{temp}$ is defined as

$$Score_{temp} = -\frac{(Score_{char}^{Ta=100^{\circ}C} - Score_{char}^{Ta=27^{\circ}C})^2}{(Score_{char}^{Ta=27^{\circ}C} - Score_{char}^{Ta=-46^{\circ}C})^2} \quad (3)$$

where Ta is the temperature compensating coefficient for SPICE.

Consequently, the total evaluation value $Score$ is given as

$$Score = k_1 Score_{char} + k_2 Score_{num} + k_3 Score_{temp} \quad (4)$$

where k_1 , k_2 , and k_3 are constants which satisfy the following condition.

$$k_1 + k_2 + k_3 = 1 \quad (5)$$

On the basis of the results of the SPICE simulation, the evaluation value is computed upon alternation of generation.

4. Simulation

In order to confirm the performance of the proposed automated synthesis procedure, a simple non-linear analog circuit that is a sigmoid function circuit, is generated by this system. The desired sigmoid function can be represented as

$$V_{desire}(V_{in}) = \frac{1}{1 - e^{-(V_{in}-6.0)}} [V] \quad (6)$$

The initial configuration is given as shown Table 2. In order to search for a suitable circuit topology efficiently, there should be a small number of left chromosomes upon the alternation of generations. The operation to change the length of an elastic chromosome is equivalent to fluctuating the number of devices in the circuit. This operation is also for searching for a suitable circuit topology. The number of left chromosomes is 1, and the number of elastic chromosomes is 4. Therefore, half of the chromosomes search for a suitable circuit topology, and the remainder correspond to the optimization operation for the circuit.

The initial characteristic of each device is given as shown in Table 3. The initial coefficients in the evaluation function are $k_1 = 0.9$, $k_2 = 0.0$, and $k_3 = 0.1$. If $|Score_{char}| < 0.1$ is satisfied, the coefficients are changed as $k_1 = 0.88$, $k_2 = 0.04$, and $k_3 = 0.08$. These parameters are based on empirical data. The reason coefficient k_2 increases that optimises the scale of the generated circuit. Figure 10 shows the transition of each evaluation value. The horizontal axis shows the generation, and the vertical axis shows the evaluation value.

Figure 10 indicates that the generated circuit satisfies the desired specifications when $Score_{char}$ exceeds

Table 2 Initial configuration of the simulation

Total number of chromosomes	10
Number of elastic chromosomes	4
Number of mutable chromosomes	4
Number of left chromosomes	1
Number of devices	15
Maximum number of devices	21
Minimum number of devices	1
Occurrence rate of mutation	0.6
Number of alternation of generations	15000
V_{start}	0.1 [V]
V_{end}	12.1 [V]
V_{step}	1

Table 3 Initial characteristic of each device. The transistor and the diode are described by the SPICE model.

Resistor	1 [K Ω]
Transistor	2SC1015Y or 2SC1815Y
Diode	1N4002

-0.1 at approximately 6000 generations. At this moment, $Score_{num}$ indicates -1.0. This suggests that the system is composed of 21 devices, which is the maximum number of devices for our system. After this moment, the point of $Score_{num}$ rises when changing the coefficients k_1 , k_2 , and k_3 . Figure 10 shows that $Score_{num}$ becomes -0.6 at 15000 generations. This fact suggests that the number of devices in the generated circuit is decreased by 40%, and means that the system optimises the number of devices in the generated circuit. The reason the total evaluation value $Score$ reduces at 10000 generations is that the coefficients k_1 , k_2 , and k_3 are changed. Figure 11 shows an example of a generated sigmoid function circuit which has been emerged from the simulation. Our simulation is run using WindowsXP with Intel Pentium4/2.8GHz. The calculation time of the simulation

Fig. 10 The transition of each evaluation value

Fig. 11 The generated sigmoid function circuit

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Sigmoid_function(x)
V1 2 1 12.000000V dc
V2 8 0 0.000000V dc
V3 1 0 8.000000V dc
V4 3 0 15.000000V dc
V5 7 0 2.000000V dc
R1 2 5 100
R2 3 4 1.00K
R3 4 0 1.00K
Q1 6 4 5 QMODEL001
R4 7 17 12.0
R5 0 6 4.70
D1 0 6 DMODEL001
Q2 11 0 17 QMODEL002
D2 11 0 DMODEL002
R6 17 6 360
D3 11 19 DMODEL003
R7 19 0 2.70
Q3 0 11 18 QMODEL003
R8 0 6 130
D4 11 0 DMNMODEL004
R9 6 17 1.30
R10 8 19 16.0
D5 6 0 DMODEL005
R11 8 11 62.0
.dc V1 0.100000 12.100000 1.000000
.include out000.lib
.end
```

Fig. 12 The netlist of the generated circuit

is approximately 50 hours.

Because the resistors are applied to the E24 series, it appears to have a useless part in the generated circuit, for example, two resistors are connected in parallel. However, this is the best circuit is this experiment. Note that the sigmoid function circuit is a very simple nonlinear analog circuit. Therefore, an expert of analog circuit designer could create more sophisticated circuits. The corresponding netlist of the generated circuit is shown in Fig.12, and its device model is shown in Fig.13.

The actual input-output characteristic of the generated circuit is shown in Fig.14. The horizontal axis shows an input voltage, and the vertical axis shows an output voltage. The 'actual' curve is given by the generated circuit, and the 'ideal' curve is the desired characteristic. This actual characteristic is simulated on SPICE. From this figure, it is apparent the measured characteristic fits the ideal characteristic.

Since this circuit is composed of simple discrete devices, we can easily implement the circuit as shown in

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.model QMODEL001 PNP(Is=650.6E-18 Xti=3 Eg=1.11 Vaf=115.7
+ Bf=231.7 Ne=1.829 Ise=54.81f Ikf=1.079 Xtb=1.5
+ Br=3.563 Nc=2 Isc=0 Ikr=0 Rc=.715 Cjc=14.76p
+ Mjc=.5383 Vjc=.75 Fc=.5 Cje=19.82p Mje=.3357 Vje=.75
+ Tr=111.3n Tf=603.7p Itf=.65 Vtf=5 Xtf=1.7 Rb=10)

.model DMODEL001 D(IS=1.411000e-008 RS=0.033890 N=1.984000
+ TT=4.761000e-006 CJO=5.117000e-011 VJ=0.390500
+ M=0.276200 EG=1.110000 XTI=3.000000 KF=0.000000
+ AF=1.000000 FC=0.500000 BV=100.100000 IBV=10.000000)

.model QMODEL002 PNP(Is=295.1E-18 Xti=3 Eg=1.11 Vaf=100
+ Bf=140 Ne=1.5 Ise=0 Ikf=0 Xtb=1.5 Br=10.45 Nc=2 Isc=0
+ Ikr=0 Rc=15 Cjc=66.2p Mjc=1.054 Vjc=.75 Fc=.5 Cje=5p
+ Mje=.3333 Vje=.75 Tr=10n Tf=1.661n Itf=0 Vtf=0 Xtf=0)

.model DMODEL002 D(IS=1.411000e-008 RS=0.033890 N=1.984000
+ TT=4.761000e-006 CJO=5.117000e-011 VJ=0.390500
+ M=0.276200 EG=1.110000 XTI=3.000000 KF=0.000000
+ AF=1.000000 FC=0.500000 BV=100.100000 IBV=10.000000)

.model DMODEL003 D(IS=1.411000e-008 RS=0.033890 N=1.984000
+ TT=4.761000e-006 CJO=5.117000e-011 VJ=0.390500
+ M=0.276200 EG=1.110000 XTI=3.000000 KF=0.000000
+ AF=1.000000 FC=0.500000 BV=100.100000 IBV=10.000000)

.model QMODEL003 NPN(Is=2.04f Xti=3 Eg=1.11 Vaf=6 Bf=140
+ Ne=1.5 Ise=0 Ikf=20m Xtb=1.5 Br=3.377 Nc=2 Isc=0
+ Ikr=0 Rc=1 Cjc=2p Mjc=.3333 Vjc=.75 Fc=.5 Cje=5p
+ Mje=.3333 Vje=.75 Tr=10n Tf=311.1p Itf=0 Vtf=0 Xtf=0)

.model DMODEL004 D(IS=1.411000e-008 RS=0.033890 N=1.984000
+ TT=4.761000e-006 CJO=5.117000e-011 VJ=0.390500
+ M=0.276200 EG=1.110000 XTI=3.000000 KF=0.000000
+ AF=1.000000 FC=0.500000 BV=100.100000 IBV=10.000000)

.model DMODEL005 D(IS=1.411000e-008 RS=0.033890 N=1.984000
+ TT=4.761000e-006 CJO=5.117000e-011 VJ=0.390500
+ M=0.276200 EG=1.110000 XTI=3.000000 KF=0.000000
+ AF=1.000000 FC=0.500000 BV=100.100000 IBV=10.000000)

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Fig. 13 The netlist of the generated circuit

Fig. 14 The characteristic of the generated circuit. The 'actual' curve is given by the generated circuit, and the 'ideal' curve is the desired characteristic.

Fig.15. Figure 16 shows the actual characteristic as obtained from the laboratory measurement of the implemented circuit. The actual measured characteristic fits the ideal characteristic except at the high input voltage because of the characteristic has a difference in the actual device and the device model.

Fig. 15 Example of the implemented circuit

Fig. 16 Characteristic obtained from the laboratory measurement of the implemented circuit. The horizontal axis shows V_{in} : 2[V/div]. The vertical axis shows V_{out} : 200[mV/div]. This characteristic is obtained using a Tektronix TDS3014.

5. Conclusions

We proposed an automated procedure for the synthesis of a two-port circuit which has a simple non-linear characteristic, by means of a genetic algorithm. The proposed synthesis procedure emerges the desired analog circuit topology by using the minimum number of actual discrete devices. We showed the experimental result that the system generated a sigmoid function circuit. The result has good agreement with the characteristic that has been obtained by the SPICE. Also, the actual measured characteristic of the implemented circuit fits the desired characteristic. The sigmoid function circuit is a very simple nonlinear analog circuit. Therefore, an expert analog circuit designer could create a more sophisticated circuit. However, the system can automatically create desired analog circuits without circuit design knowledge.

Our system does not require any more computa-

tional capacity than the system of Koza[1], but to develop the simple sigmoid function circuit about 50 hours is needed. Because the SPICE simulation requires a large computation capacity, the decreasing the computation capacity is problem that must be addressed in the future.

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