Material and Process for Insulation Reliable Circuitry below 2/2 μm Line/Space

Kazuyuki MITSUKURA*, Shinichiro ABE*, Masaya TOBA*, Kenichi IWASHITA**
Tomonori MINEGISHI*, Kazuhiko KURAFUCHI* and Kozo FUJIMOTO***

(Received April 18, 2018)

The ultrafine line and space (L/S) for the advanced package is required to achieve high-density interconnection between chips. The productivity and insulation reliability are the key items for fine circuit layer below 2/2 μm . In this article, we propose the trench circuitry process using high resolution photoimageable dielectric to realize highly productive copper circuitry. The trench circuitry below 2/2 μm , even 1/1 μm , was successfully demonstrated. For insulation reliability, we have studied two kinds of methods, one is the covering of exposed copper with barrier metal and the other is that with the highly insulation reliable organic material. The circuitry layer of 2/2 mm L/S, which is covered with a thin Ni layer by selective electroless plating, has passed the biased highly accelerated temperature and humidity stress test (biased-HAST) screening. We have studied the required material properties to obtain insulation reliable layer. The newly designed insulation barrier film (iBF) demonstrated high insulation reliability of 1/1 mm. Finally, we have studied the analysis method to quantify the insulation reliability and simulate the reliable L/S and the process compatibility.

Key Words: Trench Circuitry, Insulation Reliability, Photoimageable Material, Interposer

1. Introduction

Today's packaging technology requires high density connections between various kinds of devices, especially between DRAM (Dynamic Random Access Memory) and logic. To realize it, the 3D vertical integration of DRAM on logic and side by side integration using silicon interposer (2.5 D) with TSV (Through Silicon Via) have been studied. However, TSV technology faces some issues such as poor high-frequency properties and high fabrication cost. Organic interposer (2.1D) with embedded high density circuitry is one of the key solutions for the electronic package development¹⁾.

Current organic substrates fabricated by SAP (Semi-Additive Plating) technology (Fig. 1a) are limited to line/space larger than 8/8 μm because of the weak adhesion of Cu line and wire thinning and delamination during the seed etching²⁾. On the other hand, 5/5 μm line/space is required to replace the silicon interposer. Furthermore, ITRS (International Technology Roadmap for Semiconductors) says that the organic interposer will require 1/1 μm line/space in 2019³⁾. In this paper, a trench wiring method (Fig. 1b) using photoimageable dielectric (PID) was studied to realize high density interconnection⁴⁾⁻⁵⁾.

The insulation reliability below 2/2 μm line/space is one of

the key technologies to realize the fine circuitry using organic material. We demonstrate the high insulation reliable trench circuitry by covering exposed Cu line with Ni barrier metal. On the other hand, there are many articles about insulation reliability and the copper migration mechanism⁶⁾⁻⁸⁾. However, the required material properties for fine circuitry are not discussed. In this paper, we have evaluated insulation reliability below 5/5 μm using various kinds of materials and studied the required

Fig. 1 Process flow of conventional Semi-additive process (a) and proposed trench process (b).

* 日立化成株式会社 パッケージングソリューションセンタ (〒 300-4247 茨城県つくば市和台 48)
Packaging Solution Center, Hitachi Chemical Co., Ltd (Wadai 48, Tsukuba-shi, Ibaraki 300-4247, Japan)

** 日立化成株式会社 (〒 300-4247 茨城県つくば市和台 48)
Hitachi Chemical Co., Ltd (Wadai 48, Tsukuba-shi, Ibaraki 300-4247, Japan)

*** 大阪大学大学院工学研究科 (〒 565-0871 吹田市山田丘 2-1)
Graduate School of Engineering, Osaka University (2-1, Yamada-oka, Suita, Osaka 565-0871, Japan)

material properties to pass biased HAST for 200 h. We also report the simulation method of insulation reliability and process compatibility.

2. Fabrication structure and experimental materials

The developed photoimageable dielectric (PID) is chemically amplified- type negative tone to fabricate below $2/2\ \mu\text{m}$. The material was formed on 200 mm silicon wafers. The samples were exposed with broadband light from high pressure Hg ramp. After the exposure, the wafers were baked at 85°C for 4 min and then developed with 2.38% tetra-methyl ammonium hydroxide (TMAH) solution for 50 s. The samples were cured at 180°C for 1 h. For the evaluation of photolithographic property, the $3\ \mu\text{m}$ or $2\ \mu\text{m}$ thick PID was formed on the above cured sample. The wafers were exposed with i-line stepper. After the exposure, the samples were baked at 85°C for 4 min and then were developed with 2.38% TMAH solution for 50 s. The samples were cured at 180°C for 1 h. 50 nm thick titanium and 100 nm thick copper were formed on trench patterns by a sputtering process and filled with electro-plated copper. The embedded traces were exposed by copper removal process. **Fig. 2** shows the assembly process flow.

We designed the test element group (TEG) to evaluate biased HAST as shown in **Fig. 3**. The obtained trench wiring layers were covered with cured materials having different moisture absorption rates and anion impurities as shown in **Fig. 4**. The condition of biased HAST was 130°C , 85%RH and 3.3 V. The criteria of insulation reliability is electrical resistance over $10^7\ \Omega$. Cu

migration was observed by STEM-EDX (Scanning transmission electron microscope energy dispersive x-ray spectrometry).

The moisture absorption rates of the resins were measured as follows. The $30\ \mu\text{m}$ thick cured resins on silicon wafer were put in the condition of 85%RH at 130°C for 200 h. The samples were taken out from the chamber at 40°C . The weight loss rate at 100°C was measured as the moisture absorption rate by thermal gravimetric analysis. N_2 flow rate and temperature rising rate were 400 mL/min and $10^\circ\text{C}/\text{min}$. The amount of anion impurities in the resins were measured as follows. The cured resins in ultra-pure water were put in the oven at 130°C for 5 h. Each water extracts after filtration was evaluated by ion chromatography. The detected anions were chloride ion, sulfate ion, phosphate ion, fluoride ion, bromide ion, nitrate ion and nitrite ion.

The relationship between $\ln V/S$ which is logarithm of electric field strength and $\ln t$ which is insulation retention time as shown in formula (1) was reported⁹⁾. We quantified and analyzed the insulation reliability about fine circuitry obtained from biased HAST evaluation.

3. Fabrication of fine trench circuitry

Fig. 5 shows the cross-sectional scanning electron microscope (SEM) images of $5/5\ \mu\text{m}$, $2/2\ \mu\text{m}$ and $1/1\ \mu\text{m}$ patterns obtained by lithography. The PID shows excellent resolution without any residue and footing in each pattern size. The trench wiring layers below $5/5\ \mu\text{m}$ were fabricated by sputtering, copper plating and copper removal process. **Fig. 6** shows the surface overviews and cross-sectional SEM images of $5/5\ \mu\text{m}$, $2/2\ \mu\text{m}$ and $1/1\ \mu\text{m}$ circuitries. We successfully fabricated the wiring below $5/5\ \mu\text{m}$

Fig. 2 Assembly process flow of trench wiring layer

Fig. 3 TEG design to evaluate biased HAST.

Table 1 TEG design scales for biased HAST.

Line/Space	5/5	2/2	1/1
a	30	30	30
b	100	100	100
c	2000	2000	2000
d	1000	1000	1000
e	3000	3000	3000
f	100	100	100

Unit: μm

Fig. 4 Schematic structure for biased HAST evaluation

Fig. 5 Cross-sectional SEM images of 5/5, 2/2 and 1/1 μm pattern using PID.

Fig. 6 Surface overviews and cross-sectional SEM images of trench circuitry with 5/5, 2/2 and 1/1 μm .

Fig. 7 Surface roughness of copper line and PID.

without delamination and electrical shorting. The surface of the circuit layer shows smooth roughness (R_a) below 30 nm as shown in **Fig. 7**, which is the advantage for multi-layer fabrication.

4. Insulation reliable trench circuitry by barrier metal

Insulation reliability is the largest challenge to be solved for fine L/S using organic materials. To satisfy insulation reliability, the exposed copper trace was covered with the thin barrier metal by 100 nm Ni-P electroless plating, which is compatible with wafer as well as substrate processes and enables high selective coverage on copper¹⁰⁾. The Ni-P on copper line was expected to form passivation layer by oxidation and prevent the copper migration. The electrical resistance of 2/2 μm circuitry after 200 h was over $10^7 \Omega$ as shown in **Fig. 8**. **Fig. 9** shows the elemental mapping of the area around the 2/2 μm after 250 h biased HAST using STEM-EDX. The titanium is one of the elements of seed layer and the nickel is a barrier metal on copper trace. The carbon

Fig. 8 Electrical resistance changes of 2/2 μm circuitry during biased-HAST.

Fig. 9 Cross-sectional STEM view and C, Ti, Ni and Cu elemental mapping by EDX after biased-HAST over 200 h of 2/2 μm circuitry covered with Ni barrier.

element mapping was reasonably explained by organic material. Copper elemental mapping indicates no electrical migration during biased HAST. On the other hand, the anode Cu wiring without Ni-P barrier metal was eluted after biased HAST as shown in **Fig. 10**. From these results, we have verified that the trench circuitry covered with barrier metal has excellent insulation reliability.

5. Material property for insulation reliable circuitry

Fig. 11 shows the schematic structure for evaluation of insulation reliability (a), the schematic copper migration mechanism (b) and chemical reaction on cathode, anode electrode and in the resin (c). On the cathode electrode, the acid is generated by electrolysis of the water included in resin, and then the copper is eluted. The copper elution is accelerated in low pH condition. In the resin, the copper is migrated from cathode to anode by repeating the salt formation of eluted copper and anion impurities in the resin and copper re-ionization. On the anode electrode, the copper is deposited from migrated copper ion by receiving electron. From these results, the electrical resistance of line-to-

Fig. 10 Cu elemental mapping by EDX after biased-HAST over 200 h of 2/2 μm circuitry without Ni barrier.

Fig. 11 Schematic structure for evaluation of insulation reliability (a), copper migration mechanism (b) and chemical reaction on cathode, anode electrode and in the resin (c)

Fig. 12 Influence of moisture absorption rate on insulation reliability. The anion concentrations are 1000 ppm approximately.

line becomes low⁶⁻⁸⁾. Therefore, it is assumed that the moisture absorption rate and the amount of anion impurities impact on the insulation reliability.

We evaluated the biased HAST of several kinds of materials having different moisture absorption rates and anion impurities to clarify the material criteria. **Fig. 12** shows the influence of moisture absorption rate on the insulation reliability of 5/5 μm and 2/2 μm . The anion concentrations in this figure are 1000 ppm approximately. To pass insulation reliability of 5/5 μm , the material criteria is moisture absorption rate below 1.4%

Fig. 13 Influence of anion concentration on insulation reliability. The rates of moisture absorption are below 0.3%.

and anion impurities below 1000 ppm. In the case of 2/2 μm , the all evaluated materials broke down within 50 h because of high anion impurities. **Fig. 13** shows the influence of anion concentration on insulation reliability of 5/5 μm and 2/2 μm . The rates of moisture absorption in this figure are below 0.3%. The 5/5 μm circuitry passed biased HAST over 200 h. In the case of 2/2 μm , the amount of anion impurity strongly influences on the insulation reliability. The correlation coefficient from exponential approximation was 0.9988, which value indicated reliable analysis result. It is assumed that the mobility of Cu ion became main factor for insulation reliability because the low moisture absorption rate caused low Cu ion elution from cathode. To pass biased HAST of 2/2 μm , the material criteria is moisture absorption rate below 0.3% and anion impurities below 200 ppm.

6. Reliability evaluation of circuitry using iBF

We have newly designed the insulation barrier film (iBF) to achieve insulation reliability of 1/1 μm circuitry. The features of iBF are lower moisture absorptivity than 0.3%, lower anion impurity than 100 ppm and high resistance to hydrolysis. **Fig. 14** shows the electrical resistance changes of 1.5/1.5 μm and 1/1 μm using iBF. The electrical resistance kept over $10^7 \Omega$ for 200 h as our criteria. **Fig. 15** shows the overview of 2/2 μm circuitry using iBF before (a) and after (b) biased HAST for 300 h. The circuitry was not much changed before and after biased-HAST. **Fig. 15** shows the elemental mapping of the area around the 2/2 μm line/space after 300 h biased HAST. The titanium and the carbon element mapping are reasonably assigned as the seed layer, and the PID and iBF, respectively. The copper elemental mapping indicates no electrical migration under biased HAST condition. From these results, iBF showed excellent insulation reliability on 2/2 μm , 1.5/1.5 μm and 1/1 μm .

7. Analysis and simulation of insulation reliability

The analysis and simulation of insulation reliability is expected as the indicator for material development. We quantified the insulation reliability from biased HAST results of 10/10, 5/5, 3/3,

Fig. 14 Electrical resistance changes of 1.5/1.5 μm (a) and 1/1 μm (b) trench wiring covered with iBF during biased HAST.

Fig. 15 Overview of 2/2 μm circuit covered with iBF before (a) and after (b) biased-HAST over 200 h.

2/2 μm . **Fig. 17** shows the relationship between $\ln V/S$ and $\ln t$ to compare the impacts of materials (a) and the structures with or without Ni barrier (b). The plots on the straight line indicated quantitative results. **Table 2** summarizes the activation energy (E_a) calculated from y-intercept. The E_a value of iBF shows 1.5 times more than Material A and quantitatively verified the high insulation reliability by the decrease of moisture absorption rate and anion impurities. The E_a value of sample with Ni barrier is also 1.5 times more than without Ni. **Table 3** shows the insulation reliable L/S. The simulation of iBF indicates insulation reliable 0.9/0.9 μm circuitry and actual experimental data shows biased-HAST over 200 h in 1/1 μm circuitry. On the other hand, the simulation with Ni barrier indicates insulation reliable 1/1 μm circuitry. However the biased-HAST of 1/1 μm circuitry failed within 50 h. We observed the Ni bridges between Cu lines and revealed to need the process optimization. This quantification method of the insulation reliability is useful for not only the simulation of insulation reliability but the indicator of process compatibility.

Fig. 16 Cross-sectional STEM view and elemental mapping of C, Ti and Cu by EDX after biased HAST over 200 h using iBF.

Fig. 17 Relationship between $\ln E$ and $\ln t$ of Material A ~ D, and iBF (a), and with or without Ni barrier on Cu line (b).

8. Conclusion

The highly insulation reliable circuitry of 1/1 μm has successfully been developed. The developed photosensitive dielectric has demonstrated 1/1 μm line/space. The trench circuitry with Ni barrier showed excellent insulation reliability. We have studied the required material properties for insulation reliability.

Table 2 Calculated Ea of Material A ~ D, iBF and Ni barrier on Cu.

Material	Material A	Material B	Material C	Material D	iBF	Ni barrier
Ea (eV)	0.33	0.36	0.40	0.47	0.49	0.49

Table 3 Calculated insulation reliable L/S.

Material	Material A	Material B	Material C	Material D	iBF	Ni barrier
L/S (μm)	> 20/20	16/16	7/7	3/3	0.9/0.9	1/1

The material criteria of 5/5 μm to pass the insulation reliability is the moisture absorption rate below 1.4% and anion impurities below 1000 ppm. In the case of 2/2 μm, the material criteria is moisture absorption rate below 0.3% and anion impurities below 200 ppm. The newly designed insulation barrier film (iBF) has achieved excellent insulation property. We also have revealed the analysis method to quantify the insulation reliability and simulate the reliable L/S and the process compatibility.

Reference

- 1) Y. Fukuzaki, M. Badaroglu, "More Moore landscape for IoT world – ITRS2.0 requirement," ICEP-IAAC 2015 proceeding.
- 2) Y. H. Chen, S. L. Cheng, D. C. Hu, T. J. Tseng, "Ultra-thin line embedded substrate manufacturing for 2.1D/ 2.5D SiP application," ICEP-IAAC 2015 Proceeding
- 3) ITRS (International technology roadmap for semiconductors) 2012 Update, Table AP10 and INTC2
- 4) K. Mitsukura, M. Toba, K. Urashima, K. Iwashita, T. Minegishi, K. Kurafuchi, "Proposal of ultra-fine and high reliable trench wiring process for organic interposer," Journal of Microelectronics and Electronic Packaging, **14** (2017) 26-31.
- 5) K. Mitsukura, M. Toba, K. Urashima, K. Iwashita, T. Minegishi, K. Kurafuchi, "Proposal of ultra-fine and high reliable trench wiring process for organic interposer," Proceedings of The International Microelectronics and Packaging Society, 2016.
- 6) A. Dermarderosian, "The electrochemical migration of metals," Proceedings of International Society of Hybrid Microelectronics Symposium, 1978
- 7) G. Ripka, G. Harsanyi, "Electrochemical Migration in Thick Film ICs," Electrocomponent Science and Technology, **11** (1985) 281-290.
- 8) G. Harsanyi, "Dendritic Growth from Dielectric Constituents: a Newly Discovered Failure Mechanism in Thick Film ICs," International Journal of Microcircuits and Electronic Packaging, **16** [3] (1993) 207-216.
- 9) T. Tsukui, "Insulation deterioration and the prevention method by electrochemical migration by electric equipment," Journal of Japan Institute of Electronics Packaging, **8** (2005) 523-530.
- 10) F. Chen, E. Huang, M. Shinosky, M. Angyal, T. Kane, Y. Wang, A. Kolics, "A comparative study of ULK conduction mechanisms and TDDDB characteristics for Cu interconnects with and without CoWP metal capat 32 nm technology," IITC2010

Mail Address

Kazuyuki MITSUKURA k-mitsukura@hitachi-chem.co.jp