Mesh Zoning Method for Electro – Thermal Analysis of Submicron Si MOSFET

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Abstract
The results of electro – thermal analysis, which is widely known as hydrodynamic model, are strongly dependent on the mesh size of model. However, the theory and method of accurate mesh size have not investigated. In this paper, we presented the calculation errors caused by the mesh size by using several mesh size models. The calculation results show that the mesh size for lateral direction, i.e. direction from the source electrode to the drain electrode in MOSFET, does not strongly affect the calculated characteristics of MOSFET. On the other hand, the calculation results strongly depend on the mesh size for vertical direction, i.e. direction from the gate oxide to the bottom surface in MOSFET. Here, we proposed the mesh zoning method for electro – thermal analysis, which was derived from the theory of the semiconductor physics. The calculation results with our mesh zoning method showed good accuracy compared to the results of the fine mesh. Since the mesh zoning means the reduction of mesh number, as a result, our mesh zoning method could reduce the calculation time by at least 30 times.

Key words: Mesh Zoning Method, Electro – Thermal Analysis, Submicron Si MOSFET, Debye Length

1. Introduction

The process size of semiconductor devices has reached the range of sub-100 nm length scale. The report of ITRS ’05(1) has originally predicted that 65 nm process would be realized in 2007. LSI (Large Scale Integration) is the most important part in the electrical devices, and mainly consists of Si MOSFETs (Metal-Oxide-Semiconductor Field Effect Transistors). The development of manufacturing process of semiconductor devices leads to the miniaturizing of Si MOSFETs, resulting to the increase of the MOSFETs density in LSI. Due to the increase of the heat dissipating devices in the LSIs, thermal problem will be a major task for packaging community. Due to the decrease of the device feature size, new type of thermal problem, submicron scale local hot spot, may become important. The local hot spot is a high temperature region within the heat dissipating devices, and is already prominent for semiconductor devices with lower thermal conductivities. Due to the decrease in device feature size and multilayer structures, this too, may become important for future silicon devices. The key idea to tackle this problem is to precisely predict the heat dissipation distribution in the devices, and for this purpose, one must consider the behavior of electrical as well as thermal characteristics(2). To consider the behavior of the electrical and the thermal characteristics of semiconductor devices, electro – thermal analysis, which is widely known as hydrodynamic model, is considered as attractive(3)(4) and widely used technique. However, the calculation accuracy of this analysis strongly depends on the mesh size of model.
size of the calculation model. For instance, considering the inversion layer of Si MOSFET, the carrier density has an abrupt change and the mesh size has to be taken care of because the device characteristics strongly depend on the inversion carrier density. However, the theory and method of accurate mesh size has not yet been investigated. One literature proposed to use the mesh size normalized by Debye length for accurate calculation (5), and proved to be quite useful information to what mesh size has to be used for accurate calculation. However, the mesh zoning method was not yet proposed.

In this paper, we presented the mesh size dependence of calculation results and propose the mesh zoning method for electro-thermal analysis, which was derived from the theory of the semiconductor physics. The model of Si MOSFET and governing equations are presented, then the calculation results are compared by using various uniform mesh sizes, and subsequently the importance of accurate mesh size is discussed. Finally, we proposed the mesh zoning method and discussed the accuracy of our method.

2. Modeling

Figure 1 shows the modeled Si MOSFET structure for numerical calculations. In this work, we focused on n-type Si MOSFET. The gate length, \( L_g \), is 90 nm and p-doped substrate with doping concentration of \( N_A = 2 \times 10^{23} \text{ m}^{-3} \) is considered. Each area underneath the source and drain electrode is highly n-doped at \( N_D = 1 \times 10^{25} \text{ m}^{-3} \). Due to the ion doping followed by annealing process, the highly doped region is modeled to have uniform distribution of \( N_D \). The highly doped thickness, \( X_j \), is 80 nm and the thickness of the gate oxide, \( t_{ox} \), is 2 nm. Applied bias condition is that the source electrode is grounded, and 1.0 V is applied to the gate and drain electrode.

We will especially focus on the channel region under the gate oxide. For convenience, the origin point of coordinate is set under the gate oxide at source side as shown in Fig. 1(b).

3. Governing Equations

Electrical current causes heat generation. The carriers (electrons and holes) accelerated by high electric field acquire high energy, and they transfer their energy to the crystal lattice. In the high electric field, the carrier temperature is much higher than the lattice temperature. Such carrier is called a “hot carrier”. Thus to analyze the thermal and electrical behavior of the devices, it is important to consider the case when the carrier temperatures are not equivalent to the lattice temperature.

The set of governing equations of MOSFET is composed of Poisson equation, the continuity equations for electrons and holes, the momentum conservation equations for
electrons and holes and the energy conservation equations for electrons, holes and the crystal lattice. The details of these equations are shown below. 

\[
\nabla^2 \phi = -\frac{q}{\varepsilon_r} (N_D - n - N_A + p) \\
\frac{\partial n}{\partial t} \frac{\nabla \cdot (n \mathbf{v}_e)}{N_s} = -R \\
\frac{\partial p}{\partial t} \frac{\nabla \cdot (p \mathbf{v}_h)}{N_s} = -R \\
-qn \nabla \phi + \nabla (nk_e T_e) = -\frac{nm_e^*}{\tau_{me}} \\
\frac{q \nabla \phi + \nabla (pk_t T_k)}{\tau_{mth}} = -\frac{pm_h^*}{\tau_{mth}} \\
\frac{\partial W_e}{\partial t} + \nabla \cdot (\mathbf{v}_e W_e) + qn \mathbf{v}_e \nabla \phi + \nabla \cdot (n \mathbf{v}_e nk_e T_e) - \nabla \cdot (k_e \nabla T_e) = -\frac{W_e - W_{th_e}}{\tau_{e-t}} \\
\frac{\partial W_h}{\partial t} + \nabla \cdot (\mathbf{v}_h W_h) + qn \mathbf{v}_h \nabla \phi + \nabla \cdot (n \mathbf{v}_h pk_h T_h) - \nabla \cdot (k_h \nabla T_h) = -\frac{W_h - W_{th_h}}{\tau_{h-t}} \\
\n\]

Equation (1) is Poisson equation, where \( \phi, q, \varepsilon_r, n \) and \( p \) are electrical potential, elementary charge, permittivity of silicon, electron density and hole density respectively. \( \phi \) is calculated from this equation. Equations (2) and (3) are the continuity equation for elementary charge, permittivity of silicon, electron density and hole density respectively. Shockley-Read-Hall (SRH) generation/recombination, impact ionization and Auger recombination are considered. Details of these equations are shown below. 

\[ R_{SRH} = \frac{np - n_i^2}{\tau_{SRH-h} (n + n_i) + \tau_{SRH-e} (p + n_i)} \]

\[ \tau_{SRH-h} = \frac{\tau_{0-h}}{1 + \frac{N_D}{N_e}} \]

\[ \tau_{SRH-e} = \frac{\tau_{0-e}}{1 + \frac{N_A}{N_h}} \]

\[ R_g = 5.044 \times 10^4 \left[ n \left( 1 + \frac{u_e}{2} \right) \text{erfc} \left( \frac{1}{\sqrt{u_e}} \right) \right] \left[ p \left( 1 + \frac{u_h}{2} \right) \text{erfc} \left( \frac{1}{\sqrt{u_h}} \right) \right] \]

\[ u_e = k_B T_e / E_{th_e} \]

\[ u_h = k_B T_h / E_{th_h} \]

\[ n_{eff} = \sqrt{2 \pi} \frac{m_e^*}{\hbar^2} (m_e^* m_t^* T_e) \frac{1}{\sqrt{u_e}} \exp \left( -\frac{E_g}{2k_B T_e} \right) \]

\[ p_{eff} = \sqrt{2 \pi} \frac{m_h^*}{\hbar^2} (m_h^* m_t^* T_h) \frac{1}{\sqrt{u_h}} \exp \left( -\frac{E_g}{2k_B T_h} \right) \]

\[ R = R_g + R_{SRH} \]

In Eq. (9), \( n_e \) denotes intrinsic carrier density. \( \tau_{SRH-h} \) and \( \tau_{SRH-e} \) represent carrier lifetimes depending on doping density, which are defined by Eqs. (9)-a and (9)-b. \( \tau_0 \) is 3.95 × 10^{-4} s and \( \tau_{0-h} \) is 3.52 × 10^{-4} s. \( N_e \) and \( N_h \) are 7.1 × 10^{21} m^{-3}. In Eq. (10), \( k_B, T_e, T_h, m_e^* \) and \( m_h^* \) represent Boltzmann constant, electron temperature, hole temperature, effective mass of electron and effective mass of hole respectively. \( E_{th} \) is the threshold energy of impact
ionization for silicon and we use 1.31 eV (2.10 × 10^-19 J). (10) \( E_G \) is the energy band gap of silicon and \( h \) is Planck constant.

Equations (4) and (5) denote the momentum conservation equation for electrons and holes respectively. \( \tau_{me} \) and \( \tau_{mh} \) denote the momentum relaxation time for electrons and for holes respectively. By using the relationship \( \mu_{e,h} = q \tau_{me,h} / m_{e,h} \), these equations become the definition of electrons and holes current (details are shown later, Eq. (31)), where \( \mu \) is mobility. In this work, we use the electron and hole mobility instead of electron and hole effective mass and we assume that electron and hole mobility dependent on lattice temperature, impurity density and electric field (8).

Equation (6) is the energy conservation equation for electrons. The electron temperature, \( T_e \), is obtained from this equation. The thermal conductivity of electrons, \( \kappa_e \), is given as (11)

\[
\kappa_e = \frac{2k_B^2 n_e \tau_{me} T_e}{m_e} \quad (12)
\]

The energy of electrons, \( W_e \), is given as

\[
W_e = \frac{3}{2} n k_B T_e + \frac{1}{2} m_e^* v_e^2 \quad (13)
\]

and the electron energy at the equilibrium state, \( W_{eo} \), is defined as

\[
W_{eo} = \frac{3}{2} n k_B T_L \quad (14)
\]

where \( T_L \) is lattice temperature. There are many values proposed for the energy relaxation time of electrons \( \tau_{e-L} \) (12) – (15), \( \tau_{e,L} \), and here it is given by a constant value of \( \tau_{e-L} = 0.30 \) ps. Equation (7) is the energy conservation equation for holes. The hole temperature, \( T_h \), is obtained from this equation. The thermal conductivity of holes, \( \kappa_h \), is given as

\[
\kappa_h = \frac{2k_B^2 p \tau_{mh} T_h}{m_h} \quad (15)
\]

The energy of holes, \( W_h \), is given as

\[
W_h = \frac{3}{2} p k_B T_h + \frac{1}{2} p m_h^* v_h^2 \quad (16)
\]

And the hole energy at the equilibrium state, \( W_{ho} \), is given as

\[
W_{ho} = \frac{3}{2} p k_B T_L \quad (17)
\]

There are also several values proposed for the energy relaxation time for holes \( \tau_{h-L} = 0.30 \) ps. Equation (8) is the energy conservation equation for crystal lattice. Prior research reported that the temperature difference between acoustic and optical phonon is relatively small \( \tau_{h-L} \) even if the gate length is 90 nm (17). Therefore, Fourier’s law is applied in Eq. (8). The thermal conductivity of silicon is given as (8)

\[
\kappa_L = 154.86 \times \left( \frac{T_L}{300} \right)^{\frac{4}{3}} \quad (18)
\]

From Eq. (8), the lattice temperature, \( T_L \), is calculated.

4. Boundary Condition

For electrical potential, the source electrode is grounded \( (V_S = 0.0 \) V) and the drain voltage is given as constant \( V_D = 1.0 \) V. Under the gate oxide, the equation derived from Gauss’s law is applied as

\[
\varepsilon_{ox} \nabla \phi_{ox} = \varepsilon_c \nabla \phi_L \quad (19)
\]

where \( \varepsilon_{ox} \) means permittivity of silicon oxide. The rest of the boundary has zero gradient of potential as boundary condition.

For carrier density, constant value of \( N_D \) is given at both the source and the drain
electrode interfaces. Zero gradient boundary condition of carrier normal to the boundary is given at rest of boundary.

For carrier velocity, the velocity is set to zero in the perpendicular direction to the boundary except under the source and drain electrode.

For carrier temperature, constant temperature, $T_c = T_h = 350$ K, is assumed at the bottom surface. At the source and drain electrode, it is assumed that the carrier temperature and the lattice temperature are same value. Adiabatic boundary condition is applied to other boundaries.

For lattice temperature, constant temperature, $T_L = 350$ K, is assumed at the bottom surface, and adiabatic boundary condition is applied to other boundaries.

Most of the physical properties and constants are taken from standard literature. (18)

5. Results and Discussion

As mentioned previously, the mesh size of device characteristics simulation is quite important because the calculation results strongly depend on the mesh size. In this section we consider the influence of mesh size to the calculation results. At first, we simulated the characteristics of MOSFETs (structure was shown in Fig. 1) by using different mesh sizes. According to semiconductor physics, Debye length is most important length scale to determine the characteristics of a semiconductor. (18) If the mesh size is shorter than Debye length, the calculation results is not deviated from physical characteristics and this Debye length is calculated from the impurity density at the substrate of MOSFET. Thus, the smaller the mesh size, the better the calculation accuracy. In this work, we used four mesh sizes considering Debye length calculated from the impurity carrier density at the substrate. (5) Debye length is calculated from the following equation.

$$ L_D = \sqrt{\frac{k_B T_e \varepsilon_s}{q^2 N_A}} \quad (20) $$

Also in this work, impurity carrier density at the substrate is taken to be $2 \times 10^{23}$ m$^{-3}$. Assuming $T_L = 350$ K, Debye length is calculated to be $9.94 \times 10^{-9}$ m. For lateral direction (x direction in Fig. 1 (b)), $\Delta x$ is defined to be 1.0 nm, 2.5 nm, 5.0 nm and 10 nm. Similarly, for vertical direction (y direction in Fig. 1 (b)), $\Delta y$ is meshed to be also 1.0 nm, 2.5 nm, 5.0 nm and 10 nm. The case where $\Delta x$ and $\Delta y$ is 1.0 nm is what we defined it as ‘fine mesh’.

Mesh size for lateral direction

First, we consider the mesh size dependence of the calculation results for lateral direction (x direction in Fig. 1 (b)). In this part, the mesh size for vertical direction (y direction in Fig. 1 (b)) is uniformly set to 1.0 nm and that for the lateral direction is uniformly varied to 1.0 nm, 2.5 nm, 5.0 nm or 10 nm. In other words, $\Delta x \times \Delta y$ are 1.0 nm $\times$ 1.0 nm, 2.5 nm $\times$ 1.0 nm, 5.0 nm $\times$ 1.0 nm and 10 nm $\times$ 1.0 nm.

Table 1 shows the results of the drain current, $I_D$, and the maximum lattice temperature, $T_L$ max, of each mesh size. $\Delta I_D$ means the difference ratio compared to the drain current of fine mesh (1.0 nm $\times$ 1.0 nm) and $\Delta T_L$ max means the difference ratio compared to the maximum lattice temperature of fine mesh. From this table, it can be seen that the difference of the drain current density is 0.15 % if comparison is done to the results of $\Delta x = 1.0$ nm mesh and $\Delta x = 2.5$ nm mesh, 0.75 % for $\Delta x = 1.0$ nm and $\Delta x = 5.0$ nm, and 2.47 % for $\Delta x = 1.0$ nm and $\Delta x = 10$ nm. The difference of the maximum lattice temperature is 0.05 % if comparison is done to the results of $\Delta x = 1.0$ nm and $\Delta x = 2.5$ nm, 0.16 % for $\Delta x = 1.0$ nm and $\Delta x = 5.0$ nm, and 0.41 % for $\Delta x = 1.0$ nm and $\Delta x = 10$ nm.

Figure 2 (a) shows the results of electron density distribution below the gate oxide at the drain side (pinch-off region) and Fig. 2 (b) shows the results of lattice temperature distribution below the gate oxide. From Fig. 2 (a), it can be shown that the electron density
abruptly decreased at the pinch-off region, which is untraceable if larger mesh is used. However, the difference of the drain current is only 0.75 % by using $\Delta x = 5.0$ nm mesh and that is 2.47 % even if $\Delta x = 10$ nm mesh is used. In Fig. 2 (b), the local hot spot appears at the same position at any mesh size. And from Table 1, the difference of the maximum lattice temperature is 0.41 % even if $\Delta x = 10$ nm mesh is used. These mean that the mesh size for lateral direction does not strongly influence the calculation results.

**Table 1  Drain current and maximum lattice temperature of each mesh size**

<table>
<thead>
<tr>
<th>Mesh size (nm)</th>
<th>$I_D$ [mA/mm]</th>
<th>$\Delta I_D$ [%]</th>
<th>$T_{L_{max}}$ [K]</th>
<th>$\Delta T_{L_{max}}$ [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>1337</td>
<td>-</td>
<td>364.7</td>
<td>-</td>
</tr>
<tr>
<td>2.5</td>
<td>1335</td>
<td>0.15</td>
<td>364.5</td>
<td>0.05</td>
</tr>
<tr>
<td>5.0</td>
<td>1327</td>
<td>0.75</td>
<td>364.1</td>
<td>0.16</td>
</tr>
<tr>
<td>10</td>
<td>1304</td>
<td>2.47</td>
<td>363.2</td>
<td>0.41</td>
</tr>
</tbody>
</table>

Fig. 2  Distribution in the channel region of MOSFET

**Mesh size for vertical direction**

Next, we consider the influence of the mesh size on calculation results for vertical direction ($y$ direction in Fig. 1). In this part, the mesh size for lateral direction is uniformly set to $\Delta x = 1.0$ nm and that for the vertical direction is uniformly varied to $\Delta y = 1.0$ nm, 2.5 nm, 5.0 nm or 10nm.

Table 2 shows the value of drain current and the maximum lattice temperature at each mesh size. The drain current is 1337 mA/mm in the case of $\Delta y = 1.0$ nm and 927 mA/mm in case of $\Delta y = 2.5$ nm, and the difference between these results is 30.7 %. The drain current is 683 mA/mm and 533 mA/mm in the case of $\Delta x = 5.0$ nm and $\Delta x = 10$ nm respectively. The difference if comparison is done to the results of $\Delta y = 1.0$ nm is 48.9 % and 60.1 % in the case of $\Delta y = 5.0$ nm and $\Delta y = 10$ nm mesh respectively. The maximum lattice temperature is 364.7 K in the case of $\Delta y = 1.0$ nm but 359.8 K in the case of $\Delta y = 2.5$ nm. Comparing these results, 1.34 % difference exists and the absolute value differs by about 5 K.

**Table 2  Drain current and maximum lattice temperature of each mesh size**

<table>
<thead>
<tr>
<th>Mesh size (nm)</th>
<th>$I_D$ [mA/mm]</th>
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<th>$T_{L_{max}}$ [K]</th>
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<tbody>
<tr>
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<td>-</td>
<td>364.7</td>
<td>-</td>
</tr>
<tr>
<td>2.5</td>
<td>927</td>
<td>30.7</td>
<td>359.8</td>
<td>1.34</td>
</tr>
<tr>
<td>5.0</td>
<td>683</td>
<td>48.9</td>
<td>356.9</td>
<td>2.14</td>
</tr>
<tr>
<td>10</td>
<td>533</td>
<td>60.1</td>
<td>354.7</td>
<td>2.74</td>
</tr>
</tbody>
</table>
Figure 3 shows the electron density distribution for vertical direction. Fig. 3 (a) shows the results at x = 20 nm, i.e. the results at the source side, and Fig. 3 (b) shows the results at x = 80 nm (drain side). In Fig. 3 (a), electron densities at the source side underneath the gate oxide (y → 0 nm) is about $1 \times 10^{25}$ m$^{-3}$ and abruptly decreasing until around y = 20 nm. This part represents the electron channel. Then the electron densities gradually decrease toward the bottom surface of the device (y = 300 nm). However, the result of wider mesh size underestimates the carrier density in whole region. The electron density in the substrate strongly depends on the mesh size. In Fig. 3 (b), the electron densities underneath the gate oxide show quite similar values. But the values of electron density are smaller than the x = 20 nm case because x = 80 nm means the pinch-off region in the electron channel. And the electron densities in the substrate strongly depend on mesh size as well as at the source side.

From these results, the mesh of $\Delta y = 1.0$ nm is needed for vertical direction. In the present work, the mesh size of 1.0 nm has two different significance: the first means a size 10 times shorter than Debye length, which is calculated from the substrate impurity density, and the other is discussed in later sections.

Debye length determines the distance over which a small unbalanced charge decays and is derived as below.\(^{(18)}\)

Considering only y direction, current continuity equation of semiconductor devices is

$$\frac{\partial n}{\partial t} + \frac{1}{q} \frac{\partial (J_y)}{\partial y} = 0 \quad (21)$$

In the case that there is the small local fluctuation of the majority carriers from the uniform equilibrium concentration, $n_0$, the locally created space-charge density is $n - n_0$.

From the Poisson equation, locally created electrical field is

$$\frac{\partial E_y}{\partial y} = -\frac{q(n-n_0)}{\varepsilon_y} \quad (22)$$

and electron current is

$$J_y = \epsilon E + \mu_e k_B T_i \frac{\partial n}{\partial y} + q n_0 \mu_i E + \mu_e k_B T_i \frac{\partial n}{\partial y} \quad (23)$$

where $E$ and $\sigma$ means electric field and the electrical conductivity respectively.

Assuming $\sigma$ is constant and $T_i$ is uniform, the following equation can be obtained.

$$\frac{\partial n}{\partial t} + \frac{\sigma(n-n_0)}{q} \frac{\partial (J_y)}{\partial y} + \frac{\mu_e k_B T_i}{q} \frac{\partial^2 n}{\partial y^2} = 0 \quad (24)$$

For spatial response, by using the boundary condition that $n = n_0$ at $y \to \infty$, the solution of Eq. (24) becomes

$$n - n_0 = (n-n_0)|_{y=0} \exp(-y/L_D) \quad (25)$$

where $L_D$ is the Debye length, which is now becomes

$$L_D = \frac{\varepsilon_y k_B T_i}{q n_0} \quad (26)$$
In above discussion, the electrical conductivity, $\sigma$, is determined by $n_0$. However, the electrical conductivity strongly depends on the local carrier density especially for channel region of MOSFET, where majority carrier has higher density than the impurity. Therefore, the electrical conductivity must be defined by the channel carrier density under the gate oxide of MOSFET. Furthermore, current flow in the semiconductor is determined by the gradient of the carrier temperature. Considering these things (details are described later), Debye length changes from original form to

$$L_D^* = \frac{\varepsilon_s k_B T_e}{q n^*}$$

(27)

where $n^*$ is channel carrier density and $n^*$ is about $1 \times 10^{25}$ m$^{-3}$ in the present work. This results to the Debye length under at the channel region of MOSFET becomes $1.4 \times 10^9$ m. The Debye length determines the distance over which an unbalanced charge decays, and here 1.0 nm mesh size is smaller than this Debye length of channel region. Considering the carrier density distribution around the channel region of MOSFET (especially strong inversion region at the source side), abrupt change exists for the vertical direction as shown in Fig. 3 (a). If the mesh size is wider than Debye length of channel region, the carrier density distribution cannot be described appropriately and the calculation results become inaccurate. This is the reason why the results changed by several decades of percentage between the case of $\Delta y = 1.0$ nm and other cases for vertical direction.

To tackle thermal problem of semiconductor devices, precise prediction of temperature distribution inside MOSFET is needed. Therefore, appropriate mesh size for vertical direction is more important. On the other hand, if 1.0 nm $\times$ 1.0 nm mesh is used, the calculation time is several weeks just only for estimating the temperature distribution or any other characteristics of one MOSFET. This is not useful from the industrial point of view. However, if wider mesh size is used, the calculation accuracy worsens. One of the available ways possible is by using wider mesh for lateral direction and finer mesh for vertical direction. However if mesh zoning is possible for vertical direction, the accurate results with short calculation time is realized. In following part, we will discuss the mesh zoning method for vertical direction.

Mesh zoning method

As mentioned above, Debye length at the channel region in MOSFET has to be defined by the carrier density at the channel and Debye length at the channel region can be derived from the continuity equation and Poisson equation. These are the characteristics for mesh zoning of MOSFET simulation.

In the electro-thermal analysis (hydrodynamic model), continuity equation and momentum conservation equation for electrons are below.

$$\frac{\partial n}{\partial t} + \nabla \cdot (n \mathbf{v}_e) = -R$$

(28)

$$-qn \nabla \phi + \nabla (nk_B T_e) = -\frac{nm_e^* \mathbf{v}_e}{\tau_{me}}$$

(29)

The electron current is defined as $\mathbf{J}_e = -qn \mathbf{v}_e$, and Eq. (28) can be rewritten to the similar form of Eq. (21). Here, we only consider vertical ($y$) direction.

$$\frac{\partial n}{\partial t} + \frac{1}{q} \frac{\partial \mathbf{J}_e}{\partial y} = -R$$

(30)

By using the relationship of $\mu_e = q \tau_{me} / m_e^*$, the momentum equation changes to the definition of current.

$$\mathbf{J}_e = qn \mu_e \mathbf{E} + \mu_k \mathbf{E} \nabla \left( nT_e \right) = \sigma \mathbf{E} + \mu_k \mathbf{E} \nabla \left( nT_e \right)$$

(31)

where $\sigma$ represents the electrical conductivity. As mentioned before, in the channel
region of MOSFET, this electrical conductivity is defined by channel carrier density, \( n^* \). In this work, we defined the electrical conductivity as \( qn^* \mu_e \) in the channel region and assume this conductivity is constant in whole region. \( \mu_e \) of the second term is also assumed to be constant.

Setting the uniform equilibrium concentration \( n_0 \), Poisson equation is as Eq. (22).

\[
\frac{\partial^2 E}{\partial y^2} = -\frac{q(n-n_0)}{\varepsilon_t} \quad (32)
\]

Substituting Eqs. (31) and (32) to Eq. (30) yields the following equation.

\[
\frac{\partial}{\partial t} n_0 qn^* \mu_e (n-n_0) - \frac{\mu_e k_B}{q} \frac{\partial^2}{\partial y^2} (nT_e) = -R \quad (33)
\]

This equation is quite similar to Eq. (24). Using the calculation results of 1.0 nm \( \times \) 1.0 nm mesh model, we can eliminate some terms of Eq. (33) and rewrite a more simple form.

For the case of steady state analysis, the first term at left hand side of Eq. (33) can be eliminated. The carrier generation/recombination term, \( R \), is a complex function of carrier density, \( n \), but for the sake of simplicity we avoid using this term. Eq. (33) now becomes

\[
T_e \frac{\partial^2 n}{\partial y^2} + 2 \frac{\partial n}{\partial y} \frac{\partial T_e}{\partial y} + n \frac{\partial^2 T_e}{\partial y^2} = \frac{q^n}{\varepsilon_k B_T n} (n-n_0) \quad (34)
\]

Figure 4 shows the magnitude of the term at left hand side of Eq. (34) near the channel region \((y = 0 \text{ nm to } 20 \text{ nm})\). These are the results from fine mesh model. In this figure, the absolute values of each term are shown. From this result, the second term at the left hand side of Eq. (34) is several orders smaller than the first term. Also the third term at the left hand side of Eq. (34) is smaller than the first term underneath gate oxide. With closing the bottom surface of MOSFET, these terms become comparable but the characteristics of MOSFET are mainly determined by the channel inversion region, especially underneath the gate oxide. Therefore, the second and third terms can be neglected and Eq. (34) can be rewritten to a more simple form.

\[
\frac{\partial^2 n}{\partial y^2} - \frac{q^n}{\varepsilon_k B_T n} (n-n_0) = 0 \quad (35)
\]

Applying boundary condition, that is \( n = n_0 \) at \( y \to \infty \) and \( n = n^* \) at \( y = 0 \), the solution of this equation is

\[
n = \left(n^* - n_0\right) \exp\left(-\frac{y}{L_D^*}\right) + n_0 \quad (36)
\]

\[
L_D^* = \sqrt{\frac{\varepsilon_k B_T T_e}{q^n}} \quad (37)
\]

From Fig. 3, the electron density at the substrate in the calculation domain is about \( 2 \times 10^{23} \text{ m}^{-3} \) and highest electron density in the channel region is about \( 1 \times 10^{23} \text{ m}^{-3} \). These density values are similar to substrate impurity density, \( N_A \), and the electron density in the highly doped region under the source or drain electrode, \( N_D \), respectively. Therefore, we applied \( n^*_{y=0} = 1 \times 10^{25} \text{ m}^{-3} \) and \( n_0 = 2 \times 10^{23} \text{ m}^{-3} \) and solve Eqs. (36) and (37) to obtain the value of Debye length. Considering the form of Eq. (37), \( L_D^* \) becomes larger with increasing electron temperature. However, electron temperature cannot be detected before calculation. For accurate calculation results, smaller mesh is preferred. This means that, if we assume the electron temperature is uniform at 350 K, calculated \( L_D^* \) is shorter than the actual \( L_D^* \) and accurate MOSFET characteristics can be obtained. Therefore, here, \( T_e = 350 \text{ K} \) is assumed and the calculation procedure is as follow.

1. Setting \( n^* = n^*_{y=0} = N_D \), \( L_D^* \) can be obtained from Eq. (37).
2. Multiplying \( L_D^* \) by weighting factor, \( w \) (must be less than 1), \( dy_1 \) can be obtained.
3. This value of \( dy_1 \) is mesh size of the first layer.
4. Substituting \( dy_1 \) and \( n^* = n^*_{y=0} \) to Eq. (36), the value of \( n \) at \( y = dy_1 \) can be obtained.

This \( n \) becomes \( n^*_{y=dy_1} \).
4. Substituting \( n^* = n^*_{y=dy1} \) to Eq. (37), a new \( L^*_D \) value can be obtained. Multiplying new \( L^*_D \) by \( w \), dy2 is obtained. This dy2 becomes the mesh size of the second layer.

5. Solving 1 – 4 iteratively, zoned mesh can be obtained in whole region of calculation domain.

Comparison of the results

In following part, the results of the fine mesh model and zoned mesh model are compared. We used the zoned mesh model, which is zoned mesh for vertical direction and \( \Delta x = 1.0 \) nm for lateral direction. In the zoned mesh, a \( w \) value of 0.696 is used. As a result, the mesh size of the first layer for vertical direction becomes about 1.0 nm (similar to unzoned mesh model) and total mesh number for vertical direction becomes 48.

Table 3 shows the drain current and the maximum lattice temperature of each model. As can be seen in this result, the drain current of zoned mesh model is 1319 mA/mm and the difference between fine mesh model and zoned mesh model is 1.35 %. The maximum lattice temperature of zoned mesh model is 363.8 K and the difference between fine mesh model and the zoned mesh models is 0.27 %. These results of zoned mesh model have a good agreement with the results of fine mesh model, with the calculation time of zoned model is greatly reduced by 30 times than that of fine mesh model.

<table>
<thead>
<tr>
<th>Mesh size</th>
<th>( I_D ) [mA/mm]</th>
<th>( \Delta I_D ) [%]</th>
<th>( T_{L \max} ) [K]</th>
<th>( \Delta T_{L \max} ) [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fine mesh</td>
<td>1337</td>
<td>-</td>
<td>364.7</td>
<td>-</td>
</tr>
<tr>
<td>Zoned mesh</td>
<td>1319</td>
<td>1.35</td>
<td>363.8</td>
<td>0.27</td>
</tr>
</tbody>
</table>

Fig. 4  Comparison of each term of Eq. (34)

Fig. 5  Distribution of electron density
Figure 5 shows the results of electron density distribution in the MOSFET. This graph shows the electron density distribution of fine mesh and zoned mesh with the result of 1.0 nm $\times$ 2.5 nm mesh model as reference.

From these results, it can be said that our mesh zoning method is useful from the industrial and engineering point of view.

4. Concluding Remarks

In this work, electro-thermal analysis of Si MOSFET with several mesh sizes was performed. From the calculation results, the mesh size for lateral direction did not strongly affect the calculation results. On the other hand, the mesh size for vertical direction is much more important. Minimum requirement of the mesh size for vertical direction is defined by the Debye length, which is calculated by the channel carrier density. If the mesh size becomes larger than this Debye length, percentage error of results becomes several decades. Furthermore, we proposed the mesh zoning method for MOSFET simulation, and by using our mesh zoning method, accurate results can be obtained, with the calculation time greatly reduced by at least 30 times.

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