Study of Trap Generation in the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ Gate Dielectric Stack by Scanning Tunneling Microscopy*

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Scanning tunneling microscopy is used to study trap evolution in the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gates tack. Current-voltage characteristics extracted from leakage sites exhibit stress-induced-leakage-current (SILC) or barrier-height-lowering (BHL) behavior. The high- κ layer is observed to have larger *intrinsic* trap generation rate, compared to the SiO_x layer, due to a higher surface plasmon generated hot-hole current at the tip/high- κ interface. In the presence of electronic traps: (i) SILC traps near the cathode inhibit trap generation in the layer near the anode due to inelastic-trap-assisted-tunneling mechanism; (ii) SILC traps near the cathode may evolve into BHL as lattice displacement due to electron charging during the inelastic-trap-assisted tunneling process may accelerate the wear-out of the neighboring region; and (iii) traps with BHL characteristics in the high- κ may accelerate the breakdown of the Interfacial layer (IL) due to enhanced electric field in the IL. An electrical stress induced trap evolution model in the gate stack is proposed.

1. Introduction

Electronic traps have been identified to play a crucial role in the wear-out/breakdown process of SiO_2 gate dielectric. During the wear-out phase, traps are generated inside the oxide¹⁾ and at the interfaces²⁾ by the applied voltage and/or the current flowing through the oxide³⁾. The density of these traps would eventually become high enough to result in a locally high current density, which triggers thermal runaway in the localized region⁴⁾. Recently, a conventional electrical characterization study based on the metal-oxide-semiconductor (MOS) capacitor with high-dielectric constant (high- κ) gate stack has reported very interesting observations which are yet to be understood. For instance, the Weibull slope of the high- κ gate stack subjected to gate injection stress is much smaller than that of substrate injection stress (SIS). Interpretation of this observation in the context of the percolation model leads to unrealistic outcomes, such as very large defect size (~ 10 nm diameter)^{5,6)}. It is unclear how electronic traps in each layer (the high- κ and interfacial layers) will influence the overall reliability of the gate stack.

Inherent non-uniformity in most high- κ thin films presents significant challenges to macroscopic characterization techniques. As the gate insulator becomes thinner, the direct tunneling (DT) current becomes measurable (> 1 pA). Hence, it is feasible to use scanning tunneling microscopy (STM) to measure spatially resolved tunneling current (I_t) flowing from the STM tip

through the thin insulating layer to the substrate, hence probing the localized electrical properties of the ultrathin insulator with nanoscale spatial resolution.

In this paper, using ultrahigh-vacuum-STM (UHV-STM), the polycrystalline structure of the high- κ and amorphous SiO_x interfacial layer (IL) can be imaged independently using different biasing polarity (V_s). In this way the STM can provide images of individual leakage sites in the film. Current-voltage (I_t - V_s) characteristics extracted from leakage sites are found to exhibit either stress induced leakage current (SILC) or barrier height lowering (BHL) behavior. The polarity dependent STM current can therefore allow the demarcation of electronic traps of different properties in the high- κ and the IL. It is important to note that the use of UHV is critical as it allows for measurement under both polarities without electro-deposition or anodic oxidation.

Electronic trap evolution in each layer is studied under electrical stress. The high- κ layer is observed to have a larger intrinsic trap generation rate as compared to the IL due to a higher anode-hole-injection coefficient, resulting in higher surface plasmon generated hot-hole current at the tip/high- κ interface. In addition, when electronic traps exist prior to any applied stress, we show that: (i) SILC traps near the cathode inhibit trap generation in the dielectric layer near the anode. We attribute this observation to inelastic-trap-assisted-tunneling (iTAT) mechanisms; (ii) SILC traps near the cathode may evolve into BHL as lattice displacement due to electron charging (which occurs physically at the trap location) could accelerate the wear-out of the neighboring region; and (iii) traps with BHL characteristics in the high- κ could accelerate the breakdown of the IL due to an enhanced electric field in the IL.

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Details of the STM results leading to the above conclusions are presented below, and a model of the stress-induced trap evolution in the high- κ gate stack is proposed.

2. Experiment

Our study was made on the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ dielectric stack grown on n-Si by electron-beam evaporation in UHV. Post-deposition annealing (PDA) was carried out at 300°C and 500°C in nitrogen for 5 minutes. The respective thickness of Sc_2O_3 , La_2O_3 , and SiO_x are 2.4, 4.3 and 1.2 nm, as determined from high resolution transmission electron microscopy (TEM). UHV–STM was performed using a W tip. For routine topography imaging and STM control, V_s of -4 V was applied to the substrate and the W tip was grounded. During imaging a feedback circuit keeps I_t constant at a preset value (typically 20 pA) by varying the separation between the W tip and the sample surface. Such topography maps are called constant current images (CCI). The contrast variation in the images can arise from local variation in the film thickness and/or conductance. The current voltage characteristic (I_t - V_s curve) was measured at any chosen position in the image by freezing the feedback control and sweeping V_s from -4 to $+4$ V, at a rate of ~ 60 mV/ms.

A powerful variation of STM imaging we use is current imaging tunneling spectroscopy (CITS), in which the tunnel current is measured at a number of predetermined voltages at all pixel locations in the image. A constant voltage current image (CVI) can then be formed showing the current flow at a particular voltage across the surface, which can reveal the spatial distribution of electronic traps. SIS was applied during CITS imaging by extending the I_t - V_s measurement to higher voltages (-5 V).

2.1 Polarity dependent I_t

The Wentzel-Kramers-Brillouin (WKB) approximation gives the relation between the tunneling probability T_t and the barrier height (BH)[$V(z) - E$]^{7,8)}

$$T_z = \exp \int_{z_1}^{z_2} \left\{ \frac{2\pi^2 m^*}{h^2} [V(z) - E] \right\}$$

where z is separation between electrodes, E is the electron energy, V is the applied bias, and m^* is the effective electron mass. **Figure 1** shows the variation of T_t with lowering of the BH at the cathode/dielectric interface (open square for DT current, solid line for Fowler-Nordheim (FN) current) and dielectric/anode interface (closed square for DT current, dotted line for FN current). Tunneling is far more sensitive to the barrier variation at the electron injecting interface i.e. the cathode. The electron collecting interface (anode) has insignificant contribution to I_t .

BHL simulates the presence of an electronic trap. The calculation was performed by assuming an electronic trap with diameter $6 \text{ \AA}$ ⁹⁾ located near the cathode or the anode of a single layer dielectric material with BH of 2.3 eV (i.e. the conduction band offset between La_2O_3 and Si). The electronic trap is assumed to induce energy states from 1 eV to 1.6 eV below the conduction band minima (CBM) of the dielectric¹⁰⁾. Hence, T_t is calculat-

Fig. 1 Variation of T_t with lowering of BH at the cathode/dielectric interface and dielectric/anode interface. BH lowering (BHL) simulates the presence of an electronic trap. T_t is much lower and is insensitive to the BHL at the dielectric/anode interface.

Fig. 2 $110 \times 110 \text{ nm}^2$ CITS images at positive bias polarity. (a) CCI at $+3.5$ V, 20 pA. The positive bias condition images the high- κ interface. The z scale ranges from 0 to 6 nm; (b) corresponding CVI at $+2$ V. The variation in I_t is from 0 to 5 pA.

ed with a BHL varying from 1 eV to 1.6 eV at 2 V (DT) and 3 V (FN tunneling).

T_t is much lower and is insensitive to BHL at the dielectric/anode interface. This result implies that in the STM experiments surface and interface properties can be analyzed almost independently for the high- κ interface at positive V_s and for the SiO_x/Si interface at negative V_s .

Figure 2(a) shows a CCI obtained at $V_s = +3.5$ V, with I_t of 20 pA. I_t of 20 pA is selected to avoid crashing the tip onto the sample, yet is sufficiently large to maintain good signal to noise ratio. A granular structure of diameter varying from 10 to 40 nm is evident. CVI at $+2$ V is shown in **Fig. 2(b)**. CVI at V_s ranging from $+1$ to $+2.5$ V consistently show a higher I_t at the edge of the grains, due possibly to dangling bonds at the grain boundary (GB). In contrast to the much higher I_t at the boundary, a distinctly lower I_t is observed within the grain itself. This direct observation of a high I_t at the GB of a high- κ gate dielectric lends support to the hypothesis of GB assisted breakdown, as reported for HfO_2 ¹¹⁾.

In order to obtain the grain size distribution from the STM image, a larger area of $200\text{ nm} \times 200\text{ nm}$ is scanned at $+3.5\text{ V}$, 20 pA . TEM plan-view of the same sample is shown in **Fig. 3(a)**. An estimation of the grain size distribution from both techniques is shown in **Fig. 3(b)** and can be approximated by a Gaussian distribution. The average grain sizes are 22 nm and 27 nm , obtained from STM and TEM plan-view technique, respectively. The slightly larger grain size observed in STM, may be attributed to finite tip size effects.

Scanning at -4 V , an amorphous like image was revealed (**Fig. 4(a)**). As discussed above, under negative V_s , the current I_t is more sensitive to BH at the SiO_x/Si interface. Hence the STM image at -4 V provides convoluted information on the SiO_x/Si morphology and electrical properties. The CCI shows a root-mean-square roughness of 0.34 nm and granular structures of $\sim 5\text{ nm}$ diameter. In order to separate the electrical properties from morphology, a CVI was used for comparison (**Fig. 4(b)**). The bright features in CVI correspond to regions with higher I_t at a given V_s . A higher I_t can arise from electrical defects (e.g. oxygen vacancy, crystal defects) or a smaller physical thickness. High I_t regions due to a thinner film will appear dark in the CCI but bright in the CVI (labeled “T” in **Fig. 4**). The direct observation of an ap-

parent leakage current induced by a thickness variation gives a physical explanation to the lack of thickness/area-scalability in I_t - V_s characteristics of the La_2O_3 MOS capacitor¹²⁾. On the other hand, an electrical defect giving rise to a higher I_t will appear bright in both CCI and CVI (labeled “E” in **Fig. 4**). An analysis of the number of leakage sites in the CITS images enables the electrical defect density to be estimated as $\sim 4 \times 10^{11}\text{ cm}^{-2}$. The images provide direct evidence for the coexistence of both space-charge-limited¹³⁾ and DT¹²⁾ leakage current.

The polarity dependent I_t enables the high- κ and the IL to be probed independently, hence facilitating the study of electronic trap evolution in each layer, as presented below.

3. Results and Discussions

3.1 Demarcation of locations and properties of electronic traps

Figure 5(a) depicts a set of CITS data showing: (I) CCI at 20 pA and -4 V , (II) CVI at a low negative V_s (-2.3 V), (III) CVI at low positive V_s ($+2.3\text{ V}$) and, (IV) CVI at a high positive V_s ($+4\text{ V}$). the contrast of the CVI images is adjusted such that pixels having I_t (at the specified V_s) in the top fifth percentile of the current dis-

Fig. 3 (a) plan view TEM; (b) Grain size measured from STM (blue line) and plan-view TEM (red line) techniques. Plan-view TEM result is in courtesy of L. J. Tang.

Fig. 4 $50 \times 50\text{ nm}^2$ CITS images at negative bias polarity. (a) STM topography at -4 V , 20 pA . The negative bias condition images the SiO_x/Si interface. The z scale ranges from 0 to 3 nm (b) corresponding CVI at -2 V . The variation of current is 0 to 5 pA .

Fig. 5 (a) CITS measurement data with STM feedback control set at -4 V , 20 pA . The data shows the CCI (I) and CVI at (II) -2.3 V , (III) $+2.3\text{ V}$ and (IV) $+4\text{ V}$. (b) CITS measurement of the same area as in (a), but with the STM feedback control set at $+3.5\text{ V}$, 20 pA . The data shows the CCI (I) and CVI at (II) -3.5 V , (III) -2 V and (IV) $+2\text{ V}$.

Fig. 6 I_t - V_s characteristics of the different types of leakage sites shown in **Fig. 5**. Also shown are the reference curves, which are the averaged I_t - V_s curves for the image area, excluding the leakage sites. Measurement was carried out under STM feedback control of (a) -4 V , 20 pA and (b) $+3.5\text{ V}$, 20 pA .

tribution (as measured over the entire image) are shown uniformly bright. This is to identify the most leaky locations within the scanned area. Different CVI are observed depending on the value of V_s , signifying the presence of localized leakage paths with distinct properties.

First, we observe that some bright spots occur at all positive V_s (Fig. 5(a) (III) and (IV)). These are categorized as type A leakage sites. The I_t - V_s curve extracted from a typical type A leakage site (Fig. 6(a), filled circle) shows a near-parallel shift towards lower voltages, as compared to the reference curve (Fig. 6(a), open rectangle). Note that for all I_t - V_s curves, we plot the average current per pixel as a function of V_s . The I_t - V_s curves depicted are therefore independent of the effective area of the leakage site. The reference I_t - V_s curve is an average for all pixels in the entire image area *excluding* leakage sites.

Next, some bright spots are observed at low positive V_s (Fig. 5(a)(III)) but they do not show up as bright in the CVI at high positive V_s (Fig. 5(a)(IV)). These are labelled type B leakage. The I_t - V_s characteristic of type B leakage is similar to that of SILC, i.e. a larger current, as compared to the reference curve, is observed at a low V_s ¹⁴⁾. As V_s is increased, the current value approaches and merges with that of the reference I_t - V_s curve (Fig. 6(a), solid line). Similar behavior is observed at negative V_s and the corresponding locations are named as type C leakage (Fig. 6(a), closed triangle). Type C leakages are only observed at a low negative V_s (Fig. 5(a)(II)).

Leakage sites are also seen whose I_t - V_s curves are shifted parallel (with respect to the reference curve) towards lower voltage under negative V_s ; these are named as type D leakage. However, they cannot be identified in the CITS data of Fig. 5(a) since the STM feedback control was set at -4 V, 20 pA. Thus, the current map at -4 V should show uniform contrast because any increase in current at a type D leakage site is compensated by the STM feedback changing the tip-sample distance to maintain a constant I_t . To reveal the existence of type D leakage sites, CITS is acquired with STM feedback set at $+3.5$ V, 20 pA, as shown in Fig. 5(b) for the same area as that depicted in Fig. 5(a). Columns II, III and IV in Fig. 5(b) show CVI at -3.5 , -2 and $+2$ V respectively. Type D leakage sites can now be observed in Fig. 5(b)(II and III) and the corresponding I_t - V_s curve is shown in Fig. 6(b)(filled circle). In Fig. 5(b)(IV), type B leakage can also be observed at the same position as in Fig. 5(a)(III), although some of them appear to have recovered during the second CITS measurement. A similar observation applies to the type C leakage site (compare Fig. 5(a)(II) and Fig. 5(b) (III), where the solid line shows reproducible type C leakage and the dotted line shows recovered type C leakage). The I_t - V_s curves of type B and C leakage sites are shown in Fig. 6(b)(solid line and filled triangle respectively). Type A leakage cannot be observed in Fig. 5(b) at $+3.5$ V STM feedback conditions due to the same reason that type D leakage cannot be observed in the CITS data of Fig. 5(a) at -4 V.

The near-parallel shift in the I_t - V_s curve of type A (D)

leakage site in the positive (negative) V_s regime implies that the tunneling mechanism at these leakage sites remains the same as that of the trap-free location but the tunneling BH is lowered. It should be noted that more leakage current will also flow if the local film thickness is decreased. Such regions show up as bright spots in the CVI with corresponding dark (i.e. thinner) spots in the CCI. These are labeled as type T in Fig. 5 and are not considered further. The type A (or D) leakage is not a consequence of a locally thinner film and is therefore electronic in nature. Hence, the near-parallel shift in the I_t - V_s curves of type A and D leakage may be ascribed to BHL at these locations.

The similarity between the I_t - V_s characteristics of type B and C leakage sites and those of SILC implies that tunneling via trap states localized in a certain energy interval in the dielectric bandgap is responsible for the observed increased leakage¹⁴⁾. Similarly, type B (C) leakage sites are associated with trap states that are located in the high- κ (SiO_x) layer. Increased I_t arises only when V_s causes the Fermi level (E_f) of the emitting electrode to align with the trap states. The I_t - V_s curve will merge back to the reference curve once the tip E_f moves away from the trapped state energies.

Therefore, it is proposed that type A and D leakage sites are due to lowering of the conduction band minima (CBM) of the high- κ and IL respectively. Type B and C leakage sites are due to trap-assisted-tunneling through the bandgap states in the high- κ and IL, respectively.

3.2 Intrinsic trap generation mechanism

The study on intrinsic trap generation was carried out on $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stacks annealed at 500°C due to its good electrical uniformity (Fig. 7(a)). Fig. 7(a)(I) shows the CCI of a 50×50 nm² area. The respective CVI at $V_s = -2.3$, $+2.3$ and $+4$ V are shown in Fig. 7(a)(II, III and IV). A uniform image is apparent in all cases, indicating excellent thickness and electrical uniformity of the scanned area. The solid line in Fig. 8 depicts the average I_t - V_s curve of the scanned area. A significant increase in I_t for $V_s < -2$ V may be ascribed to DT through the IL (insert (i)). I_t in the positive V_s regime is negligibly small, due to the much thicker high- κ layer (and hence a much larger tunneling barrier)(insert (ii)). This observation also implies that the high- κ layer has negligible pre-existing traps.

The effect of a trap on the electron tunneling probability T_t at the injecting electrode decreases with trap distance from the electrode¹⁵⁾. Thus, differences in stress induced trap generation in the high- κ and IL may be assessed through the relative difference in the increase of I_t under negative and positive V_s ¹⁶⁾, respectively.

Figure 7(b) shows the CITS data of a second consecutive scan of the same area as Fig. 7(a). The negative CVI (Fig. 7(b)(II)) remains uniform, indicating negligible trap generation in the IL after the first scan. On the other hand, localized bright spots are observed in the positive CVI (Fig. 7(b)(III and IV)), signifying trap generation in the high- κ layer. It should be highlighted that there are no bright spots in Fig. 7(a)(III and IV) during the first scan and Fig. 7(b)(II) during the second scan. However,

Fig. 7 CITS data of a 500°C PDA $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack. Column (I) depicts CCI of a $50 \times 50 \text{ nm}^2$ area obtained under STM feedback control of 20 pA, -4 V . Columns (II), (III) and (IV) depict the respective current maps at $V_s = -2.3$, $+2.3$ and $+4 \text{ V}$. Row (a), (b) and (c) denote the CCI and CVI of the selected area after the first, second and fifth scan. The contrast of CVI in row (b) and (c) was adjusted such that only locations exhibiting leakage current above the 95th percentile of the current distribution of the scanned area appear bright. The actual current range of each CVI is shown on the top right corner of each image (in pA).

Fig. 8 Solid line denotes the average I_t - V_s of the $50 \times 50 \text{ nm}^2$ scanned area. The open circles denote a typical I_t - V_s characteristic of the bright spots observed in the positive current maps (Fig. 7 (b-III) and (b-IV)) during the second scan. A significant increase in tunneling current is observed in the positive bias regime only. Insets: Energy band diagrams of the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack under (i) negative and (ii) positive biasing.

bright shades are observed in Fig. 7(b)(III) at a relatively small positive V_s . We therefore infer that trap generation in the high- κ happened during the -4 to 0 V sweep of the second scan. For $V_s < -2 \text{ V}$, electrons from the n-Si conduction band directly tunnel through the ultrathin SiO_x and enter the high- κ conduction band (insert (i); Fig. 8). Due to a lower high- κ CBM as compared to SiO_x , these electrons appear “hot” and they thermalize through electron-lattice interaction in the high- κ bulk

and/or at the tip/high- κ interface, resulting in trap generation. As will be shown later, a much larger relative increase of I_t under positive V_s indicates that most of the traps are located close to the tip/high- κ interface, implying that an interface-related trap generation mechanism dominates over a bulk mechanism. The open circles in Fig. 8 depict a typical local I_t - V_s curve taken at the bright spots in Fig. 7(b)(III and V). The onset of I_t at a much lower positive V_s indicates significant BHL at the tip/high- κ interface, confirming that substantial generation of traps has occurred in the high- κ layer during the -4 to 0 V sweep of the second scan.

After the fifth consecutive scan over the same area, bright spots can be observed in both the negative (Figure 7(c)(II)) and positive (Fig. 7(c)(III and IV)) CVI. The presence of bright spots in the negative CVI implies that trap generation has also occurred in the vicinity of the IL.

To estimate the rate of trap generation in the two layers, we plot the percentage P of the scanned area having I_t greater than a predetermined threshold (arbitrarily defined to be the 95th percentile of the current distribution of the second scan) as a function of the scan time T . The slope of the P - T plot yields an estimate for the trap generation rate. The initial trap generation rate in the high- κ layer is $\sim 0.8\%/ \text{min}$ (before IL SILC traps are generated), about 40 times that in the IL ($\sim 0.02\%/ \text{min}$). The subsequent lowering of trap generation rate in the high- κ layer, upon trap generation in the IL, to $0.3\%/ \text{min}$ will be addressed later. These results indicate: (i) high- κ is more susceptible to electrical stress induced wear-out as compared to SiO_x and (ii) most of the traps generated in the high- κ are close to the tip/high- κ interface.

A larger anode hot-hole injection coefficient (α_h) at the tip/high- κ interface, as compared to the SiO_x/Si interface provides a plausible explanation for the higher trap generation rate in the high- κ . The probability for defect generation at a given interface is related to α_h , which may be expressed as the product $P_h \theta_h$. P_h is the probability for generating a hole by a hot electron arriving at the anode interface. θ_h is the probability for a hot-hole to tunnel back to the cathode. Hot electrons induce surface plasmons while they are still unscreened at the anode interface. The surface plasmons subsequently decay by generating electron hole pairs (EHP). The fact that the plasmon is generated at the metal surface increases the probability that the hole gets injected back into the oxide, even though the life time of a hole in metal is in the femto second regime¹⁷.

Figure 10 illustrates this process of EHP generation by excitation and decay of surface plasmons. Firstly, electrons accelerate and gain energy while traveling from the cathode to the anode (1). A significant fraction of the energetic electrons lose energy at the anode/oxide surface by emitting surface plasmons (2). Surface plasmons decay and EHP are excited (3). A fraction of EHP recombine and emit as photons^{18,19} while the remaining EHP get reinjected back towards the cathode and are trapped in the oxide (4). The threshold energy $\hbar \omega_{sp}$ for

surface plasmon excitation at a SiO_2/Si interface has been consistently observed at about 7.5 eV by Electron Energy Loss Spectrum²⁰. The energy $\hbar \omega_{\text{sp}}$ at a W surface is predicted to be 3 eV²¹, a result supported by localized light emission spectra observed in STM^{18,22} and scanning tunneling optical spectroscopy (STOM)²³. This implies that for the range of voltage considered in this study, the surface plasmon effect is negligible at the SiO_x/Si interface while it is relatively significant at the metal/high- κ interface. We expect a much higher θ_h at a low bias regime at the metal/high- κ interface due to a smaller hole energy barrier. An intrinsically greater anode hot-hole effect at the metal/high- κ interface thus explains why high- κ is more susceptible to wear-out during SIS.

3.3 Influence of electronic traps on trap evolution

It is observed that the trap generation rate reduces from 0.8%/min to 0.3%/min after the third CITS scan (Fig. 9). This behaviour coincides with the onset of the

Fig. 9 Percentage P of the scanned area exhibiting I_t greater than a predefined current threshold. The filled (open) squares denote results obtained under negative (positive) biasing, which probes trap generation in the SiO_x (high- κ) layer. The slope of the plot provides an estimate for the average trap generation rate. The current threshold is defined as the 95th percentile of the respective I_t distribution for $V_s = -2.3$ V and $+4$ V after the second scan.

Fig. 10 Illustration of electron hole pair (EHP) generation by surface plasmon emission and decay. (1) Electrons accelerate and gain energy while traveling from the cathode to the anode. (2) A significant fraction of the energetic electrons lose energy at the anode/oxide surface by emitting surface plasmons. (3) The surface plasmons decay and EHP are excited. (4) A fraction of EHP recombine and emit as photons whereas the holes for the remaining EHP get re-injected back towards the cathode and are trapped in the oxide.

generation of IL SILC in the stressed area (Fig. 7). This implies that the presence of electronic traps in the gate stack have significant influence on trap evolution under electrical stress.

For the study on the role of pre-existing electronic traps on electrical stress induced trap evolution, the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack annealed at 300°C was chosen due to the high density of traps observed in the as-processed film (Fig. 11). Three observations (called Scenarios I-III) on the role of pre-existing electronic traps will now be elaborated based on SIS data.

Scenario I: Fig. 11 shows the CITS of an area of $50 \times 50 \text{ nm}^2$ (a) before and (b) upon SIS. CVI at -2 V show the regions of SILC in the IL. During high voltage stress, electronic traps are expected to be generated in the layer near the metal/high- κ interface, as discussed in the previous section. However, it can be observed from the CVI that, with the presence of IL SILC traps (dotted circles in the current map at -2 V of Fig. 11(a)), there are no new traps generated in the high- κ layer (dotted circles in the CVI at $+4$ V of Fig. 11(b) at the identical locations). Conversely, new traps in the high- κ layer are preferentially generated at locations without IL SILC traps (solid circles in the CVI at (a) -2 V and (b) $+4$ V of (b) of Fig. 11). Dash-dotted circles highlight the evidence for scenario III, which will be discussed later. For better visualization, the CVI at $+4$ V of row (a) is subtracted from that of row (b) to delineate locations showing significant increase in I_t (which implies new traps generated) at $+4$ V (Fig. 12(a)). Fig. 12(a) is then superimposed with the CVI at -2 V of Fig. 11(a) (which best shows the IL SILC traps), to give the image shown in Fig. 12(b). In Fig. 12(b), the dark shades are chosen to show the increase in I_t at $+4$ V (corresponding to the bright shades in Fig. 12(a)) and the bright shades show SILC IL traps (corresponding to the bright shades in the CVI at -2 V of Fig. 11(a)). The bright and dark shades

Fig. 11 CITS of an area of $50 \times 50 \text{ nm}^2$ from the 300°C PDA $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack, (a) before and (b) after SIS. STM feedback conditions 20 pA, -4 V. In the presence of IL SILC traps (dotted circles in the CVI at -2 V of row (a)), there is no new traps generated in the high- κ layer (dotted circles in the CVI at $+4$ V of row (b)) at the corresponding locations. New traps in the high- κ layer are preferentially generated at locations without IL SILC traps (solid circles in the CVI at -2 V of row (a) and CVI at $+4$ V of row (b)). Dash-dotted circles give evidence for scenario III.

Fig. 12 (a) Difference of I_t at +4 V before and after SIS. Bright shades show locations with significant increase in I_t . (b) Superposition of (a) with the current map at -2 V of Fig. 11(a). Locations which exhibit increase in positive I_t (signifying new trap generation in the high- κ) are spatially separate from the locations with pre-existing SILC IL traps.

Fig. 13 I_t - V_s curves taken at locations (a) with pre-existing IL SILC traps (b) without pre-existing IL SILC traps. Data is taken before (filled squares) and after (open squares) SIS stressing. The solid line shows the reference curve.

in Fig. 12(b) are spatially mismatched. This suggests that the presence of IL SILC traps can inhibit further trap generation in the high- κ layer at the same location.

Figure 13 shows I_t - V_s curves extracted from locations with (Fig. 13(a)) and without (Fig. 13(b)) IL SILC traps before (filled square) and during (open square) SIS. The reference curve (solid line) is included in both graphs to highlight the different characteristics (SILC or BHL). In Fig. 13(a), the I_t - V_s at positive V_s is comparable before and after SIS in the presence of IL SILC traps. New traps generated in the high- κ , leading to BHL of the high- κ layer, in the absence of IL SILC traps are evident in Fig. 13(b), with the positive I_t - V_s shifted to a lower V_s upon SIS.

The above observations can be attributed to an inelastic trap-assisted-tunneling (iTAT) mechanism²⁴⁻²⁷. Electrons lose energy while tunneling via a SILC trap, resulting in “cooler” electrons at the anode²⁴⁻²⁶. An iTAT model which includes relaxation²⁷ is thus adopted. For simplification, the multi-barrier high- κ /SiO_x/Si system, together with the vacuum barrier of the STM experiment, is modeled as a single barrier system (**Fig. 14**). By fitting the reference I_t - V_s curve to a DT equation, the effective BH (ϕ_{eff}) and thickness (t_{eff}) of the single barrier model are determined as 5 eV and 3.8 nm, respectively.

The equivalent single barrier model can be inserted into the iTAT model, which is graphically described in Fig. 14. Details of the model can be found in references 24 and 27. It is assumed that there is no elastic out-tun-

Fig. 14 Band diagram for the inelastic trap-assisted tunneling model. See text for details.

neling from the trap to the anode. Electrons tunnel from the cathode to the defect states when the Fermi energy E_f of the cathode lies at or above the defect energy state (J_{in} in Fig. 14). Once the defect state is charged with an electron, the defect changes its structure because it can lower the energy by deforming or reconstructing the lattice. This results in a downward shift of the defect level (which is now charged with an electron). The trap-assisted tunneling therefore is an inelastic process and the excess energy, which equals the shift of the energy level between the charged and uncharged state (i.e. E_{relax}), can be lost in the form of heat²⁸. Subsequently after the energy relaxation, the electron is emitted from the trap (with relaxed energy) to the anode (J_{out} in Fig. 14).

In **Fig. 15**, we fit an I_t - V_s curve extracted from SILC trap sites to the iTAT formulation. The trap-free I_t - V_s is also fitted (to the DT model) and is shown for comparison. The calculated iTAT current fits well to the experimental I_t - V_s extracted from leakage sites which exhibit SILC. Therefore, leakage current at the locations with SILC traps can be explained by an inelastic trap-assisted tunneling mechanism. The presence of an energy loss E_{relax} implies a decrease in electron energy at the anode during the tunneling process. Lower trap generation probability is thus expected at the anode due to thermalization of the “cooler” electrons. This explains why the presence of SILC traps could delay wear-out, and thus increase the reliability margin of the high- κ gate stack.

The iTAT model assumes the location of the trap is at the “electrical” center of the barrier, which results in the maximum T_t for the iTAT mechanism. The electrical center does not necessarily correspond to the physical center in the dielectric layer. This is especially true in our case where the band alignment of the multi-layer dielectric is asymmetric. As established in the literature¹⁵) and shown in the previous section, I_t is most sensitive to the barrier of the injecting interface. We therefore determined the trap location (either in the high- κ layer or in the IL) by whether the SILC characteristic occurs at positive V_s (traps located in high- κ) or negative V_s (traps located in the IL). Irrespective of the physical location of the trap, the assumption that the trap is at the electrical center of the single barrier model still holds provided J_{in}

Fig. 15 Comparison of I_t - V_s data with the iTAT model. The solid line shows I_t calculated by the iTAT mechanism. The enhanced low voltage current and almost self-limiting high voltage current of the experimental I_t - V_s curve from locations with IL SILC traps (closed square) is well modeled by the iTAT mechanism. The I_t - V_s found at trap free locations (+) can be fitted to the DT model at low bias with $\phi_{\text{eff}} = 5$ eV (dottedline).

$\approx J_{\text{out}}$, which gives the largest T_t .

Scenario II: Whilst delaying the formation of a percolation path throughout the entire gate stack by “hampering” trap generation in the layer next to the anode (i.e. scenario I), SILC traps in both layers of the gate stack are observed to develop into a leakage path showing BHL upon further electrical stress (**Fig. 16**). Pre-existing high- κ SILC traps are depicted as bright shades in Fig. 16(a). Fig. 16(b) shows an increase of I_t at a relatively high voltage (+4 V) upon SIS. The I_t - V_s curve of these leakage sites is shifted to a lower V_s after SIS, implying BHL, possibly induced by a structural change such as the formation of a percolation path.

Fig. 16(c) is the superposition of images (a) and (b). The overlap of bright shades in (a) and (b) appear as the brightest shades (in red) in (c). Fig. 16(d) shows I_t - V_s curves extracted from a bright shade in Fig. 16(c) and its corresponding I_t - V_s prior to SIS stressing. SILC traps exist in both the IL and the high- κ before SIS. As described in Scenario I, the presence of IL SILC traps should hamper further degradation of the adjacent high- κ layer. However, degradation of the SILC traps into a leakage site with lowered BH is evident in Fig. 16, which cannot be attributed to electron thermalization. A possible mechanism arises from the inelastic nature of tunneling via SILC traps. Energy loss during iTAT is possibly caused by a lattice deformation upon capturing an electron. The energy loss could transform into localized heat. As a result, trap generation in the vicinity of pre-existing IL SILC traps is enhanced and subsequently, IL SILC traps evolved into a percolation path of lowered BH.

Scenario III: During SIS, electronic traps are expected to be generated in the high- κ layer due to hot electron thermalization at the anode. However, trap generation at the IL can also be observed at locations with pre-existing leakage sites in the high- κ which exhibit BHL charac-

Fig. 16 Data for Scenario II showing 50×50 nm² CITS images of the 300°C annealed $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack. The STM feedback control is -4 V, 20 pA. (a) Bright shades show pre-existing high- κ SILC traps. Image obtained by subtracting the CVI at +4 V from the corresponding CVI at +2 V (this procedure highlights the SILC characteristic) (b) Bright shades show increase of current at +4 V upon SIS. Image obtained by subtracting the CVI at +4 V before stressing from that after stressing. (c) Superposition of (a) and (b). The brighter shades correspond to overlapping of bright shades in (a) with bright shades in (b). (d) I_t - V_s extracted from the brighter shades in (c), showing that SILC traps in the high- κ evolve into a leakage path of lowered BH (I_t - V_s curve shifted parallel towards lower V_s) within the high- κ , even in the presence of IL SILC traps. Filled squares show before SIS and open squares after SIS.

teristics. In this case, the potential drop (and hence electric field) across the IL is greatly enhanced in the presence of the low resistance^{29,30} percolation path in the high- κ . On the other hand, a leakage path in the IL will not result in significant E enhancement in the high- κ layer as the high- κ layer is much thicker than the IL.

Experimental evidence for scenario III is shown in **Fig. 17**. Fig. 17(a) shows the CITS CVI at +4 V before SIS. Bright shades signify leakage sites exhibiting BHL characteristics. To observe leakages generated in the IL, the CVI at -4 V before stressing is subtracted from the CVI at -4 V after stressing (Fig. 17(b)). Fig. 17(b) is superimposed on Fig. 17(a) for comparison and the resultant image is shown in Fig. 17(c). The overlap of the bright spots in Fig. 17(b) with those of Fig. 17(a) (brighter shades in Fig. 17(c)) shows that most of the SIS induced leakage sites in the IL occur at locations where leakage sites pre-exist in the high- κ .

The solid circle highlights the SIS induced IL traps which do not coincide with the pre-existing high- κ traps (Fig. 17(b)). These are exceptional cases and can be explained by the mechanism of Scenario II, where leakage in the IL can evolve from IL SILC traps (the IL SILC traps were found to exist prior to SIS).

Fig. 17 Data for Scenario III showing $50 \times 50 \text{ nm}^2$ CITS images of the 300°C annealed $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack. The STM feedback controls -4 V , 20 z pA . (a) CVI at $+4 \text{ V}$. Bright shades signify leakage sites exhibiting BHL characteristic in the high- κ layer. (b) Image obtained by subtracting the CVI at -4 V before and after SIS. Bright shades signify generated IL leakage sites with BHL characteristic. The bright shades enclosed by the circle are exceptional in that they evolve from IL SILC traps, as described in scenario II. (c) Superposition of (a) and (b), showing most stress induced IL traps are located at pre-existing high- κ leak sites exhibiting BHL characteristic.

Fig. 18 (a) I_t - V_s curves extracted from bright shades in the overlaid image in Fig. 17(c). Filled squares before SIS and open squares after SIS.

I_t - V_s curves are shown in **Fig. 18**. Traps are generated in the IL (open square, parallel shift of I_t - V_s to a lower V_s) at locations in the high- κ with pre-existing traps which exhibit BHL characteristics (filled square, increase in current at positive V_s).

3.4 Breakdown model

Based on the three scenarios above, a model is proposed for the evolution of soft breakdown in a high- κ gate stack under SIS (**Fig. 19**). Fig. 19(a) shows schematically an area of an unstressed film. Locations marked with labels I to III correspond to scenarios I to III. A pre-existing (filled circle) IL trap with SILC characteristic (marked as II) and a high- κ leakage site exhibiting BHL (i.e. a percolation path in the high- κ layer, marked as III) are shown in an area before SIS is applied (Fig. 19(a)). The shaded area in the high- κ layer (marked with I) shows a location with suppressed trap generation probability in the presence of an IL SILC trap (Scenario I).

Fig. 19(b) shows the area after SIS. Traps are generated (open circle) with a higher probability in the high- κ layer due to hot electron thermalization at the anode. No trap is generated at the shaded area in the high- κ

Fig. 19 Proposed soft breakdown evolution under SIS. Filled circles in (a) show as-processed traps and open circles in (b) and (c) show newly generated traps. The shaded region shows the location where trap generation is suppressed (Scenario I). Trap generation is expected at the high- κ (anode) during SIS except at the location with IL SILC (Scenario I, see I in (b)). SILC in both IL and high- κ can further evolve into a full percolation path exhibiting BHL (Scenario II, see II in (b)). With the formation of a full percolation path in the high- κ , the corresponding IL experiences enhanced E , leading to trap generation (Scenario III, see III in (c)). Soft breakdown is triggered when traps line up shorting the cathode to the anode.

(Scenario I). The IL SILC trap (II) will evolve into a full percolation path in the IL due to trap generation (open circles) in the neighboring region of the pre-existing IL SILC trap by the mechanism described in Scenario II. A reduced voltage drop in the high- κ results in an enhanced electric field E across the IL layer, hence a higher trap generation probability in the IL, as described under Scenario III. Trap generation in the IL can be observed at locations with a pre-existing high- κ percolation path (III).

Traps generated in Fig. 19(b) (open circles in (b)) can be viewed as pre-existing traps (closed circles) in subsequent stress cycles (Fig. 19(c)). In Fig. 19(c), the as-processed IL SILC traps (marked as II in (a) and (b)) evolve into a percolation path in the IL and the characteristic SILC I_t - V_s disappears. Further, as there is no longer energy loss via the inelastic tunneling process, traps are now generated favorably in the adjacent high- κ layer. Stress induced traps (open circles in (b)) percolate the high- κ layer forming a low conductivity path in the high- κ (III), initiating trap generation in the IL by the mechanism of scenario III. The pre-existing high- κ percolation path (III in Fig. 19(a)), with further trap generation in the corresponding IL, evolves into a full percolation path shorting the cathode to the anode (III in Fig. 19(c)), triggering a breakdown event in the entire high- κ gate stack.

4. Conclusions

Demarcation of electronic traps with SILC or BHL characteristics in the high- κ and SiO_x interfacial layers can be achieved with high spatial resolution using UHV STM at different bias polarity. A distinct trend in trap generation at locations with or without pre-existing traps is observed. In the presence of pre-existing traps: (I) SILC traps at the cathode layer could suppress trap generation in the corresponding anode layer; (II) SILC traps at the cathode layer could evolve into a percolation path; (III) Leakage which shows BHL in the high- κ

could accelerate breakdown in the IL. Observations (I) and (II) can be attributed to mechanisms arising from inelastic tunneling via SILC traps and observation (III) to an enhanced electric field across the IL in the presence of a percolation path in the high- κ layer. At locations without pre-existing traps, electronic traps are generated at a higher rate in the high- κ due to a higher anode-hole injection coefficient. The results have important implication for high- κ gate stack reliability because trap generation is shown to be correlated to pre-existing electrical defects, in contrast to the uncorrelated breakdown observed in ultra-thin SiO₂ gate dielectric.

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