Technical Paper

Electrical Properties of Flat MOS Transistors

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Electrical characteristics of MOS transistors fabricated with the flat MOS technique, where the silicon nitride was used as a mask against the thermal oxidation, were investigated and compared with those of MOS transistors fabricated with the conventional technique. It is found that the threshold voltage (V_T) is substantially greater and the effective carrier mobility (μ_{eff}) is smaller for N -channel devices with the flat MOS technique than those with the conventional technique which have the same gate oxide thickness and substrate resistivity. While for p -channel devices, V_T is slightly smaller with the flat MOS technique than with the conventional technique. The difference of V_T and μ_{eff} mentioned above is found to be due to the fact that the deviation of the impurity profile near Si-SiO₂ interface from the bulk level of impurity concentration is slight in flat MOS transistors compared to conventional MOS transistors, where the impurity redistribution is remarkably brought about during the field oxidation.

1 Introduction

Recently a new technique, where a layer of silicon nitride is used as a mask against the thermal oxidation of silicon wafer, attracts attentions of semiconductor integrated circuit manufacturers because of its several merits. This silicon nitride mask technique has been called Planox process^{1),2)}, LOCOS method^{3)~5)}, etc.⁶⁾, and applied for fabrication of bipolar devices, MOS devices, and etc..

The most obvious advantage by this new technique is the reduction in the different levels in the oxide on the wafer surface for the production of MOS integrated circuits. This makes it easier to form fine patterns by photomasking process and to prevent the metal strips from breaking at the steps of the oxide. Accordingly, this technique makes it possible to fabricate more densely packed and reliable MOS integrated circuits.

Morandi¹⁾ made MOS transistor by the silicon nitried mask technique named Planox process for the first time. J. A. Appels, et al.^{3),5)} developed this technique as LOCOS method and applied it to devices other than MOS transistor. But the electrical characteristics of MOS transistor prepared by this new technique were not yet studied systematically.

The purpose of this paper is to describe the electrical properties of the flat MOS transistors*¹ fabricated with the silicon nitride mask technique, comparing with those of the conventional MOS transistors obtained under the same condition. The electrical characteristics, such as threshold voltage and effective

carrier mobility, are presented for both n - and p -channel devices.

2 Experimental Procedure

In this experiment, both n - and p -channel MOS transistors were fabricated by each of the two techniques; the flat MOS technique and the conventional technique. For n -channel devices, boron-doped p -type (100) silicon wafers with three kinds of resistivity (A), (B), and (C) as shown in Table 1 were used respectively as substrates. On the other hand, for p -channel devices, antimony-doped n -type (100) silicon wafers with resistivity of 3.5~5.5 $\Omega \cdot \text{cm}$ were used. After lapping and polishing, the silicon wafers were chemically etched.

Table 1 Material and dimensional properties

Channel type	n	p
Starting material	Boron-doped p -type (100) Si (A) 0.5~1.5 $\Omega \cdot \text{cm}$ (B) 1.5~2.5 $\Omega \cdot \text{cm}$ (C) 3.5~4.5 $\Omega \cdot \text{cm}$	Antimony-doped n -type (100) Si (D) 3.5~5.5 $\Omega \cdot \text{cm}$
Gate oxide thickness	1050 $\pm$ 50 Å	1050 $\pm$ 50 Å
Field oxide thickness	14000 $\pm$ 1000 Å	14000 $\pm$ 1000 Å

The process sequence of the flat MOS technique is schematically shown in Fig. 1 with that of the

*¹ Here, the MOS transistor fabricated with the silicon nitride mask technique is called the flat MOS transistor for the purpose of distinguishing from the MOS transistor fabricated with the conventional technique, because the final surface of the device is relatively flat.

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Fig. 1 Process sequences of the flat MOS technique (a) and the conventional MOS technique (b)

conventional technique. In the flat MOS technique, first, a silicon dioxide layer with thickness of 300 Å was thermally grown on a silicon surface, and then, a silicon nitride layer with thickness of 3000 Å was deposited by a reaction of SiH₄ and NH₃ at 750°C. The nitride layer was selectively etched away from the field region with the hot phosphoric acid.

The thin silicon dioxide layer under the nitride layer protected the silicon surface from attack by the hot phosphoric acid. Next, the substrate was put into a furnace in an oxidizing environment to grow a field oxide on the substrate excepting the silicon nitride region. The field oxide with thickness of 1.4 μm was formed in steam at 1140°C for 4 hours. Furthermore, after the nitride layer on the source and the drain regions of the MOS transistor were selectively etched away, the source and drain diffusion were performed in the conventional method. Then, after the last nitride layer on the gate region was removed, the gate oxide with thickness of 1050 Å was thermally grown in steam on that region and the wafer was annealed in dry N₂ at 1000°C for 40 minutes in order to diminish surface states. Contacts were etched and Al was deposited by electron beam evaporation. Ohmic contact was obtained by alloying in dry N₂ at 450°C for 30 minutes. The physical characteristics of this process are summarized in Table 1.

In the conventional technique, the field oxide was firstly grown over a whole surface of a silicon wafer by thermal oxidation. This oxide was then etched away with the buffered hydrogen fluoride from the source and the drain areas that were defined by photoresist maskings. After the source and drain diffu-

sion were performed, the oxide was etched away from the gate region, and the gate oxide with thickness of 1050 Å was grown by thermal oxidation. The process ends with the usual operations of Al evaporation, selective etching of Al, and alloy. The processes such as the growth of field oxide and gate oxide, the source and drain diffusion, the annealing, and the formation of Al electrodes, which were common to both techniques were performed respectively at the same time in both techniques.

MOS transistors with the gate of 100 μm in length and 300 μm in width were formed with these techniques respectively. Electrical characteristics, as the threshold voltage and the effective carrier mobility, were measured with these MOS transistors.

3 Experimental Results and Discussion

3.1 Threshold voltage

The threshold voltage (V_T) of MOS transistors is generally defined as the voltage that must be applied to the gate in order to induce a conducting channel. Threshold voltage values in this reports were measured at 1 μA when the drain-to-source voltage was 5 V. V_T was measured as a function of the substrate-to-source voltage (V_{BG}). Fig. 2 shows the measured V_T as a function of $|-2\phi_F + V_{BG}|^{1/2}$ where ϕ_F is the Fermi potential.

Fig. 2 Threshold voltage (V_T) vs. back-gate voltage (V_{BG}) characteristics of flat MOS and conventional MOS transistors

○—○ : Flat MOS
●—● : Conventional MOS

It was found that for *n*-channel devices, V_T of the flat MOS transistor was greater than that of the con-

ventional MOS transistor in the same group of substrate resistivity (ρ). For instance, V_T for the flat MOS transistor with ρ of $1.00 \Omega \cdot \text{cm}$ was 0.90 V , while V_T for conventional MOS transistor with of $0.97 \Omega \cdot \text{cm}$ was 0.26 V at $V_{BG}=0 \text{ V}$. The difference value of V_T between these two MOS transistors became large as V_{BG} was increased as shown in Fig. 2. In p -channel devices, however, V_T was slightly smaller for the flat MOS transistor than for the conventional MOS transistor.

It was also found in Fig. 2 that both for the flat MOS transistors and for the conventional MOS transistors, the relation of V_T vs. $|-2\phi_F + V_{BG}|^{1/2}$ can be closely approximated by a straight line²⁾:

$$V_T = \pm \frac{t_{ox}}{\epsilon_{ox}\epsilon_o} \sqrt{2q\epsilon_{si}\epsilon_o N_{eff}} |-2\phi_F + V_{BG}| + 2\phi_F + V_{FB} \quad (1)$$

where t_{ox} is the gate oxide thickness, ϵ_{ox} and ϵ_{si} are the relative permittivity of SiO_2 and Si, respectively, ϵ_o is the vacuum absolute dielectric constant, q is the elementary charge, N_{eff} is the effective impurity concentration which is obtained from the slope, V_{FB} is the flat-band voltage. The $+$ and $-$ signs apply to n - and p -channel devices, respectively.

We can determine N_{eff} from the slope according to eq. (1). The difference of the slope was ascribed to the difference of N_{eff} , because t_{ox} is equal for all devices. Typical values of N_{eff} obtained for all eight kinds of devices are shown as well as the impurity concentration of the starting substrate (N) in Table 2. The values of N were determined from measured ρ according to Irving's data³⁾.

Table 2 Typical values of N and N_{eff}

Channel type	Technique	ρ ($\Omega \cdot \text{cm}$)	N (cm^{-3})	N_{eff} (cm^{-3})
n	Flat	1.00	1.6×10^{16}	1.88×10^{16}
	Conventional	0.97	1.6×10^{16}	8.60×10^{15}
	Flat	2.10	6.6×10^{15}	6.62×10^{15}
	Conventional	1.95	7.1×10^{15}	4.27×10^{15}
p	Flat	4.10	3.3×10^{15}	3.65×10^{15}
	Conventional	4.00	3.4×10^{15}	2.24×10^{15}

No significant difference between N_{eff} and N was observed in the flat MOS transistor. In the n -channel conventional MOS transistor, however, N_{eff} was substantially smaller than N . It is not distinct in the p -channel conventional device from the data in Table 2, whether N_{eff} was really greater than N , but it will be ascertained, later, that N_{eff} is greater than N .

The difference of V_T between the flat MOS device

and the conventional device with the same ρ was caused by the difference of N_{eff} , which is the effective impurity concentration close to Si-SiO₂ interface beneath the gate oxide.

3.2 Impurity profile

The substrate impurity profile beneath the gate oxide was determined from d. c. characteristics according to Shannon⁹⁾. The results are shown in Fig. 3 and Fig. 4 for n -channel and p -channel devices, respectively. The effective impurity concentrations (N_{eff}) determined from the slopes in Fig. 2 are also shown for comparison.

It was found that, in n -channel devices, the impurity (boron) was remarkably depleted near the Si-SiO₂ interface for the conventional MOS transistor, but the depletion of impurity for the flat MOS transistor was much less. On the other hand, in p -channel devices, no change of the doping level for the flat MOS transistor was observed in the range of measurement, while the impurity (antimony) for the conventional MOS transistor was slightly piled up.

The cause of the difference of the impurity profile between the flat and conventional MOS devices can be thought as following. In conventional MOS devices, the channel region underwent a long time of thermal oxidation when the field oxide was grown before the gate oxidation was performed. Accordingly, boron

Fig. 3 Impurity profiles of boron-doped substrates determined from d. c. measurements on n -channel flat MOS and conventional MOS transistors

- : Flat MOS ($\rho=1.00 \Omega \cdot \text{cm}$)
- : Conventional MOS ($\rho=0.97 \Omega \cdot \text{cm}$)
- N_{eff} : Effective impurity concentration from Table 2

Fig. 4 Impurity profiles of antimony-doped substrates determined from d. c. measurements on *p*-channel flat MOS and conventional MOS transistors.

- : Flat MOS ($\rho=4.30\Omega\cdot\text{cm}$)
- : Conventional MOS ($\rho=4.10\Omega\cdot\text{cm}$)
- N_{eff} : Effective impurity concentration from Table 2

whose segregation coefficient is greater than unity was remarkably depleted^{(7),(10)} and antimony whose segregation coefficient is smaller than unity was piled up near the interface during the long time of thermal oxidation⁽¹⁰⁾. On the other hand, in flat MOS devices, the channel region was not subjected to the thermal oxidation except for the gate oxidation, because the silicon nitride on the channel region acted as a mask against the field oxidation. For that reason, the redistribution of impurity near the Si-SiO₂ interface was much less, if happen, during the field oxidation. Of course, the redistribution during the gate oxidation might happen, but its level was as much as shown in Fig. 3 and Fig. 4 at most in flat MOS devices.

3.3 Effective mobility

The effective carrier mobility (μ_{eff}) in the surface channel was determined from the experimental drain conductance (G) vs. gate voltage (V_G) characteristics at zero drain-to-source voltage according to

$$\mu_{\text{eff}} = \frac{L}{W} \frac{t_{\text{ox}}}{\epsilon_{\text{ox}} \epsilon_0} \frac{G}{(V_G - V_T)} \quad (2)$$

where L and W are the channel length and width, respectively. The value of μ_{eff} depended on V_G and showed the maximum value in the region near $V_g = V_T$ ⁽¹¹⁾.

The maximum value of μ_{eff} , the electron mobility in *n*-channel devices and the hole mobility in *p*-channel devices, obtained for each transistor is shown in Fig. 5 as a function of N . In *n*-channel devices, the maximum value of μ_{eff} was apparently smaller

Fig. 5 The effective mobility (μ_{eff}) against the impurity concentration of the starting substrate (N)

- : Flat MOS
- : Conventional MOS

for the flat MOS transistor than for the conventional MOS transistor at the same N in the range of measurement. In *p*-channel devices, no difference was found in the value of μ_{eff} between the flat and conventional MOS transistors.

The maximum values of μ_{eff} were replotted as shown in Fig. 6 against N_{eff} which was determined by the slope of V_T vs. $|-2\phi_F + V_{\text{BG}}|^{1/2}$ characteristics as in Table 2. Now, the dependency of the maximum μ_{eff} on N_{eff} in the flat MOS transistor is similar to that of the conventional MOS transistor in *n*-channel devices, and the maximum value of μ_{eff} seems to depend on N_{eff} regardless of the device fabrication

Fig. 6 The effective mobility (μ_{eff}) against the effective impurity concentration (N_{eff})

- : Flat MOS
- : Conventional MOS

technique. These facts indicate that the lowering of effective carrier mobility in the n -channel flat MOS transistor was caused by the less depletion of impurity near Si-SiO₂ interface compared to conventional MOS transistor prepared under the same condition.

The reason of the same value of μ_{eff} for the p -channel flat and conventional MOS transistors is thought that N_{eff} of them did not so differ much from each other as the difference of μ_{eff} was brought about. In fact, the dependency of the bulk hole mobility on the impurity concentration is very slight in the region near $1 \times 10^{15} \text{ cm}^{-3}$.

4 Conclusion

It was found that the electrical properties of the MOS transistors prepared by the flat MOS technique are different from those of the conventional MOS transistors. For n -channel devices with the same substrate resistivity, the threshold voltage and the effective carrier mobility of the flat MOS transistors were substantially greater and smaller than those of the conventional MOS transistors obtained under the same condition, respectively. While, for p -channel devices the threshold voltage of the flat MOS transistors was slightly smaller than that of the conventional MOS transistors obtained under the same condition,

and the effective carrier mobility was almost same with that of the conventional MOS transistors.

The difference of both V_T and μ_{eff} can be explained to be due to the fact that the change of the impurity profile near Si-SiO₂ interface caused by the redistribution during the field oxidation was slight in the flat MOS transistors compared to the conventional MOS transistors.

Acknowledgement:

The authors wish to thank Dr. T. Matzokura and Dr. S. Nakanuma for their helpful advice and encouragement.

The authors also thank M. Kaminaka for assistance with the experiments.

(Received March 3, 1973)

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Berichte der Bunsen-gesellschaft für physikalische Chemie 76, No. 11 (1972)

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