Silicon Wafers for 0.25 μm Technology Age. From the Viewpoint of Trends of Silicon Device, Process and Manufacturing Engineering

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The technology trends of LSIs are summarized and the issues predicted on the basis of these trends are described. Then countermeasures from Si wafer technology are discussed. Finally, key items in the future specifications of typical Si wafers are pointed out and the future direction of wafer technology is revealed with deployment of LSI-quality functions to wafer specification items. For the 0.25 μm technology age, the typical wafer specifications of future 256MDRAMs are estimated by extrapolation from the past trends vs. design rule.

1. Introduction

In LSI fabrication, improved control of silicon wafer characteristics is one of the indispensable key factors for realizing superior yield. That is, a deeper understanding of interrelationships among silicon material, ULSI device and process technologies is essential for an approach to higher cost effectiveness and better performance.

Silicon crystal growth technologies have already been discussed elsewhere¹⁾. For example, gettering phenomena have been summarized²⁾, and the amount of oxygen dissolved from the crucible³⁾ or the oxygen behavior in wafer fabrication processes⁴⁾ were investigated in order to control the locations of gettering sinks and the thickness of the denuded zone. Recently, computer simulation has become a very powerful tool to study the melting zone in Czochralski (CZ) crystal growth⁵⁾, which aids in controlling the oxygen contents in CZ silicon.

In this paper, the future direction of silicon wafer technology is described, based on the trends of silicon ULSI device and

process technologies. The purpose of this study is to predict future specifications for silicon wafers. In Sec.2, the technology trends of present and future LSIs are summarized and in Sec.3, the predicted issues in silicon device manufacturing and countermeasures from wafer technologies are described. Finally, in Sec.4, crucial items in the future specifications of a typical silicon wafer are pointed out and the direction of the future silicon wafer technology is predicted with deployment of LSI-quality functions to wafer specification items. As a typical example, the above-noted items of wafer specifications for 256MDRAM are estimated through extrapolation from the past trends vs. design rule. There are few, if any reports which describe the relation between such wafer specifications and the device-design scaling-factor.

2. Technology Trends of LSIs

2.1. Trends in Technology Development

2.1.1. New Device Development

The packing density of memory devices has continuously increased. Figure 1 shows the size and minimum geometry trends of Dynamic RAMs(Random Access Memories). The circles and squares indicate the two stages of device manufacturing namely Development, with data taken from the annual ISSCC(International Solid State Circuit

ULSI Device Development Laboratories, NEC Corporation, (Sagamihara-shi, Kanagawa, 229 Japan)

Key words : Silicon wafer, Specifications, Future trend, Design rule.

Fig.1 The size and the minimum geometry trends of Dynamic Random Access Memories. Development stage (●and○) and peak of volume production (■and□) data are based on ISSCC and WSTS reports, respectively. Squares in parentheses are estimated.

Conference) and Volume Production Peak with data taken from WSTS (World Semiconductor Trade Statistics) for every generation. Solid lines mean actual data and dashed lines indicate future projections. Recently N. Tadano⁶⁾ has also described his predictions. The dot-dashed line and dotted lines show the trends of volume production start and future predictions of volume production starts and peaks, respectively.

As shown in Fig.1, especially in the development trend, the design rule of the state-of-the-art product is approaching the limitation of optical lithography technology, i.e. $\sim 0.2\mu\text{m}$. The characteristics of the starting

material including the flatness and the allowable limit of adhered particle size should also follow this trend.

MPU(Micro-Processor Unit) and ASIC(Application Specific Integrated Circuit) also show the same trend as DRAM's. Thus, demand for flatness and other characteristics of the starting materials for these devices should be the same as those of wafers for DRAMs.

In the memory area, in addition to DRAM, SRAM(Static RAM) and conventional PROM(Programmable Read Only Memory), and more recently, flash memory, should also be watched. Already a 5V-only 16Mbit flash memory has been developed by T. Jinbo et.al.⁷⁾, as shown in Fig.2. 1Mbit and 4Mbit flash memory devices have been commercially available and a commercial 16Mbit flash memory has already been announced. Recently a 64M bit flash memory has been discussed by Takeshima, et al.⁸⁾ Such flash memory structures have a so-called tunnel-gate-oxide, of which the function and properties have yet to be fully understood, and therefore require a deeper physical understanding of the Si-SiO₂ interface. From a practical point of view, an ultra-uniform interface is needed to avoid any local concentration of electric field.

To avoid such interface problems, buried-channel FETs have also been investigated due to their high driving capability and good threshold voltage controllability⁹⁾. A cross-sectional view of a buried-channel pMOS FET is shown as an insert in Fig.3, where potential profile engineering is used to fabricate the n⁺ region in the channel. As shown in Fig.3, the short channel effect is drastically improved in the case of the device with n⁺ regions. In this

Fig.2 A photograph of a 5V-only 16Mbit flash memory developed by T.Jinbo et. al⁷⁾.

Fig.3 An example of improvement of short channel effect in the buried channel pMOS FET. The cross-sectional view obtained by potential-profile-engineering is inserted. (K.Okabe et al.⁹⁾).

structure, a high quality silicon crystal is required, as channels are formed in the bulk silicon.

High quality starting material is more essential in analog devices, such as HDTV(High Definition Television) CCD(Charge Coupled Device) image sensor. The request for highly-uniform crystal-structure inquires MCZ (CZ growth under Magnetic field) crystal growth or epitaxial wafer technology.

The recent supply voltage change, typically from 5V to 3.3V or 3V, should also be noted. Figure 4 indicates hot-electron breakdown-voltage and punch-through-voltage behaviors which depend on the supply

Fig.4 Supply voltage and gate length dependences of punch-through breakdown-voltage of transistors with conventional Source / Drain structures and LDD structures. (After Fukuma, who is a member of the supply voltage research team organized by the author.)

voltage and gate length. Practically, the hot-electron breakdown-voltage, rather than the punch-through-voltage, determines the maximum supply voltage¹⁰⁾. Hot electrons are also affected by Si crystal characteristics, the Si-SiO₂ interface, and SiO₂ characteristics.

2.1.2. New Process Technology Development

In order to fabricate new devices, wafer fabrication technology has been remarkably improved. Especially lithography technology has always been faced with the high barriers of resolution and depth of focus (DOF) in reduction projection aligner. Resolution has been improved by the investigation of NA(numerical aperture) and σ (coherent factor) optimization¹¹⁾, where σ is the NA ratio of the illumination optics and the reduction projection optics from the reticle side. DOF has been investigated by using phase-shift-mask technology and annular illumination¹²⁾. Figure 5 shows the resist pattern profile of 0.25 μ m L/S as a function of focus where annular illumination technology is compared with the conventional one. Even though such improvements have been carried out, the DOF limitation ($\sim 1\mu$ m, in Fig.5) still requires an extreme Si wafer flatness. For example, an

Focus Position	Conventional Illumination	Annular Illumination	4-point Illumination
+0.9 μ m			
+0.7 μ m			
+0.4 μ m			
+0.1 μ m			
-0.2 μ m			
-0.3 μ m			
-0.7 μ m			

Fig.5 Typical examples of resolution and depth of focus (DOF) on the resist pattern profile of 0.25 μ m L/S where annular illumination is compared with conventional one. (K.Tounai et al.¹²⁾)

LTV(Local Thickness Variation defined as the maximum value of thickness variation among more than 55 sites of 15mm^2 in a $6\text{''}\phi$ wafer) of $0.3\mu\text{m}$ is required for 256MDRAM assuming, for instance, a step height difference of approximately $0.5\mu\text{m}$ with an additional $\sim 0.2\mu\text{m}$ due to particles adhered on the wafer backside.

Fig.6 Typical process flows of CMP technology. Damascene type polished from the surface to a-a' line of plug metal film (P1) connected with metallization pattern (M1) and just polishing type from the surface to b-b' line of insulator film (I1) are shown in the cross-sectional views of Fig.A-2 and Fig.B-1, respectively.

On the other hand, with increases in the packing density of LSIs using multi-level metallization or stacked capacitor structures, the height of steps, i.e. the aspect ratio on the Si wafer is also increasing. To avoid the DOF limitation and the difficulties of step-coverage, CMP (Chemical-Mechanical Polishing) technology has recently become highlighted. Figure 6 shows the two types of CMP processes, the so-called damascene type¹³⁾ (6A) and just polishing¹⁴⁾ (6B). In general, the former is used to obtain a metallization pattern and the latter is used to get a flat surface of insulating film and/or metal film. Again, the flatness of the wafer is crucial to control the polished layer thickness.

To fabricate flash memory devices, high reliability of tunnel oxide is essential. It depends not only on the characteristics of Si and SiO₂, but also on the Si/SiO₂ interface¹⁵⁾. Figure 7 shows AFM(Atomic Force Microscopy) results measuring the roughness of the Si/SiO₂ interface depending on the heat treatment temperatures. Figures 7A and 7B were obtained through a 1000°C-thermal oxidation process and through an 800°C HTO CVD(High Temperature Oxide Chemical Vapor Deposition) process using a gas mixture

Fig.7 Heat treatment temperature dependence of the Si/SiO₂ interface roughness. The interface in A is after a 1000°C thermal oxidation process, and that in B is after an 800°C HTO CVD process using SiH₄-N₂O reaction.

of SiH₄ and N₂O, respectively. It is clearly revealed that a lower temperature process gives a smoother interface.

Substantial progress has also been observed in other fields, such as dry etching technology using high density plasma gases, and precise impurity-profile-engineering with high-energy ion-implantation technology, etc. Simulation is now a powerful technology to improve development efficiency. Yokozawa et al presented simulation results of step coverage¹⁶⁾ and the growth mechanism of thin films¹⁷⁾. In order to utilize these technologies effectively, high uniformity over the whole wafer scale is the major premise.

2.2. Trends in Manufacturing Engineering

Cost effectiveness has been continuously pursued. The reduction of the number of process steps and the shrinkage of chip size are very effective. TQC (Total Quality Control), TPM (Total Production Management) and COO (Cost of Ownership) programs and strategies are also useful to improve production efficiency. Reduction of the down-time of production equipment directly relates with the cost. Thus increasing the durability of wafers can reduce costs. Increasing wafer diameter is also effective for cost reduction and recently, 12 to 16-inch-diameter wafers have been investigated¹⁸⁾. In that case, again

Table 1 Requirements from Device Development Trends and Corresponding Subjects of Silicon Wafer Technology.

Requirements	Subjects
<ul style="list-style-type: none"> ○ Reduction of Leakage Current e.g. Stand by Current of 16MSRAM $<1\mu\text{A}$ ○ Low Noise ○ High Quality Image of HDTV CCD 	<ul style="list-style-type: none"> ○ Elimination of Heavy Metal e.g. Gettering Technology Oxygen Control ○ Level of Bulk Characteristics Same as Epitaxial Layer ○ Improvement of Recombination-Generation Rate ○ Improvement of Epitaxial Technology <div style="border: 1px solid black; padding: 2px; width: fit-content; margin: 10px auto;">Improvement of Crystal Quality</div>

the uniformity for every specification is more crucial.

3. Subjects on Si Wafer Technology

3.1. Crystalline Quality Required from Device Technology

From the viewpoint of device progress, leakage current is becoming increasingly serious. For example, in the case of 16Mbit SRAM, the standby current should be less than $1\mu\text{A}$, which means the leakage current should be less than the order of 10^{-13}A/cell . To solve this matter, heavy metals should be eliminated by using various gettering technologies, such as intrinsic gettering and extrinsic gettering sinks. Bulk crystal characteristics should be improved to the level of epitaxial Si, especially in the characteristics of the carrier recombination-generation rate.

To realize low noise and high performance for analog devices, such as HDTV CCD, the above-described technologies are also useful. For low power devices and for flash memory devices, again a high quality wafer is essential. Most of such requirements from the device-technology-trend can be categorized into the improvement of Si crystal quality, as shown on Table 1.

3.2. Polishing Specifications Required from Process Technology

The process technology trend indicates that the DOF limit is becoming crucial. If an

ArF laser (193nm wave length) is to be practical, the DOF must be within the range of $\pm 0.25\mu\text{m}$. This requires improving the value of LTV. Prior to that, however, the technology to measure such small LTV must be established.

Realizing the minimum L/S (line width and space) will also be more difficult. This indicates not only a reduction of particles on processed wafers, but improvement of the detection limit of the particle size. Suppose the allowable particle diameter should be less than half of the alignment accuracy, and the alignment accuracy should be less than one fifth of the minimum L/S, then the allowable particle size should be less than one tenth of the minimum design rule, hence a $0.025\mu\text{m}\phi$ particle for the $0.25\mu\text{m}$ age.

However, since actual wafer fabrication lines have been faced with particle counter detection limits which could not meet the above requirements, such allowable particle size has not yet been proved. Thus, in general, the most effort has been concentrated on reducing the detectable particle numbers with an assumed corresponding reduction in particle size.

From the thin film technology trend, improvement of reliability of gate oxide and tunnel oxide is required. This directly relates with surface roughness of Si wafers and heavy metal contamination.

Table 2 Requirements from Process Technology Development Trends and Corresponding Subjects of Silicon Wafer Technology.

Requirements	Subjects
<Lithography> ○ Enough Margin of DOF ○ Enough Margin for Min. L/S.	○ Improvement of LTV ○ Reduction of Particle Number ○ Reduction of Particle Diameter ○ Reduction of Surface Roughness ○ Reduction of Heavy Metals ○ Reduction of Warpage Improvement of Polishing Technology
<Thin Film> ○ Improvement of Gate Oxide. ○ Improvement of Tunnel Oxide	
<Metallization> ○ Coverage & CMP	

Table 3 Requirements from Manufacturing of Silicon Device Products and Corresponding Subjects of Silicon Wafer Technology.

Requirements	Subjects
○ Large Diameter ○ Cleanness ○ Global Production ○ Reduction of Number of Process Steps ○ Reduction of Chip Size ○ Improvement of Up-Time of Production Equipment ○ Standardization	○ Stable Supply ○ Improvement of Wafer Cleaning Technology ○ Improvement of Packaging Technology ○ Retention of Gettering Effects ○ Enforcement of Counter Measures for Leakage Current ○ Strengthening against Wafer Breakage ○ Improvement of Uniformity Cost Effectiveness for Every Specification

For multi-level metallization, step coverage and planarization, such as CMP, require reducing the warpage of the Si wafer. All items described in this section resolve themselves into the improvement of wafer polishing technology, including wafer cleaning, as summarized on Table 2.

3.3 Cost Effectiveness Required from Manufacturing Engineering

In order to reduce the cost of products, manufacturing engineering requires various means, such as an increase of the Si wafer diameter, reduction of the number of process steps, reduction of the chip size, and standardization of Si wafer specifications, etc. Even though the number of process steps are reduced, the gettering effect should be retained. And even if the chip size is shrunk,

the leakage current should still be minimized to meet the circuit design.

To improve the production yield, the cleanness of Si wafers, tight packaging technology to keep wafers contamination-free, and the reduction of the down-time of production equipment are all important factors. A durable wafer structure is especially required to avoid Si dust generation if the wafer is broken in production equipment. Rounding the edge of Si wafers is one of the ways of achieving such durability. All of the items described above relate to the cost effectiveness, as indicated on Table 3.

4. Direction of Si Wafer Specifications for Future Products

The demands on the basis of both trends of semiconductor development and production are summarized on Table 4, where the tight(○) and tighter(◎) relationships within these key items of the required quality and the countermeasure specifications are shown. Required items come from three major areas, i.e. device technology, process technology and manufacturing engineering, which are previously described in Secs. 2.1.1 and 3.1,

Table 4 Relationships between Si Wafer Specifications and Demands on the Basis of Trends in Device and Process Technologies and Semiconductor Manufacturing Engineering.

Quality Required	Specification Major Item	Polishing					Crystal Characteristics		
		Particles	Scratch	Contaminants	LTV	Warpage	Gettering Sinks	Defect Density	p.e. top etc
Device Technology	Leakage Current	○ ○ ○					○ ○ ○		
	Retention Time	○ ○ ○					○ ○ ○		
	Low Noise			○			○ ○ ○		
	Oxide Reliability	◎ ○ ○					○ ○		
Process Technology	Design Automation								◎
	Alignment Accuracy	○			○ ○				
	DOF Budget	◎			○ ○				
	Planarization				○ ○				
	Step Coverage				○ ○				
	Thin Film Quality	○ ○ ○					○ ○		
Manufacturing Technology	Thin Film Reliability	◎ ○ ○					○ ○		
	Large Wafer (8" x)	○ ○ ○ ○ ○ ○					○ ○ ○ ○		
	Cleanness	○ ○ ○							
	Packaging	◎ ○ ○							
	Durability	○ ○ ○							
	Cost Effectiveness	○ ○ ○ ○ ○ ○					○ ○ ○ ○		

2.1.2 and 3.2, and 2.2 and 3.3, respectively. Corresponding to these, the subjects in the wafer specifications are categorized into two major groups, i.e. the crystalline quality of bulk and epitaxial Si, and the quality of polishing. The crystalline quality includes the gettering sinks of oxygen contents (Oi) and backside damage and various defect controls in addition to the usual items of more precisely controlled resistivity, and epitaxial layer thickness, etc. The polishing quality includes the reductions of particle number and particle size, contamination related matters and LTV, warpage, etc. Table 4 is a summary sheet of the results of analysis with a quality function deployment method¹⁹⁾.

As indicated on Table 4, the technology trends of the device and the process require the improvement of crystalline characteristics and polishing technologies, respectively. The manufacturing trend requires both. In the crystalline characteristics, gettering-sink-related matters, such as Oi, backside damage, defect density will be more important and the severeness in the specification values is increasing. In the polishing technology, the LTV, warpage and particle-related items should be noted. For every item, uniformity should be emphasized.

As a typical example, Table 5 shows the trends of the Si wafer specifications for fabrication of DRAM devices. The specification items focused here correspond to the items noted as tighter relationship between the device side requirements and wafer characteristics(◎ on Table 4). From 1MDRAM to 16MDRAM the values are actual ones and for 256MDRAM the values are obtained by extrapolation from the past trends.

Figures 8,9 and 10 were used for the estimation of the 256MDRAM wafer specifications and Table 6 shows a summary of the empirical relationship between each specification item and the device-design scaling-factor S.

In Fig. 8, the allowable particle size (A) and the upper limit of number-of-adhered-particles/wafer-area(B) are plotted as functions of design rules of DRAM shown as

Table 5 Trend of Si Wafer Specifications in DRAMs.

DRAM(bit)	1M	4M	16M	64M	256M
Wafer Diameter(inch)	6	6	8	8	12~16(?)
Particle Size(μm)	>0.3	>0.3	>0.3	>0.16	>0.10
Number(1/W)	<30	<30	<30	<20	<10
Warpage(μm)	<20	<20	<20	<20	<20
LTV(μm)	<1.0	<0.8	<0.6	<0.5	<0.3
Gettering Sink e.g. Oi(Normalized)	1	0.88	0.88	0.84	0.84
Defect Density e.g. OSF(1/cm ²)	<20	<20	<20	<10	<5
Uniformity e.g. Deviation of ρ_g (%)	± 5	± 5	± 3	± 3	± 3
Quality	NIG&DZIG	DZIG	Clean DZIG	(Epitaxial-Like)	(Epitaxial-Like)

Fig.8 Allowable particle size (A) and particle number (B) trend vs. design rule.

the minimum geometry in Fig. 1. The design rule is a function of scaling factor S . If the particle size relates to an electrical short

between two conducting lines, the size is a function of S , i.e. the slope factor $k=1$ in Fig. 8A. The actual data, however, lie neither on $k=1$ nor $k=2$. Presumably the deviation is due to the detection limit of the particle counter, that is, the past specification numbers were limited by the counter capability, thus the past data cannot prove the estimated relationship. The extrapolated value, however, may be appropriate because the plot($\circ$) is approaching on a line with a slope factor $k=1$.

Figure 8B shows the actual relation between the design rule and chip size. The slope factor k is -1 . If the allowable particle number is a function of $S/\text{chip-size}$, the particle number is determined by $S/S^{-1}=S^2$, i.e. $k=2$. In Fig. 8B, the particle-number/wafer-area is plotted as a function of design rule and the estimated value for the $0.25\mu\text{m}$ age($\circ$) is near the line of $k=2$. The past actual data show nearly $k=1$, which may have been affected by the detection limit.

Figures 9A and 9B show the warpage/wafer-area and LTV as a function of design rule, respectively. Both plots indicate the slope factor k is equal to 1 and the estimated values ($\circ$ in Figs. 9A and 9B) are on the extrapolated lines from their past trends.

Figures 10A and 10B illustrate the relations of OSF and $\Delta\rho_s/\rho_s/\text{wafer-area}$ with design rule, respectively. Both cases indicate a

Fig.9 Warpage / wafer-area (A) and LTV (B) vs. design-rule.

slope factor k of 2, and the estimated values of OSF and $\Delta\text{ps}/\text{ps}/\text{wafer-area}$ are on lines extrapolated from past trends.

Oxygen content O_i is difficult to discuss with the design rule relationship, because the value of O_i does not show a remarkable change although the OSF value originated by O_i has drastically changed in this range. In addition, the number of O_i strongly depends on individual production lines. Therefore, in this paper, the O_i value of 256MDRAM is just extrapolated from the value of 64MDRAM. In general, the O_i value must be adjustable to get the maximum yield from a fabrication line.

The crystalline quality trend indicates a more perfect crystalline structure than that used in the previous generation. From that point of view, for 256MDRAM the required quality will be "epitaxial-like" with a leakage current of $10^{-14}\text{A}/\text{cell}$.

5. Conclusion

Technology trends of the LSI-device- and process- development and manufacturing engineering have been summarized. On the basis of these trends, major issues have been indicated and solutions to the issues have been

Fig.10 Oxidation-induced Stacking Fault density (OSF) (A) and rs deviation/wafer-area (B) vs. design-rule.

discussed from wafer technology. Then, with a deployment of quality functions of the requirements from device side to the silicon characteristics, the future specifications of Si wafers can be predicted.

For the $0.25\mu\text{m}$ technology age, from the view point of the wafer-fabrication process-technology-trend, the items of particles and thickness variation, and from the view point of the device engineering trend, the items of gettering sinks, defect densities and uniformity will be crucial. For 256MDRAM designed with a $0.25\mu\text{m}$ rule, the allowable particle number/12~16 inch wafer will be less than 10 for particle sizes of larger than $0.10\mu\text{m}$. The warpage of a 12~16 inch wafer will be in the range of less than $20\mu\text{m}$ and LTV will be required under a level of $0.3\mu\text{m}$. The oxygen contents tend to decrease roughly 16% compared with the 1MDRAM age. The OSF will be required to be less than $5/\text{cm}^2$ and the deviation of ps will be required as $\pm 3\%$ on 12~16 inch wafer. These estimated values are confirmed by the extrapolation of each trend vs. design rule. The empirical relations between these wafer specification trends vs. design rule are summarized on Table 6. In

Table 6 Empirical Relations between Si Wafer Specifications and Design-rule Scaling-factor S.

Particle Size (μm)	S
Particle Number ($1/\text{cm}^2$)	S ²
Warpage / Wafer Area ($1/\text{cm}$)	S
LTV (μm)	S
OSF ($1/\text{cm}^2$)	S ²
$\Delta\rho_g/\rho_g$ / Wafer Area ($\% / \text{cm}^2$)	S ²

general the improvement of the bulk crystalline quality will be increasingly critical from generation to generation to approach the quality level of an epitaxial layer.

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