1. Introduction

The ability to perform serial-to-parallel conversion (SPC) of high-speed data signals is critical in optical communications as it resolves the mismatch between the optical data rate and the speed of current Silicon-CMOS technology, thus allowing the application of CMOS circuits for signal processing and buffering. In particular, for future optical packet-switched (OPS) networks [1]-[3], SPC of high-speed, asynchronous burst optical packets would enable key packet processing functions of label processing and buffering to be carried out by CMOS circuits, leading to a high-performance, highly scalable approach to optical packet switching [1]. However, for achieving such an interface, current electrical demultiplexers may be insufficient in terms of speed, consume large amounts of power, and are ill-suited for the burst mode operation required for an asynchronous input.

We will review two approaches for SPC of asynchronous burst, preamble-free optical packets. The first is an optoelectronic approach targeted for 10-Gb/s to >40-Gb/s packets, based on an optically clocked transistor array (OCTA). SPC and parallel-to-serial conversion (PSC) (i.e., multiplexing), as well as generation of the clock required for both conversion functions are achieved with a single, low-power optoelectronic integrated circuit (OEIC) chip [4]. The second is an all-optical approach which employs optical switching by means of differential spin excitation, for SPC of 40-Gb/s to 1-Tb/s optical packets [5].

2. Optoelectronic Approach

Operation of the OCTA is illustrated by Fig. 1. A photodetector (PD) first converts the input optical packet to an electrical signal. As the signal propagates down a transmission line, it is sampled by triggering an array of optically triggered electrical switches attached to the line (Fig. 1a)). The switch consists of a discharge-based metal-semiconductor-metal (MSM) PD driving a high-electron-mobility-transistor (HEMT) switch. With the input charge time constant \( t_{in} = R_{in}C_{in} \) of the PD set much longer than the output discharge time constant \( t_{out} = (R_{MSM} + R_{bias}/2) \times C_{in} \), the bias across the MSM approaches zero when triggered by an optical pulse, resulting in a reduction of the photoresponse tail to generate an ultrafast electrical clock pulse (FWHM \( \approx 3.3 \) ps [1]) for modulating the HEMT switch. With each switch/channel sampling a particular periodic time slot, the entire packet is written in parallel into CMOS circuits (SPC). Furthermore, when a leading optical trigger pulse adequately discharges \( C_{in} \), the PD response to subsequent pulses is eliminated, thus enabling the input optical packet itself to be employed as the trigger.

Fig. 1. Diagrams illustrating a) SPC and b) PSC with OCTA. A pulse or packet may be used for the optical trigger.

Fig. 2. a) Cross-correlation measurement results with 8-ch OCTA (left) and discriminated output (right). b) PSC output.

(self-clocked operation). For reading out processed packets from CMOS with the same device, the packet signal is entered in parallel from the CMOS circuit into the switches through the MSM bias nodes (\( V_{bias} \)), a high voltage for a “1” and zero volts for a “0” (Fig. 1b)). At the same time, the hold capacitors (\( C_{H} \)) are charged HIGH through reset transistors. Optical triggering generates the packet as a serial voltage signal (PSC), with a modulator (EAM) and laser (LD) performing electrical-to-optical conversion to produce the output optical packet.

The bidirectional SPC and self-clocked operation described above are particularly suited for processing short, fixed-length packets, as required for the label processing/swapping function. In this case, the number of channels equals the number of packet bits, with the optical trigger for each channel created by simply splitting and
appropriately delaying a portion of the input optical packet [4].

An eight-channel OCTA was fabricated in a 0.18-μm gate length HEMT OEIC technology. Each channel of the array was used to sample a 40-Gb/s, 16-bit input packet in self-clocked operation. The left of Fig. 2a) shows cross-correlation measurement results, with the output held signal plotted versus relative phase of the trigger. A comparator circuit discriminated the outputs at a fixed trigger phase (dotted line, Fig. 2a)), with results shown on the right. Successful SPC of the first eight packet bits is observed. Using the same device, two different 8-bit parallel signals were converted to their corresponding 40-Gb/s serial signals (Fig. 2b)). Electrical power consumption of the OCTA was only 8 mW per channel. The entire array occupies a $1.5 \times 2.5$ mm$^2$ area. Multiple functions realized within a low-power, single-chip OEIC enables a compact, low-power label swapper.

3. All-Optical Approach

Fig. 3 illustrates the all-optical SPC scheme. The input optical packet is first split into N-delay lines which differ by the bit period ($N=16$ in figure) and output in a two-dimensional array using a surface-emitting planar lightwave circuit (PLC). The orthogonal components of the output beams are then separated with a polarization beam splitter (PBS), and focused onto a pair of surface reflection all-optical switches which contain a 1-μm-thick multiple quantum well (MQW) active layer. Clock/pump pulses with opposite circular polarization enter the switch such that the time window between the two contains N consecutive bits of the packet (Upper left, Fig. 3). As a result of spin-selection rules, only spin-down carriers are excited by the first pump pulse to induce a spin-dependent absorption saturation, causing the polarization of the reflected beams to become elliptical and a subsequent parallel output to the right of the PBS. The energy of the second pump pulse is adjusted so that spin equilibrium is restored, with the reflected beams becoming linearly polarized again and no output. Thus, with the switching window defined by the position of the two pump pulses, only packet bits within the time window are output in parallel to achieve SPC. Subsequent optical-to-electrical conversion is performed using a slow PD array, with the output written into CMOS circuits. Handling the orthogonal components of the input with separate switches leads to polarization insensitivity.

The SP converter module of Fig. 3 was used to perform SPC of two different 100-Gb/s, 16-bit optical packets. Switch extinction ratio was improved (~38 dB) by attaching isolators composed of Faraday rotators and polarizers to the PBS. Fig. 4 shows the input serial packet waveforms, and camera images of the corresponding output parallel signals. High contrast, high-speed conversion is observed for both results.

Although the experimental results described above are for fixed-length packets, conversion of longer, arbitrary-length packets requires generation of an optical pulse train clock with repetition rate equal to the packet data rate divided by the number of parallel channels, and duration matching that of the input packet. An Optical Clock Pulse Train Generator (OCPTG) device has been demonstrated in previous work for generating this clock [6].

4. Conclusion

Two compact, low power approaches for SPC of high-speed, asynchronous burst optical packets have been described. The OCTA integrates multiple functions into a single OEIC chip for a compact, simplified solution to label processing, while the all-optical approach provides ultrafast SPC capability.

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References