Molecular Dynamics Simulation of Void Generation during Annealing of Copper Wiring

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In the production of LSIs, annealing is necessary to coarsen the crystal grains in the wires. In this process, wiring breakdown is frequently caused by defect generation at the T-shaped buried wire. To overcome this difficulty, we investigated the conditions for defect generation and the atomic behavior during the annealing process by molecular dynamics simulation. We focused on the influence of the adhesion strength between substrate and wire materials on void generation. As samples for the simulation, a Cu single crystal was buried in three different substrates, Si, Ti, and W. After structural relaxation at low temperature (50 K), the movements of individual Cu atoms were simulated for different annealing temperatures using the molecular dynamics method. The strain of the buried wire was also varied where the thickness of the covered layer, the width and the height of the wire were fixed. We found that the system with strong adhesion strength between substrate and wire materials suppressed void generation. [doi:10.2320/matertrans.MRA2008477]

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1. Introduction

In recent years, copper instead of aluminum has come to be generally adopted as the wiring material in LSIs so as to decrease the electrical resistance. Different production techniques are required for the copper interconnects on the patterned insulator layer because the copper film cannot be patterned for the interconnect using the same conventional etching process as for aluminum film.^{1,2)} The damascene process is commonly utilized to prepare the multi-layer structure composed of the copper interconnect and the insulator.^{3,4)} In this process, the covered layer on the wire is removed after the copper deposition on the patterned insulator layer.^{5,6)}

After the deposition of the copper layer, an annealing process is necessary to coarsen the crystal grains in the wire. Coarse crystal grains increase the resistance strength to electromigration and simultaneously decrease the electrical resistance.^{7,8)} However, wiring breakdown is frequently caused by the void generation at the base of the T-shaped buried wire during annealing. To overcome this difficulty, we investigated the conditions for the void generation and the atomic behavior during annealing by molecular dynamics simulation.

2. Calculation Method

2.1 Outline of simulation procedure

The specimen for simulation study is composed of a substrate, wire and covered layer. As the substrate mimics the patterned insulator layer, three rigid plates, i.e. two side walls and a bottom plate, are placed in a rectangular parallelepiped shape. Then, a copper single crystal is assumed as the wiring material and the covered layer material. The free boundary condition is set along the vertical direction of the covered layer, and the periodic boundary condition along the other directions.

After relaxation at a low temperature (50 K) to stabilize the structure, an annealing temperature is set. Temperature is controlled with *ad hoc* velocity scaling. Relaxation time and annealing time are 10 ps and 20 ps, respectively. Simulation parameters are the annealing temperature and the strain of the wire, where the thickness of the covered layer, and the width and the height of the wire are fixed.

2.2 Structure of wire

At first, Cu single crystal is produced and cut into the shape of a T for the wire. Then three rigid plates are set as two side walls and one bottom plate as substrate. The orientations between Cu and the substrate are: Cu [100] // wire direction, Cu [010] // normal to the side wall, and Cu [001] // normal to the covered layer. The distance between surface atoms and the bottom rigid plate is set to be the stable distance of the Morse potential which models the interaction between a Cu atom and the substrate.

Then the position of the side walls is varied to change the volume of the buried wire. The ratio of the change of the volume is defined as the strain of the buried wire. Figure 1 summarizes the specimen setting process. The dimension of the calculated system containing both Cu atoms and substrate is shown in Table 1. The strain of the wire is defined as follows (see Fig. 2): Let the equilibrium distance of Cu(100) plane be $d(100)$ and the equilibrium distance between Cu atom and the substrate be r_0 . The wire width with no strain, W_0 , is calculated as

$$W_0 = 3 \times d(100) + 2 \times r_0. \quad (1)$$

The value of $d(100)$ is taken from that of the bulk, 0.361 nm, and r_0 is assumed to be the same as the Morse potential parameter r_0 (see section 2.3 and Table 2). The determined values of W_0 were 1.583 nm, 1.603 nm, and 1.623 nm for Cu-Si, Cu-W and Cu-Ti system, respectively. Then the wire width is changed from W_0 to W and the wire strain $\delta(\%)$ is defined as

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Fig. 1 Setting process for specimen.

Table 1 Calculation conditions for the reference system.

Dimensions (nm)	$2.89 \times 4.33 \times 4.51$
Number of atoms	1806
Strain (%)	0
Width of wire (nm)	1.08
Height of wire (nm)	3.88
Thickness of covered layer (nm)	0.361

Table 2 Parameters of Morse potential.

Surface boundary	Cu/Si	Cu/W	Cu/Ti
D_e/aJ	0.194	0.150	0.112
α/nm^{-1}	13.7	14.7	12.7
r_0/nm	0.25	0.26	0.27

Fig. 2 Schematic of wire structure with no strain.

$$\delta = \frac{W - W_0}{W_0} \times 100 (\%). \quad (2)$$

The number of the inserted Cu(200) layers is fixed to be 7 regardless of the value of W .

At first, we get a void free reference system in a preliminary calculation. The heat-treatment temperature and strain in wire are then changed from those of the reference system to find the conditions which produce voids. Table 1 shows the calculation conditions for the reference system. The time integral of the atomic motion is calculated by the velocity Verlet method. Δt is set to 1 fs.

2.3 Interaction potentials

The interaction between Cu atoms is calculated by the extended Tersoff potential.^{9,10)} This potential is based on the Tersoff potential, and can reproduce the energy of a semiconductor, metal, oxide and other compounds.^{11,12)} It is shown in the Appendix. The interaction between atoms and rigid plates is calculated by the Morse potential to save calculation time.¹³⁾ The substrate is composed of rigid plates that interact with Cu atoms through a two-body Morse potential. Therefore the effect of atomic arrangement of substrate atoms is not considered here, only the strength of the interaction between substrate and Cu atoms is considered.

Figure 3 shows the Morse potentials for Cu-Si, Cu-W and Cu-Ti interaction as a function of the distance between Cu atoms and substrates. The Morse potential parameters, r_0 , D

Fig. 3 Morse potential curves of Cu-Si, Cu-W and Cu-Ti.

Fig. 4 Change of atomic arrangement with 2% compressive strain in 300 K heat-treatment for Ti substrate. (a)–(c) are arrangements at 10 ps, 20 ps and 30 ps, respectively.

Fig. 5 Change of atomic arrangement with 2% tensile strain in 300 K heat-treatment for Ti substrate. (a)–(c) are arrangements at 10 ps, 20 ps and 30 ps, respectively.

and α were determined as follows. Firstly, the potential curves of the interaction between Cu and substrate atoms (Si, W and Ti) were calculated using the extended Tersoff potential. Then the parameters r_0 and D were determined as the equilibrium distance and the minimum of the potential curve, respectively. Finally, the rest parameter α was determined by best fitting to the potential curve.

The equation of the Morse potential is

$$\phi(r) = D\{\exp[-2\alpha(r - r_0)] - 2\exp[-\alpha(r - r_0)]\}, \quad (3)$$

where r is the nearest distance between a Cu atom and the substrate. The determined parameters are listed in Table 2.

3. Results and Discussion

Simulation results were visualized to estimate the void generation. Figure 4 represents the change of atomic arrangements with 2% compressive strain for Ti substrate. Voids were absent at the base of the T-shaped wire. The covered layer was attracted to the wire, and the single crystal in the wire changed to the polycrystal with several grains. We considered that local strain remained in the wire because voids were not generated. In contrast, Fig. 5 represents the change of atomic arrangements with 2% tensile strain. Voids were generated at the base of the T-shaped wire. The atomic arrangement in the wire became more ordered than in Fig. 4.

Fig. 6 Void generation map as a function of the strain and annealing temperature for the Ti substrate cases.

Fig. 7 Void generation map as a function of the strain and annealing temperature for the W substrate cases.

Fig. 8 Void generation map as a function of the strain and annealing temperature for the Si substrate cases.

We considered that the local strain was relaxed by the void generation. In this manner, simulation results were classified as showing void suppression or void generation.

Figure 6 represents the void generation map as a function of the strain and annealing temperature for the Ti substrate cases. The plus sign of strain represents tensile strain and the minus sign, compressive strain. More voids were generated when the annealing temperature was higher and the tensile strain was larger; i.e. the higher the annealing temperature, the easier the void generation. Figure 7 represents the void generation map as a function of the strain and the annealing temperature for the W substrate cases. Void generation was

Fig. 9 Atomic arrangement of the system with 1% compressive strain on Si substrate after 300 K heat-treatment.

Fig. 10 Atomic arrangement of the system with 1% compressive strain on Si substrate after 750 K heat-treatment.

suppressed when the strain was less than 1%. The result was not dependent on the annealing temperature. Thus, the void generation could be suppressed for tensile strain up to 1% because the strength of Cu and W substrate atoms was larger than that of Cu and Ti substrate atoms (cf. D values in Table 2). Figure 8 represents the void generation map as a function of the strain and the annealing temperature for the Si substrate cases. The voids were suppressed when the annealing temperature was higher, which was opposite the trend seen for the Ti substrate. The influence of the annealing temperature on the void generation differed among the three kinds of substrates, Ti, W and Si. We could attribute this to the difference of the adhesion strength between Cu and substrate atoms. The annealing temperature dependence for the Si substrate cases could be explained by comparing the results between 300 K and 750 K heat-treatment with 1% compressive strain. Figure 9 represents the atomic arrangements after the 300 K heat-treatment with 1% compressive strain. The top of the covered layer became concave because it was drawn towards the bottom. Figure 10 represents the atomic arrangements after the 750 K heat-treatment temperature with 1% compressive strain. The concave of the top of the covered layer was larger. This showed that atomic diffusion by 750 K heat-treatment was enhanced over that by 300 K heat-treatment.

The above results showed how the difference of adhesion strength affected the void formation: (1) In the case of Si substrate, the Cu atoms in the covered layer tended to move toward the side wall surfaces of the buried wire. This movement of the Cu atoms decreased the total energy of the system due to the strong adhesion strength between the Cu

atoms and the substrate. The higher the heat-treatment temperature, the more suppressed the void formation was because the movement of Cu atoms was much easier (Figs. 9 and 10). (2) In the case of Ti substrate, the Cu atoms in the buried wire tended to move so that the area of Cu-Ti interface was decreased, leading to void generation. This movement of the Cu atoms decreased the total energy of the system because of the weak adhesion strength between the Cu atoms and the substrate. This phenomenon can be seen even in the 0% strain case, indicating that the effect of strain on void generation is not strong as that of adhesion strength. The higher the heat-treatment temperature, the more enhanced the void formation was because the movement of Cu atoms was easier.

4. Conclusions

By using the molecular dynamics method, we did simulations of annealing for the copper wiring in LSIs. Simulation parameters were the annealing temperature and the strain of the wire on three different substrates. Simulation results were classified as showing void suppression or void generation, and the void generation maps were obtained as a function of the strain of the wire and the annealing temperature. The results obtained are summarized as follows.

The temperature dependence of void generation was different among the three kinds of substrates with different adhesion strength. When adhesion was strong, the void generation could be suppressed even at high heat-treatment temperature.

The atoms of the covered layer were pulled into the wire by heat-treatment when the adhesion between wire and substrates was strong. The atoms moved more easily with heat supply, and formed a more stable structure, and that led to suppression of the void generation.

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Appendix: Extended Tersoff potential

Equations of the extended Tersoff potential between i and j atoms are shown in eq. A·1.

$$\begin{aligned}
 U_T &= \sum_{i<j} u_{ij} + \sum_i \phi_i, \\
 \phi_i &= [(I_{Ei} + A_{Ei})/(2e)]q_i + [(I_{Ei} - A_{Ei})/(2e^2)]q_i^2, \\
 u_{ij} &= u_{\text{REP}ij} + u_{\text{SHT}ij} + u_{\text{ION}ij} + u_{\text{VDW}ij}, \\
 u_{\text{REP}ij} &= f_{\text{S}ij} A_{ij} \exp(-\lambda_{ij} r_{ij}), \\
 u_{\text{SHT}ij} &= -f_{\text{S}ij} b_{ij} B_{ij} \exp(-\mu_{ij} r_{ij}), \\
 u_{\text{ION}ij} &= f_{\text{L}ij} \eta_i \eta_j q_i q_j / (4\pi \epsilon_0 r_{ij}), \\
 u_{\text{VDW}ij} &= -f_{\text{L}ij} \sqrt{(C_{\text{VDW}i} C_{\text{VDW}j})} / r_{ij}^6, \quad (\text{A}\cdot 1)
 \end{aligned}$$

where

$$\begin{aligned}
 b_{ij} &= \left[1 + \left(\beta_i \sum_k \zeta_{ijk} \right)^{n_i} \right]^{-1/(2n_i)}, \\
 \zeta_{ijk} &= f_{\text{S}ik} \exp[\mu_{ij}^{m_i} (r_{ij} - r_{ik})^{m_i}] \\
 &\quad \times \{1 + c_i^2/d_i^2 - c_i^2/[d_i^2 + (h_i - \cos \theta_{ijk})^2]\}, \\
 f_{\text{S}ij} &= f_c(r_{ij}, \sqrt{R_{\text{Si}} R_{\text{Sj}}}, \sqrt{S_{\text{Si}} S_{\text{Sj}}}), \\
 f_{\text{L}ij} &= f_c(r_{ij}, \sqrt{R_{\text{Li}} R_{\text{Lj}}}, \sqrt{S_{\text{Li}} S_{\text{Lj}}}),
 \end{aligned}$$

$$\begin{aligned}
 f_c(r, R, S) &= \begin{cases} 1, & (r \leq R) \\ 1/2 + (1/2) \cos[\pi(r - R)/(S - R)], & (R < r < S) \\ 0, & (r \geq S) \end{cases}
 \end{aligned}$$

$$\lambda_{ij} = (\lambda_i + \lambda_j)/2,$$

$$\mu_{ij} = (\mu_i + \mu_j)/2,$$

$$A_{ij} = \sqrt{A_{\text{Si}} A_{\text{Sj}}},$$

$$B_{ij} = \sqrt{B_{\text{Si}} B_{\text{Sj}}},$$

$$A_{\text{Si}} = A_i \exp(\lambda_i D_i),$$

$$B_{\text{Si}} = B_i \exp(\mu_i D_i) [a_{\text{Bi}} - |b_{\text{Bi}}(q_i - Q_{\text{Oi}})|^{n_{\text{Bi}}}],$$

$$D_i = D_{\text{Ui}} + |b_{\text{Di}}(Q_{\text{Ui}} - q_i)|^{n_{\text{Di}}},$$

$$b_{\text{Di}} = (D_{\text{Li}} - D_{\text{Ui}})^{1/n_{\text{Di}}} / (Q_{\text{Ui}} - Q_{\text{Li}}),$$

Table A·1 Potential parameters for interconnect structures.

	Cu	Ti	W	Si
A (10^{-18} J)	128.5	90.4	740.0	293.33
B (10^{-18} J)	6.92	6.86	26.5	75.491
λ (10^{10} /m)	2.83	2.26	2.94	2.4799
μ (10^{10} /m)	1.412	1.127	1.467	1.7322
β	0	0	0	1.0999×10^{-6}
N	1	1	1	0.78734
M	1	1	1	3
C	0	0	0	1.0039×10^5
D	1	1	1	16.218
H	0	0	0	-0.59826
R_{S} (10^{-10} m)	2.82	3.16	3.56	2.6
S_{S} (10^{-10} m)	3.33	3.74	4.11	3.0
R_{L} (10^{-10} m)	1.1	1.1	1.1	1.1
S_{L} (10^{-10} m)	5.0	5.0	5.0	5.0
I_{E}/e (J/C)	7.72	6.82	7.98	8.15
A_{E}/e (J/C)	0.90	1.24	0	0.60
Q_{L}/e	-6	-4	-2	-4
Q_{U}/e	2	4	6	4
D_{L} (10^{-10} m)	1.49	1.58	1.59	1.62
D_{U} (10^{-10} m)	-1.12	-1.44	-1.46	-1.54
n_{B}	10	10	10	10
η	1	1	1	0.930
C_{VDW} (Jm^6)	0	0	0	0

$$n_{\text{Di}} = \ln[-D_{\text{Ui}}/(D_{\text{Li}} - D_{\text{Ui}})] / \ln[Q_{\text{Ui}}/(Q_{\text{Ui}} - Q_{\text{Li}})],$$

$$b_{\text{Bi}} = |a_{\text{Bi}}|^{1/n_{\text{Bi}}} / \Delta Q_i,$$

$$a_{\text{Bi}} = 1/(1 - |Q_{\text{Oi}}/\Delta Q_i|^{n_{\text{Bi}}}),$$

$$Q_{\text{Oi}} = (Q_{\text{Ui}} + Q_{\text{Li}})/2,$$

$$\Delta Q_i = (Q_{\text{Ui}} - Q_{\text{Li}})/2,$$

The potential energy of the system U_T is calculated as the summation of repulsive energy $u_{\text{REP}ij}$, short-range energy $u_{\text{SHT}ij}$, ionic bond energy $u_{\text{ION}ij}$, van der Waals energy $u_{\text{VDW}ij}$ and the energy of atom i itself ϕ_i . q_i is the charge of atom i , and is optimized at every step to minimize U_T . The potential parameters for Cu, Ti, W and Si are listed in Table A·1.