In-Situ Transmission Electron Microscopy Investigation of the Interfacial Reaction between Er and SiO₂ Films

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We fabricated metal-oxide-semiconductor (MOS) devices with a high-k Er-silicate gate dielectric, and demonstrated their electrical performance. The increase in the rapid thermal annealing (RTA) temperature leads to a reduction of the equivalent oxide thickness (EOT), which is attributed in part to the thickness evolution of Er-silicate film and to the chemical bonding change from an Si-rich to an Er-rich silicate. The *in-situ* investigation of the interfacial reaction between the Er and SiO₂ film using a high-voltage electron microscopy (HVEM) revealed a linear relationship between the squared thickness of Er-silicate layer and *in-situ* annealing time, indicating that the Er-silicate growth is a diffusion-controlled process. The parabolic growth constants of the Er-silicate film were calculated to be 2.3×10^{-16} and 9.3×10^{-16} cm²/s for *in-situ* annealing temperatures of 350 and 450°C, respectively. [doi:10.2320/matertrans.M2009371]

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1. Introduction

Over the past few decades, SiO₂ has been widely used as it is considered a near-perfect gate dielectric material for metal-oxide-semiconductor field-effect transistors (MOSFETs). There is an ever-increasing need for improvement in the performance of MOSFETs, and their geometries have been scaled to the point where the SiO₂ gate dielectric has become just a few atomic layers thick. At such thicknesses, the excessive direct tunneling results in an undesirable high off-state leakage current, which is the main cause of the increase in power dissipation and heat in devices.^{1,2)} It is crucial, therefore, to switch away from the traditional SiO₂ to a new insulating material with a higher dielectric constant, referred to as a high-k material, which enables a relatively larger physical thickness with the same gate capacitance.^{3,4)} Significant efforts have been made to explore an implementation of various high-k gate dielectrics in devices, and demonstrate their electrical and structural properties. Among them, Hf-based dielectrics have attracted much attention for their promising electrical and chemical properties, such as reasonably high dielectric constants, relatively large band gaps, and a thermal stability in contact with Si.⁵⁻⁷⁾ However, substantially large threshold voltage (V_{th}) shifts and unacceptably high interface trap densities (D_{it}) serve as a major barrier to the applications of Hf-based dielectrics to deep submicron complementary metal-oxide-semiconductor (CMOS) technology.^{8,9)} Recently, Choi *et al.* investigated the electrical and structural properties of high-k Er-silicate films formed by the interfacial reaction between Er and SiO₂

films, and showed that the increase of the rapid thermal annealing (RTA) temperature results in a reduction of the interface trap density, and an increase of the relative dielectric constant of the Er-silicate film, which is compatible with the standard CMOS flow.¹⁰⁾ However, detailed knowledge of Er-SiO₂ interfacial reaction is insufficient for further development of its physical properties. In this work, we fabricate high-k Er-silicate films using the interfacial reaction between Er and SiO₂ films, and demonstrate their electrical and structural properties. In particular, the *in-situ* investigations of the Er-SiO₂ interfacial reaction and Er-silicate growth kinetics were performed using high-voltage electron microscopy (HVEM).

2. Experimental Procedures

For the evaluation of the electrical properties of the high-k Er-silicate gate dielectric, we fabricated metal-oxide-semiconductors (MOS). A 6.1 nm-thick SiO₂ film was thermally grown on a p-type (100) Si substrate with a doping concentration of 5×10^{15} cm⁻³. The physical thickness of the SiO₂ film was determined by an ellipsometry measurement. For forming gate electrodes, 45 nm-thick Er films were deposited, on which 25 nm-thick tungsten (W) films were grown as capping layers. After patterning gate areas with dimensions of $300 \times 300 \mu\text{m}^2$ using lift-off lithography, the RTA process was carried out at a temperature of 200~350°C for 1 min in a vacuum ($\sim 7 \times 10^{-7}$ torr) in order to minimize the effect of contamination. The microstructures of the Er-silicate gate dielectric were characterized by a field emission transmission electron microscopy (FE-TEM) equipped with energy dispersive spectroscopy (EDS), which

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Fig. 1 C-V characteristics of MOS devices at 100 kHz before and after RTA process. The insets of Fig. 1 exhibit the TRIM simulation of Er depth profile for sputtered Er atoms with a bias voltage of 100 eV approaching SiO₂ surface.

was operated at 300 kV. The capacitance-voltage (C-V) was measured at 100 kHz by an HP4284A Precision LCR meter. Especially, the *in-situ* investigations of the Er-SiO₂ interfacial reaction and the Er-silicate growth kinetics were examined using HVEM operated at 1250 kV. While being observed in the HVEM, the TEM specimen prepared using standard Ar⁺ ion milling at 77°K was annealed using an *in-situ* heating specimen holder. The heating rate of the TEM specimen and the image acquisition rate of a charge coupled device (CCD) camera were 10°C/min and 10 frames/s, respectively.

3. Results and Discussion

Figure 1 shows the C-V characteristics of MOS devices before and after the RTA process. The measurements were performed at room temperature at a frequency of 100 kHz. A quantum-mechanical (QM) simulation was employed to determine the equivalent oxide thickness (EOT).¹¹⁾ For all devices, the frequency dispersion and hysteresis were negligible, implying an insignificant effect of the oxygen deficiency and series resistance on C-V characteristics. It should be noted that the EOT of the as-deposited MOS device was determined to be 4.7 nm. This value is a much lower value than initial physical thickness of the SiO₂ film (6.1 nm), implying that a high-*k* Er-silicate gate dielectric was formed by the interfacial reaction between the Er and SiO₂ films without an additional thermal treatment. Such a reaction could be attributed to the high kinetic energy of sputtered Er atoms approaching the SiO₂ surface. Furthermore, considering the bias voltage (100 eV) during the sputter-deposition of Er film on SiO₂ film, the transport of ions in matter (TRIM) simulation (inset of Fig. 1) revealed that Er atoms penetrated and were confined at a depth of 2.4 nm in the SiO₂ layer, indicating that bombardment of sputtered Er atoms on SiO₂

Fig. 2 EDS line profiles for Er, Si, and O atoms taken from the interface regions between Er and Si substrate of MOS devices after an RTA process at temperatures of 200 and 300°C for 1 min.

is sufficient to allow the atomic intermixing of Er and SiO₂. It is clear that the EOT values gradually decrease with increasing RTA temperature. For example, the EOT values were determined to be 4.4, 4.2, 3.9, and 3.4 nm for MOS devices annealed at 200, 250, 300, 350°C, respectively. This indicates the thickness evolution of the Er-silicate film during the RTA process, which will be shown later.

Figure 2 represents EDS line profiles for Er, Si, and O atoms taken from the interface regions between the Er and Si substrates of MOS devices after an RTA process at temperatures of 200 and 300°C for 1 min. The line profiles were extracted from a series of EDS spectra acquired with a nominal electron probe size of 0.5 nm diameter. Since EDS intensity strongly depends on the thickness of a TEM specimen, all profiles were normalized using relative inten-

Fig. 3 HREM images taken from (a) the as-deposited thermally grown SiO₂ film, W(45 nm)/Er(25 nm)/SiO₂(6.1 nm) gate stacks (b) before and after an RTA process at temperatures of (c) 200, (d) 250, (e) 300, and (f) 350°C for 1 min.

sity (I_{relative}) defined as $I_{\text{relative}} = I_{(\text{Si, Er, O})} / [I_{\text{Si}} + I_{\text{Er}} + I_{\text{O}}]$. The profiles clearly demonstrate the presence of an Er-Si-O intermixing layer beneath the Er film, which is comparable to the TRIM simulation result (inset of Fig. 1). This implies the high- k Er-silicate film is formed between the Er and Si-substrate. It should be noted that as the RTA temperature increases, the relative intensity of Er and Si atoms increases and decreases, respectively. Such an elemental distribution behavior depending on annealing temperature indicates that the RTA process leads to the phase transformation of the Er-silicate film from the Si-rich phase into the Er-rich phase. Similarly, the XPS results (not shown here) also show that as the RTA temperature increases, Er 4d 5/2 peaks are shifted toward the higher energy side, suggesting that the chemical bonding state of the Er-silicate film is changed from Si-rich to Er-rich.¹⁰⁾

High resolution electron microscopy (HREM) images for the as-deposited thermally grown SiO₂ film, and W(45 nm)/Er(25 nm)/SiO₂(6.1 nm) gate stacks before and after RTA process are shown in Fig. 3. The thickness of the as-deposited SiO₂ film was measured to be 6 nm, which is comparable to the physical thickness determined by ellipsometry measurement (6.1 nm). It should be noted that for the as-deposited W(45 nm)/Er(25 nm)/SiO₂(6.1 nm) gate stack, the Er-silicate layer was formed on the SiO₂ layer indicated by the arrow. This shows a good agreement with the C-V measurements (Fig. 1). A careful comparison of images shows that with increased RTA temperature, the thicknesses of Er-silicate and SiO₂ layers increase and decrease, respectively. The thicknesses of the Er-silicate and SiO₂ layers are summarized in Fig. 4. For example, the thicknesses of Er-silicate and SiO₂ layers were measured to be 4.0 and

Fig. 4 Summary of the thicknesses of Er-silicate and SiO₂ layers measured from the HREM images shown in Fig. 3.

2.6 nm for the as-deposited sample, and 4.7 and 1.8 nm for the 350°C annealed sample, respectively. Such an annealing temperature dependency of the thicknesses of Er-silicate and SiO₂ layers indicates that the continual Er diffusion from Er gate electrode through Er-silicate film causes a further reaction with the remaining SiO₂ film.

Figure 5 represents HVEM images obtained from the W(45 nm)/Er(25 nm)/SiO₂(6.1 nm) gate stacks annealed at temperatures in the range of 25~350°C by using an *in-situ* heating specimen holder. The feature of thickness change for Er-silicate and SiO₂ layers *in-situ* annealed gate stacks is similar to that of the *ex-situ* annealed ones. Namely, the increase in *in-situ* annealing temperature leads to an increase and decrease in the thicknesses of Er-silicate and SiO₂ layers,

respectively. However, when comparing to the HREM results (Fig. 3), after annealing at 350°C, the thickness of a remaining SiO₂ film is negligible, implying no further interfacial reaction between Er and SiO₂. Such a relatively lower *in-situ* annealing temperature could be attributed to the preferential and fast diffusion of Er along the cross-sectional surface of the TEM specimen.

The *in-situ* investigations of the growth kinetics of the Er-silicate film and Er-SiO₂ interfacial reaction in W(45 nm)/Er(25 nm)/SiO₂(6.1 nm) gate stacks were subjected to restriction due to the relatively low *in-situ* annealing temperature (350°C) at which no further interfacial reaction between Er and SiO₂ layers proceeds. Therefore, the 45 nm-thick Er and 25 nm-thick W films were sequentially sputter-deposited on the thermally grown 15 nm-thick SiO₂ layer, followed by *in-situ* annealing in the HVEM. It should be noted that it is important to be able to measure the thickness of Er-silicate films from HVEM image for the accurate investigation of growth kinetics of the Er-silicate film. However, due to the very short image acquisition rate of a CCD camera (10 frames/s), the interface between Er gate and Er-silicate film is relatively faint, which makes a difficulty in the determination of the thickness of Er-silicate films. Alternatively, we extracted the thicknesses of Er-silicate films using the change in the thicknesses of SiO₂ layers with brightest contrast in the images, which are clearly shown in between Er-silicate film and Si-substrate. Namely, the amount of the reduction in the thickness of SiO₂ layer is comparable to that of thickness increment of Er-silicate films. Figure 6 represents HVEM images taken from W(45 nm)/Er(25 nm)/SiO₂(15 nm) gate stacks after *in-situ* annealing at 200~350°C. Similar to the HREM (Fig. 3) and HVEM

Fig. 5 HVEM images obtained from the W(45 nm)/Er(25 nm)/SiO₂(6.1 nm) gate stacks annealed at temperatures of (a) 25, (b) 100, (c) 150, (d) 200, (e) 250, (f) 300, and (g) 350°C by using an *in-situ* heating specimen holder.

Fig. 6 HVEM images taken from W(45 nm)/Er(25 nm)/SiO₂(15 nm) gate stacks after *in-situ* annealing at temperatures of (a) 200, (b) 250, (c) 300, (d) 350°C using an *in-situ* heating specimen holder.

Fig. 7 HVEM images taken from W(45 nm)/Er(25 nm)/SiO₂(15 nm) gate stacks *in-situ* annealed at 350°C for (a) 120, (b) 180, (c) 240, (d) 300, and (e) 360 s.

Fig. 8 HVEM images taken from W(45 nm)/Er(25 nm)/SiO₂(15 nm) gate stacks *in-situ* annealed at 450°C for (a) 120, (b) 180, (c) 240, (d) 300, and (e) 360 s.

results (Fig. 5) obtained from W(45 nm)/Er(25 nm)/SiO₂(6.1 nm) gate stacks, an increase in the *in-situ* annealing temperature leads to a gradual increase and decrease of Er-silicate and SiO₂ films, respectively. Namely, the effect of the thickness of the deposited SiO₂ layer on the interfacial reaction between Er and SiO₂ films is believed to be negligible.

Figures 7 and 8 show the HVEM images taken from W(45 nm)/Er(25 nm)/SiO₂(15 nm) gate stacks *in-situ* annealed at 350 and 450°C for various annealing times, respectively. For both gate stacks, the images clearly exhibit that the *in-situ* annealing for longer times leads to an increase in the thickness of Er-silicate layer with a decrease in the thickness of SiO₂ layer regardless of *in-situ* annealing temperature. However, the higher the *in-situ* annealing temperature, the greater the thickness of the Er-silicate layer, which will be discussed later.

Based on the thickness of Er-silicate layer extracted from HVEM results (Figs. 7 and 8), we investigated the growth kinetics of the Er-silicate layer layers formed by the interfacial reaction between Er and SiO₂ layers. Figure 9 shows the plot of the squared thickness increment of the Er-silicate layer as a function of *in-situ* annealing time obtained at different *in-situ* annealing temperatures. The linear relationship between the squared thickness of Er-silicate layer and *in-situ* annealing time suggests that the Er-silicate growth is a diffusion-controlled process.^{12,13} The parabolic growth constants, calculated from the linear fittings of kinetic curves, were found to be 2.3×10^{-16} and 9.3×10^{-16} cm²/s for *in-situ* annealing temperatures at 350 and 450°C, respectively. Such an increased parabolic growth constant implies that the increase in the *in-situ* annealing temperature enhances the growth rate of the Er-silicate film. Especially, the fitted lines

Fig. 9 The plot of the squared thickness increment of Er-silicate layer as a function of *in-situ* annealing time obtained at different *in-situ* annealing temperatures.

do not pass a zero point. Such a deviation could be attributed in part to the measurement errors and to a certain amount of surface diffusion along the surface of a TEM specimen. However, it is clear that the parabolic growth constant of Er-silicate film formed using *in-situ* annealing temperature at 450°C is much higher than that of Er-silicate film formed using *in-situ* annealing temperature at 350°C, which is a typical behavior governed by a diffusion-controlled process. This implies that the *in-situ* investigation of present study is believed to be valid although it is somewhat qualitative. Additionally, growth kinetics of Er-silicate film formed using the *in-situ* annealing process seems to be different from that of Er-silicate film fabricated using RTA process. This could be attributed to the redistribution of dopants and defects during RTA process. However, since *in-situ* annealing processes used in this work were carried out at the relatively

low temperature ($<450^{\circ}\text{C}$), the annealing temperature dependency of dopants and defects in present samples is believed to be insignificant. Furthermore, as compared with Er-silicate films formed using RTA process (Fig. 3), the growth behavior of Er-silicate film observed by *in-situ* HVEM is almost identical although detailed are somewhat different. In other words, thicknesses of Er-silicate and SiO_2 films increase and decrease with increasing annealing temperature, respectively. This indicates that growth kinetics of Er-silicate film derived from *in-situ* HVEM results is comparable to that of Er-silicate film formed using *ex-situ* RTA process.

4. Conclusions

We evaluated the electrical performance of MOS devices with high-k Er-silicate gate dielectrics, and the Er- SiO_2 interfacial reaction and Er-silicate growth kinetics through *in-situ* HVEM observations. The high kinetic energy of sputtered Er atoms approaching the SiO_2 surface during the Er sputtering process leads to the formation of the Er-silicate film without requiring an additional thermal treatment. As the annealing temperature was increased, the Er-silicate film exhibited a thickness evolution with a chemical bonding change from an Si-rich to Er-rich phase. The preferential and fast diffusion of Er atoms along the cross-sectional surface of TEM could be the main cause of a relatively lower *in-situ* annealing temperature, compared to the *ex-situ* RTA process. The parabolic growth constant of the Er-silicate film after *in-situ* annealing at a temperature of 450°C was 4 times higher than that after *in-situ* annealing at a temperature of 350°C , implying that the growth rate of the Er-silicate film increases with increasing *in-situ* annealing temperature.

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