Electrical Properties and Interface States of Rare-Earth Metal Ytterbium Schottky Contacts to p-Type InP

V. Rajagopal Reddy¹,²,* L. Dasaradha Rao¹, V. Janardhanam³, Min-Sung Kang² and Chel-Jong Choi²,³,*

¹Department of Physics, Sri Venkateswara University, Tirupati-517 502, India
²School of Semiconductor and Chemical Engineering, Semiconductor Physics Research Center, (SPRC), Chonbuk National University, Jeonju 561-756, Republic of Korea
³Department of BIN Fusion Technology, Chonbuk National University, Jeonju 561-756, Republic of Korea

The electronic parameters and interface state properties of Yb/p-InP Schottky diode have been investigated by current–voltage (I–V), capacitance–voltage–frequency (C–V–f) and conductance–voltage–frequency (G–V–f) measurements at room temperature. The barrier height and ideality factor of the Yb/p-InP Schottky diode are found to be 0.68 eV (I–V)/0.79 eV (C–V) and 1.24, respectively. As well, the values of barrier heights, ideality factors and series resistance are estimated by Cheung and Norde methods are compared. Under forward bias conditions, ohmic and space charge limited conduction (SCLC) mechanisms are identified at low and higher voltages, respectively. The C–V characteristics of the Yb/p-InP Schottky diode are also measured at different frequencies at room temperature. Further, the C–f and G–f measurements of the Yb/p-InP Schottky diode are performed at various biases. The interface state density Nₛ and relaxation time τ of the diode are estimated from the C–f and G–f measurements. The Nₛ and the τ show a decrease with bias from the top of the valence band toward the midgap. The profile of series resistance dependent on frequency and voltage confirms the presence of interface states in Yb/p-InP Schottky structure.


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1. Introduction

Indium phosphide (InP) is an attractive semiconductor material for the fabrication of solar cells, laser diodes, photodetectors and high speed metal–insulator–semiconductor field effect transistors (MISFETS), microwave sources and amplifiers operating at high power and high frequencies with low noise.¹–³ The formation of high quality metal–semiconductor (MS) structure is very essential since the electrical characteristics of the Schottky barrier diode (SBD) strongly depend on the quality of MS interface.⁴–⁸ Hence, the fabrication of Schottky contacts to InP with high barrier height and low-reverse leakage current is still a scientific challenge.

Many research groups have made attempts to investigate the electrical properties of p-InP Schottky barrier diodes using different metallization schemes.⁹–¹⁵ For example, Singh et al.⁹ investigated the electrical properties of Yb/p-InP Schottky diode as a function of temperature, reported a high value of ideality factor (n) for MS diode than the MIS diode. Asubay et al.¹⁰ studied the electrical characteristics of the as-deposited Au/p-InP/Zn–Au Schottky diodes (SDs), reported that the barrier height varied from 0.58 to 0.72 eV and ideality factor n from 1.1 to 1.47 from the current–voltage (I–V) characteristics. Varenne et al.¹¹ investigated the electrical parameters of Pd and Au pseudo-Schottky contacts on p-InP as a function of metal species and thickness by I–V measurements, reported that the pseudo-Schottky junctions exhibited a significant barrier height enhancement. Janardhanam et al.¹² prepared Ti/p-InP Schottky diode, and reported that the barrier height of 0.73 and 0.77 eV at 300 K by I–V and C–V measurements. Asubay¹³ investigated the electrical characteristics of identically prepared Al/p-InP Schottky diodes using I–V and C–V measurements, and reported that the effective barrier heights were varied diode to diode ranging from 0.83 ± 0.01 to 0.87 ± 0.01 eV (I–V) and 0.86 ± 0.04 to 1.00 ± 0.04 eV (C–V). Ashok et al.¹⁴ studied the electrical characteristics of Er/p-InP Schottky diodes at high temperature range (300–400 K) by I–V and C–V techniques, they found that the barrier height, ideality factor and series resistance are strongly temperature dependent. Recently, Korucu et al.¹⁵ investigated the current conduction mechanism in the Au/p-InP Schottky barrier diode. Also, they reported that the particular contact fabrication process produces a relatively high value of barrier height (0.78 eV) at room temperature.

There are, however, only limited works on rare-earth metal/p-InP Schottky barrier diodes have been investigated.⁹,¹³,¹⁶ A good Schottky contact will induce a large barrier height and small leakage current that can lead to better device characteristics. The Schottky barrier diodes are significantly influenced by the quality of the interface between the deposited metal and the semiconductor surface to their performance and reliability. Therefore, in this work, an attempt is made to fabricate and characterize the ytterbium (Yb) Schottky contacts on p-type InP at room temperature. As far as we know, no one has investigated the electrical properties of Yb/p-InP Schottky barrier diode at room temperature. Ytterbium, rare-earth element is chosen as a Schottky contact to p-type InP because it has a low work function (2.63 eV) that can yield high Schottky barrier heights. In the present work, we report on the electrical properties of Yb/p-InP Schottky barrier diode at room...
temperature. The Schottky diode parameters such as barrier height ($\Phi_b$), ideality factor ($n$), and series resistance ($R_s$) are estimated using various analysis techniques (forward $I-V$, $C-V$, Cheung, and Norde methods) and discussed. Also, the possible forward current conduction mechanism of Yb/p-InP Schottky barrier diode is discussed.

2. Experimental Details

Zn-doped p-type InP wafers with a resistivity of 0.44–0.58 $\Omega$cm (given by the manufacturer) were used in this work. Before making contacts, the p-type InP wafer was dipped in $5H_2SO_4$ solution for 1 min to remove surface damage and undesirable impurities. Then, the sample was etched in HF : $H_2O (1 : 10)$ solution for 1 min to remove the native oxide from the surface of the wafer. The wafer was rinsed thoroughly in deionized (DI) water and then dried in N$_2$ flow. An ohmic contact on the backside of InP wafer was formed by deposition of high purity (99.99%) Pt with a thickness of about 40 nm. After the Pt deposition, the contact was annealed at 450°C for 1 min in N$_2$ ambient using a rapid thermal annealing (RTA) system. 40 nm thick rare-earth metal Yb was deposited on the polished side of InP wafer with a diameter of 500 µm through a stainless-steel mask of circular dots using an e-beam evaporation system. The Yb/p-InP Schottky diodes were prepared with different deposition rates (0.1, 0.2, 0.3 and 0.4 nm/s) and different deposition temperatures (room temperature, 50, 75 and 100°C) for 0.1 nm/s only. All evaporation processes were carried out under a vacuum pressure of $7 \times 10^{-6}$mbar. The $I-V$, capacitance–voltage–frequency (C–V–f) and conductance–voltage–frequency (G–V–f) measurements were measured using a precision semiconductor parameter analyzer (Agilent 4156C) and LCR meter (Agilent 4284A) at room temperature and in the dark, respectively.

3. Results and Discussion

The forward and reverse $I-V$ characteristics of Yb/p-InP Schottky barrier diode measured at room temperature for 0.1 nm/s is shown in Fig. 1. $I-V$ characteristics of Yb/p-InP Schottky diode prepared at different deposition rates are shown in the inset of Fig. 1. The measured leakage current of Yb/p-InP Schottky diode is $9.8 \times 10^{-5}$ A at $+1$ V for deposition rate 0.1 nm/s at room temperature. The observed leakage currents for deposition rates of 0.2, 0.3 and 0.4 nm/s are $6.19 \times 10^{-5}$ A, $4.33 \times 10^{-5}$ A and $1.26 \times 10^{-4}$ A at $+1$ V, respectively. The best electrical properties are obtained for the diode prepared at 0.1 nm/s at room temperature. Thus, the Yb/p-InP Schottky diode prepared with deposition rate of 0.1 nm/s at room temperature is mainly analyzed in this work. When a SBD is considered with series resistance, it is assumed that the forward current through the SBD is due to thermionic emission (TE) theory, is given by the relation($^{17}$)

$$I = I_0 \exp \left( \frac{q(V - IR_s)}{nRT} \right) \left[ 1 - \exp \left( -\frac{q(V - IR_s)}{kT} \right) \right]$$  \hspace{1cm} (1)

where $V$ is the applied voltage, the term $IR_s$ is the voltage drop across the $R_s$ of the diode, $n$ is an ideality factor, $T$ is the absolute temperature, $k$ is the Boltzmann constant and $q$ is the electronic charge and $I_0$ is the reverse saturation current and it can be expressed as

$$I_0 = A A^* T^2 \exp \left( -\frac{q\Phi_b}{kT} \right)$$  \hspace{1cm} (2)

where $\Phi_b$ is the zero-bias barrier height, $q$ is the electronic charge, $A^*$ is the effective Richardson constant and $A$ is the diode area. The value of $\Phi_b$ can be deduced directly from the $I-V$ curves if the effective Richardson constant, $A^*$ is known (the theoretical value of $A^*$ was 60 A cm$^{-2}$ K$^{-2}$ for p-InP($^9$)) and is used to deduce $\Phi_b$. The ideality factor $n$ is calculated from the slope of the forward bias $\ln I-V$ plot in the linear region and it can be described using eq. (1) as

$$n = \frac{q}{kT} \left( \frac{d(V - IR_s)}{d(\ln I)} \right)$$  \hspace{1cm} (3)

The barrier height ($\Phi_b$) and ideality factor ($n$) are determined from the current axis intercept and the slope of the linear region of the forward-bias $I-V$ plot using eqs. (2) and (3), respectively. The barrier height and ideality factor of Yb/p-InP Schottky barrier diode are calculated as 0.68 eV and 1.24 for deposition rate 0.1 nm/s at room temperature. The values of barrier heights and ideality factors for different deposition rates (0.2, 0.3 and 0.4 nm/s) and deposition temperatures (room temperature, 50, 75 and 100°C) are shown in Table 1. Our experimental data indicate that the diode has the ideality factor that is greater than unity. Higher values of ideality factor ($n$) may be due to the presence of a thin interfacial insulator layer and a wide distribution of low-barrier height patches or barrier inhomogeneous and to the bias voltage dependence of the barrier height($^{17}$). The other reason for higher values of ideality factor $n$ could be ascribed to secondary mechanisms which include interface dipoles due to interface doping or specific interface structure with fabrication-induced defects at the interface($^{19-21}$). Tung($^{21}$) reported that the higher value of ideality factor could be ascribed to the presence of a wide distribution of low-Schottky barrier height patches caused by lateral barrier inhomogeneities. Moreover,
Table 1 Electronic parameters estimated from $I$–$V$ characteristics on the Yb/p-InP Schottky diodes at different deposition rates and temperatures.

<table>
<thead>
<tr>
<th>Conditions</th>
<th>Barrier height, $\phi_b$ (eV)</th>
<th>Ideality factor, $n$</th>
</tr>
</thead>
<tbody>
<tr>
<td>(A) Deposition rates (at room temperature)</td>
<td></td>
<td></td>
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<tr>
<td>0.1 nm/s</td>
<td>0.68</td>
<td>1.24</td>
</tr>
<tr>
<td>0.2 nm/s</td>
<td>0.58</td>
<td>1.48</td>
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<tr>
<td>0.3 nm/s</td>
<td>0.63</td>
<td>1.25</td>
</tr>
<tr>
<td>0.4 nm/s</td>
<td>0.52</td>
<td>1.92</td>
</tr>
<tr>
<td>(B) Deposition temperatures (deposition rate at 0.1 nm/s)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Room temperature</td>
<td>0.68</td>
<td>1.24</td>
</tr>
<tr>
<td>50°C</td>
<td>0.65</td>
<td>1.32</td>
</tr>
<tr>
<td>75°C</td>
<td>0.66</td>
<td>1.28</td>
</tr>
<tr>
<td>100°C</td>
<td>0.67</td>
<td>1.27</td>
</tr>
</tbody>
</table>

The forward bias $I$–$V$ characteristics of Yb/p-InP Schottky diode (see Fig. 1) are linear at low forward bias voltage, but deviate considerably from linearity at high voltage due to the effect of series resistance and interface state density. As the linear range of the forward $I$–$V$ plot is reduced, the accuracy of the determination of $\phi_b$ and $n$ becomes poorer. Thus, from the non-linear region of the forward bias $I$–$V$ data, the $\phi_b$, $n$ and $R_s$ can be obtained using a method developed by Cheung and Cheung. Cheung’s functions can be expressed as follows:

$$\frac{dV}{d(\ln I)} = IR_s + n\left(\frac{kT}{q}\right)$$

and

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^nT^2}\right)$$

A plot of $dV/d(\ln I)$ versus $I$ will be linear yielding $R_s$ as the slope and $n(kT/q)$ as the y-intercept from which the ideality factor $n$ will be extracted from eq. (4). Figure 2 shows the experimental plots of $dV/d(\ln I)$ versus $I$ and $H(I)$ versus $I$ for the Yb/p-InP Schottky diode. The values of $n$ and $R_s$ of the Yb/p-InP Schottky diode are obtained to be 1.32 and 63 $\Omega$, respectively. A plot of $H(I)$ versus $I$ will also give a straight line with the slope yielding $R_s$ and y-intercept equal to $n\phi_b$ using the $n$ value estimated by the $dV/d(\ln I)$ versus $I$ plot. The determined $R_s$ and $\phi_b$ from the plot of $H(I)$ versus $I$ are found to be 80 $\Omega$ and 0.71 eV, respectively. Experimental results reveal that both the series resistances obtained from $dV/d(\ln I)$ versus $I$ and $H(I)$ versus $I$ are in good agreement with each other, implying their consistency and validity. The calculated ideality factor values from the non linear region of forward bias $I$–$V$ plot and from the linear region of the same characteristics are different from each other. The reason for this difference can be attributed to the existence of effects such as the bias dependence of Schottky barrier height, according to the voltage drop across the interfacial layer and the change of the interface states with the bias in the low-voltage region of the $I$–$V$ plot and the series resistance.

To determine the Schottky barrier height and series resistance of Yb/p-InP Schottky barrier diode, the modified Norde function was also employed. The modified Norde’s function is defined as

$$F(V) = \frac{V}{\gamma} - \frac{1}{\beta} \ln \left[ \frac{I(V)}{AA^nT^2} \right]$$

where $\gamma$ is an integer (dimensionless) greater than the ideality factor, $F(V)$ is the current obtained from the $I$–$V$ curve, and $\beta$ is a temperature dependent value calculated using $\beta = q/kT$. The effective Schottky barrier height given by

$$\phi_b = F(V_o) + \frac{V_o}{\gamma} - \frac{kT}{q}$$

where $F(V_o)$ is the minimum point of $F(V)$ and $V_o$ is the corresponding voltage. Figure 3 shows a plot of the Norde function $F(V)$ versus $V$ for the Yb/p-InP Schottky barrier diode. The value of series resistance ($R_s$) can be estimated from the Norde function using

$$R_s = \frac{kT(\gamma - n)}{qI_{\text{min}}}$$
where \( I_{\text{min}} \) is the current in the device corresponding to voltage \( V_0 \) (at which \( F(V) \) becomes minimum). The \( \phi_b \) and the \( R_s \) values are determined from the modified Norde plot as 0.72 eV and 258 \( \Omega \), respectively. The values of \( \phi_b \) calculated from the Norde function is in good agreement with the value obtained from \( I-V \) characteristics and Cheung’s functions. Besides, the series resistance estimated from the Norde function is comparable with those estimated from the plots of \( dV/d(\ln I) \) versus \( I \) and \( H(I) \) versus \( I \).

In order to understand the current conduction mechanism dominating in the forward bias region of the Yb/p-InP Schottky barrier diode, a forward bias log \( I \) versus log \( V \) plot is presented in Fig. 4. Our Yb/p-InP Schottky barrier diode reveals three distinct regions under forward bias which are called as region I, II and III as shown in Fig. 4. These three linear regions have different slopes that obey \( I \propto V^m \) change, here \( m \) is the slope of the plot for each linear region and the values are found as 1.50, 5.48 and 2.71, respectively. At low bias region I, the current conduction mechanism exhibits an ohmic behavior, which is due to existing background doping or thermally generated carriers.\(^{24} \) In the region II, the Yb/p-InP Schottky diode can be characterized by power law dependence, indicating the charge transport is governed by space charge limited current (SCLC) with a discrete trapping level. In the region III, the value of slope is about 2.71 for the Yb/p-InP Schottky diode. The slope of the plot at high voltages tends to decrease since the device approaches the “trap-filling” limit when the injection level is high whose dependence is the same as in the trap-free SCLC.\(^{25,26} \)

The forward and reverse bias \( C-V \) characteristics of the Yb/p-InP Schottky barrier diode measured at room temperature under various frequencies as a function of applied bias voltage are shown in Fig. 5. As can be seen in Fig. 5, the capacitance value of Schottky junction is increasing in forward bias till a point where it reaches a maximum value. At low frequencies, the higher values of capacitance are ascribed to the excess capacitance resulting from the interface state density which is in equilibrium with the semiconductor that can follow the alternating current signal. Whereas, the capacitance is not dispersive at higher frequencies, as a result the interface states in equilibrium with the semiconductor do not contribute to the capacitance, as the charges at the interface states cannot follow the alternating current signal. However, at low frequencies the total capacitance is equal to the sum of space-charge capacitance and interface capacitance, whereas the total capacitance arises mostly from the space-charge capacitance at higher frequencies.\(^{27} \)

Under forward bias, measurement of the depletion region capacitance is difficult as the diode is conducting and the capacitance is shunted by a large conductance. But, the capacitance can be easily measured as a function of the reverse bias. Figure 6 shows a plot of \( 1/C^2 \) as a function of bias voltage for the Yb/p-InP Schottky diode measured at 1 MHz. In Schottky structures, the depletion layer capacitance can be written as\(^{17} \)

\[
\frac{1}{C^2} = \frac{2(V_{do} + V)}{q\varepsilon_s A^2 N_A}
\]

(10)

where \( \varepsilon_s \) is the semiconductor permittivity of p-InP (\( \varepsilon_s = 12.5\varepsilon_0 \), where \( \varepsilon_0 \) permittivity of the free space), \( V_{do} \) is
the diffusion potential at zero-bias and is determined from the extrapolation of the linear $C^{-2} - V$ plot to the $V$-axis. The value of the barrier height can be calculated by the equation $\phi_b(C - V) = V_{ds} + V_p$, here $V_p$ is the potential difference between the Fermi level and the top of the valance band of p-InP which can be calculated by knowing the carrier concentration $N_A$ and it is obtained from the equation $V_p = (kT/q)\ln(N_v/N_A)$, where $N_v = 1.1 \times 10^{19}$ cm$^{-3}$ is the density of effective states in the valence band of p-InP. The estimated diffusion potential and barrier height of Yb/p-InP Schottky diode are 0.73 V and 0.79 eV, respectively. Our results showed that the barrier heights estimated from $I$-$V$ measurements are considerably lower than those estimated from $C$-$V$ measurements. The reason for the discrepancy is that the current in the $I$-$V$ measurement is dominated by the current which flows through the region of low Schottky barrier height (SBH). The determined $I$-$V$ barrier height is significantly lower than the weighted arithmetic average of the SBHs. On the other hand, the $C$-$V$ measured barrier height is influenced by the distribution of charge at the depletion region boundary and this charge distribution follows the weighted arithmetic average of the SBH inhomogeneity. Consequently, the barrier height estimated by $C$-$V$ is close to the weighted arithmetic average of the SBHs. Also, this discrepancy could be the existence of excess capacitance at the structure due to the interfacial layer (or) trap states in the semiconductor and the existence of the barrier inhomogeneity is the another explanation.

Further, the density distribution of the interface states are calculated from the capacitance-frequency ($C$-$f$) measurements of the Schottky diodes using the Schottky capacitance spectroscopy (SCS) method. The SCS measurement is a measurement technique which can provide the required accuracy in determining the variation of interface state capacitance as a function of the forward bias at low frequency. The experimental capacitance obtained from the $C$-$f$ measurements approximately equals to the sum of space-charge capacitance ($C_{sc}$) and the interface capacitance ($C_{ss}$). Accordingly, the capacitance of the devices depends on frequency and it can be described as

$$C = C_{sc} + C_{ss} \quad \text{(at low frequency)}$$

$$C \approx C_{sc} \quad \text{(at high frequency)}$$

Based on the Nicolian and Goetzberger, the interface state capacitance is defined as

$$C_{ss} = AqN_{ss} \frac{\arctan(\omega \tau)}{\omega \tau}$$

where $\tau$ is time constant and it can be written as

$$\tau = \frac{1}{V_{th} \sigma N_A} \exp \left( \frac{qV_{th}}{kT} \right)$$

where $\sigma$ is the cross-section of interface states, $V_{th}$ is the thermal velocity of carrier and $N_A$ is the carrier concentration. The interface state density for small values of $\omega \tau$ equal to $30-33$

$$N_{ss} = \frac{C_{ss}}{q A}$$

where $A$ is the diode area. The interface-state capacitance $C_{ss}$ is obtained from the vertical axis intercept of $C_{ss}$-$f$ plots.

For p-type semiconductor, the energy of the interface states $E_{ss}$ with respect to the top of the valance band at the surface of the semiconductor is given by

$$E_{ss} = E_V = (\Phi_e - V)$$

where $E_{ss}$ is the energy of the interface states and $E_V$ the valence band edge.

Figure 7(a) shows the $C$-$f$ characteristics of the Yb/p-InP Schottky barrier diode at various bias voltages.

![Fig. 7](image-url)
teristics at various bias voltages (0.0–0.5 V) measured at room temperature. It can be seen from figure, the con-
ductance increases with increasing frequency which is due to
the fact that the jumping of interface charges increases with
frequency of applied voltage.

At a given forward bias, the experimental space-charge
capacitance values in high frequency region obtained forward
bias $C$–$f$ plots are subtracted from the experimental junction
capacitance $C_{ss}$ accordingly the interface state capacitance
$C_{ss}$ is estimated ($C_{ss}$–$f$ plots are not shown here). The
equation (15) is applicable in the plateau region of the $C_{ss}$–$f$
plot and the value of the interface state density $N_{ss}$ for each
applied bias voltage can be obtained directly from the
ordinate of the plateau. Afterward, eq. (13) is
fit to the experimental values of $C_{ss}$–$f$ to estimate relaxation time
of the interface state density $\tau$. To determine the bias
dependence of $N_{ss}$ and $\tau$, the fitting procedure is repeated
for various values of the bias voltage.33) Using eq. (16), the
dependence of $N_{ss}$ and $\tau$ on the bias is converted to a function
of $E_{ss}$. Figure 8 shows the experimental $N_{ss}$ versus $E_{ss}$–$E_v$ and
$\tau$ versus $E_{ss}$–$E_v$ plot obtained from $C$–$f$ characteristics at room
temperature, respectively. It can be seen from Fig. 8, the
interface state densities ranges from $1.82 \times 10^{13}$ cm$^{-2}$ eV$^{-1}$
($E_v - 0.68$) eV to $3.11 \times 10^{13}$ cm$^{-2}$ eV$^{-1}$ in ($E_v - 0.18$) eV.
Besides, the values of the relaxation times range from 1.05 s
in 0.18 eV to $4.86 \times 10^{-8}$ s in 0.68 eV. It is seen that the
interface state densities and the relaxation times show a
decrease with bias from the top of the valence band toward
the midgap.

Moreover, the voltage dependent series resistances and
frequency of the Yb/p-InP Schottky barrier diode can be
estimated from the $C$–$V$–$f$ measurements. According to
Nicollian and Brews,36) the series resistance $R_s$ can be
described as
\[
R_s = \frac{G}{G^2 + (\omega C)^2}
\]
where $C$ is the measured capacitance and $G$ is the measured
cconductance values. The series resistance of Yb/p-InP
Schottky barrier diode as a function of the voltage is
calculated by using eq. (17). The voltage dependency of the
series resistance for different frequencies is shown in Fig. 9.
It can be seen from Fig. 9, the peak intensity decreases with
increasing frequency. This indicates that the interface states
follow the alternative current. However, at high frequency
the peak disappears and this suggests that the interface states
cannot follow alternative current. In addition, the series
resistance of the Yb/p-InP Schottky barrier diode as a
function of the frequency is estimated using eq. (17) and it is
shown in inset of Fig. 9. It can be seen clearly from the figure
that the resistance rapidly decreases with increasing fre-
quency at low frequencies and then remains almost constant.
The frequency and voltage dependency of the series
resistance is ascribed to the particular distribution density
of interface states.

Fig. 8 The distribution plots of the interface state density and their
relaxation time constant versus $E_{ss}$–$E_v$ from the $C$–$f$ characteristics.

Fig. 9 Plot of $R_s$–$V$ of the Yb/p-InP Schottky barrier diode as function of frequencies (inset: plot of $R_s$–$f$ at various bias voltages).
4. Conclusions

In summary, the electrical parameters and interface state properties of the fabricated Yb/p-InP/Pt Schottky barrier diode have been studied by $I-V$, $C-V$–$f$ and $G-V$–$f$ measurements at room temperature. The determined barrier height and ideality factor of the Yb/p-InP Schottky diode is 0.68 eV ($I-V$)/0.79 eV ($C-V$) and 1.24, respectively. Also, barrier height calculated by Norde method is in good agreement with those obtained by the $I-V$ method. The series resistance $R_s$ of the Yb/p-InP Schottky diode is determined using Cheung functions and the values are in good agreement with each other. Further, the $I-V$ characteristic under forward bias is found to be ohmic conduction at low voltage regions. At higher voltage regions there is space charge limited conduction (SCLC) mechanism. $C-V$ characteristics of the Yb/p-InP Schottky diode are also measured at different frequencies at room temperature in the dark. The higher values of capacitance at low frequencies are due to excess capacitance resulting from the interface states that can follow the alternative current signal. Moreover, the energy distribution of the interface states and their relaxation time constants are determined from the $C-f$ and $G-f$ characteristics of the Yb/p-InP Schottky barrier diode at room temperature. The interface state density $N_a$ and the relaxation time $\tau$ show a decrease with bias from the top of the valence band toward the midgap. The frequency and voltage dependency of the series resistance is attributed to the particular distribution density of interface states. Experimental results confirmed that the $N_a$ and $R_s$ are important parameters that influence electrical properties of Schottky barrier diode.

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REFERENCES