Computer Simulation of Stress Induced Dislocation Multiplication in Large-Diameter Silicon Wafer in High-Temperature Device Processing

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The occurrence of slip bands due to stresses in large-diameter Czochralski-grown silicon (Si) wafers was studied with computer simulation to maintain them dislocation-free in ultra-large-scale-integrated-circuits (ULSIs) manufacturing. Two types of stresses induced in the circular wafers are investigated; thermal stress originated either in radial temperature variation or in gravitational stress due to the bending moment caused by the wafer's weight itself. Since the advent of 200-mm-dia wafer era for devices, slip bands generated by the gravitational stress were discovered, extending from the point jig as elongated slippages along the $\langle 110 \rangle$ directions, in addition to those due to thermal stresses. On a simplified model wherein the point jig was assumed to be a solid line, resolved shear stresses due to the gravitational stress were calculated for the 300-mm-dia wafer, which is considered to be the wafer size of the next generation. On the basis of the previously proposed thermoelastic model, critical stress curves to multiply slip dislocations were obtained as a function of microdefect density, which acts as nucleation sites for dislocation multiplication, thereby softening Si wafers under mechanical stress. By comparing both the gravitational stress and the critical stresses, conditions to suppress slip bands due to the gravitational stress in device processings are described as predictable in wafers larger than 300 mm in diameter and moreover those to suppress slip dislocations due to thermal stress were also predicted. The physical meaning of the critical stress curve is discussed by comparing with the upper yield stress obtained in conventional tensile tests.

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I. Introduction

When dislocation-free silicon (Si) crystals are stressed at a high temperature, dislocations multiply at surface irregularities such as mechanical scratches⁽¹⁾ or oxide precipitates accompanying punched-out dislocation loops in the bulk Si grown during heat treatments⁽²⁾⁽³⁾, resulting in slip bands. In plastic deformation of semiconductors, mechanical yield stresses, (i.e. upper and lower yield stresses), defined by characteristic stress-strain curves are known to depend on deformation temperature and strain rate⁽⁴⁾. The results obtained in Si⁽⁵⁾⁻⁽⁷⁾ have already been applied for estimating onset of slip dislocations due to thermal stresses⁽⁸⁾⁻⁽¹¹⁾ caused by the radial temperature variation in circular Si wafers in integrated-circuit (IC) fabrication processes, where a row of equally spaced Si wafers is heat-treated at an optimized rate in a high-temperature furnace⁽⁹⁾⁽¹²⁾⁻⁽¹⁸⁾.

In a currently used vertical-type furnace, wafers are set horizontally on a supporting jig, often of the point contact type. As a result, the wafers bow elastically at the fulcrum of the jig, owing to the gravitational stress originat-

ing in bending moment due to their weight. Under wafer diameter versus thickness trend designed for IC, this gravitational stress increases with wafer size, although the gravitational stress is independent of temperature. The gravitational stress causes slip bands if it surmounts the critical stress of dislocation multiplication in Si. When 200-mm-dia wafers are held in the vertical-type furnace at around 1473 K for several hours, slip bands along $\langle 110 \rangle$ directions several centimeters from the supported edge were observed as a new phenomenon⁽¹⁹⁾. We have confirmed that this slip propagation is not caused by thermal stresses, but by gravitational stresses, because the processed wafers were heated up and cooled down slow enough to avoid slip dislocations due to thermal stresses caused by transient radial temperature gradient. Therefore, enlarging the wafer to 300 mm, which is supposed to be the diameter of the next generation, will seriously aggravate the problem of slip bands due to gravitational stresses. To avoid such slippage, several sorts of supporting jigs are being devised. One of them is ring-shaped, allowing it to escape from stress concentration at the supporting point. Xin⁽²⁰⁾ estimated the radius of this jig's ring, to minimize stress components, to be at the ratio of

b/R (b =ring radius, R =wafer radius) ≈ 0.7 . In that case, he demonstrated that the resolved shear stress in a 300-mm-dia wafer can be reduced to 0.11 MPa. However, the calculated stresses were not compared with the mechanical strength of the processed wafers at high temperatures. Thus, in anyway, computer simulation of the initiation of slip bands due to gravitational stresses will be essential in designing wafer thickness for wafers in the next generation.

The mechanical yield strength as measured by ordinary tensile or compressive tests is drastically reduced if Czochralski-grown (CZ) dislocation-free Si crystals are subject to heat treatments prior to the tests⁽²⁾⁽³⁾. During the heat treatments, oxygen-precipitates grow and misfit strain between SiO_2 and Si matrix causes small punched-out dislocation loops which become dislocation multiplication sources under stresses. This is, what is called, precipitation softening phenomenon⁽⁹⁾. In this investigation, microdefect includes oxide-precipitates accompanying dislocation loops and stacking faults, thus, the term of "microdefect" is referred to as the indicator of softening of Si bulk crystal. As confirmed in CMOS-LSI processing, the resultant wafer warpage due to thermal stresses depends on the microdefect density, in which the threshold density to suppress wafer warpage was around $2\text{--}5 \times 10^{15}/\text{m}^3$ ⁽²¹⁾⁽²²⁾. Repetitive heat-treatments in ultra-large-scale-integration (ULSI) processes facilitate oxygen precipitation^{(23)–(25)}, as a result, prompting precipitation softening. The wafer enlargement and device miniaturization become increasingly significant in meeting the market demands for Si devices which keep higher performance at lower cost. Wafer enlargement necessitates much slower heating and cooling rates for batch-type processings to reduce thermal stresses, and the device miniaturization requires a low-temperature process because of thinner gate-oxide and shallower p-n junction. Such trends accelerate oxygen precipitation, which diminishes the mechanical strength, as long as the annealing duration is not shortened by employing new technologies such as single-wafer treatment. Thus, for running wafers in a device process, it is important to obtain the critical stress curves experimentally as a border of the initiation of slip bands against a function of microdefect density. These curves enable computer simulation of the slip bands prediction for an imaginary wafer size in plausible device modes as a function of microdefect density. Therefore, for the future wafer size, it is worthwhile to estimate gravitational stress and predict the initiation of slip bands for the wafers having a certain range of microdefect density in addition to dislocations due to thermal stresses.

This paper describes the critical conditions of slip bands occurrence in large-diameter Si wafers during high temperature processings. For the first step, gravitational stresses are estimated under a simplified model and converted to resolved shear stresses in $\{001\}$ slip planes and $\langle 110 \rangle$ slip directions. In parallel with the calculation, individual critical stress curves are independently obtained as functions of deformation temperature and

microdefect density on the basis of Matsuba's model⁽¹⁷⁾. The critical stress curves are compared with the resolved shear stresses of the gravitational stress in 300-mm-dia wafers, aiming at predicting the onset of slip bands.

II. Experimental Procedure

1. Samples used for determining the critical stress curve

Dislocation-free $\langle 100 \rangle$ oriented Si single crystals 100, 150 and 200 mm in diameter were grown by the CZ pulling method with a boron concentration of approximately 1.6×10^{21} atoms/ m^3 . The sliced wafers were lapped and mechanochemically polished to produce mirror surfaces on one side. The polished surface of the sliced wafers was tilted from the (001) plane at an angle of $4 \pm 1^\circ$ in the direction of the [010] pole. The concentration of interstitial oxygen ([Oi]) of the wafers used in the present work was $9\text{--}10 \times 10^{23}$ atoms/ m^3 (FT-IR; Digilab QS 300)⁽²⁶⁾ on the basis of the conversion coefficient obtained by JEIDA (Japan Electronic Industry Development Association). The substitutional carbon concentration was below the detection limit (2×10^{22} atoms/ m^3).

2. Heat treatments in vertical-type furnace

A highly integrated device processing adopts in oxidation and diffusion processes a vertical-type furnace in which the furnace inside had been designed to use a boat with less heat capacity and to reduce air involvement during wafer insertion and withdrawal. Figure 1(a) illustrates a currently used type of jig that supports wafers in a vertical furnace. The heat cycle to stress wafers thermally is shown in Fig. 1(b). Prior to the test cycle, sample wafers were heat-treated in two steps; at 1073 K for 2 h followed by at 1273 K for 16 h in dry oxygen ambient. Precipitated amount of oxygen is defined as the difference before and after the heat treatments.

3. X-ray topography to observe dislocations

X-ray topography was employed to verify the overall distribution of slip bands and/or dislocations in heat-treated wafers. For the measurement, $\{220\}$ reflection with Mo $K\alpha$ radiation was used. Microdefects were observed on cleaved surfaces of heat-treated wafers by interference optical microscope. Figure 2 shows X-ray topograph of slip dislocations due to thermal stress when wafers in a row were inserted into high-temperature furnace in which the thermal stress was high enough to exceed the critical stress of dislocation multiplication. Dislocations emerged at areas where resolved shear stresses were the highest⁽¹¹⁾. Gravitational stresses were also expected to become serious by holding large-diameter wafers at high temperatures. In the present investigation, the initiation of slip dislocations is examined from the viewpoint of both gravitational stress and thermal stress.

4. Calculation of gravitational stresses

In vertical furnaces, wafers are held at four points in a

Fig. 1 Schematic diagrams of a wafer jig in a vertical-type furnace and a sequence of heat treatment in standard device processing. Steps (1) and (7) are insertion and withdrawal of wafers in moderate rates, (2) and (6) are idling processes at a temperature of around 1073 K, (3) and (5) are slow heating and cooling to (4). The process temperature in this experiment was at 1473 K.

Fig. 2 X-ray topograph of slip dislocations caused by thermal stresses in Si wafer.

quartz jig, as shown in Fig. 3(a). To simplify the calculation of resolved shear stresses appearing in wafers, two points across a wafer are regarded as a solid line. Since the wafer is symmetrical across the dotted line, the half of the wafer is depicted in Fig. 3(b) and it is assumed to be fixed at both A and B. The following calculation is done on the isotropic elastic body. The load profile diagram for the half of the wafer is given in Fig. 3(c), where A and B show supporting points. In that case, the bouncing forces W_A and W_B are defined and W_A should be larger than W_B . On evaluating gravitational stresses⁽²⁷⁾, the square of the divided element (weight is assumed to be

Fig. 3 A simplified model to describe the direction of bending moment, (a) schematic diagram for four point jig made of quartz, (b) assumption to support a wafer by solid line instead of four point jig, (c) load profile diagram, (d) determination of self-gravity in the element shown in (c).

$W(x)$) was obtained by integration. At the same time, the gravity center of the element was determined by drawing and $l(x)$ is defined as the distance between the gravity center and the edge of each element, as shown in Fig. 3(d). W_A and W_B were determined by calculating the gravity center in the wafer half; then a and b were obtained proportionally under the condition of total weight; $W_A + W_B = W$, and the balancing moment centering at $x=0$; $W \cdot R = W_A \cdot a + W_B \cdot (a+b)$. As a result, moment M can be calculated in the following. The resultant bending moment in each area is as follows:

$$0 < x \leq a$$

$$M = W(x) \cdot l(x)$$

$$a \leq x \leq b$$

$$M = W(x) \cdot l(x) - W_A \cdot (x-a)$$

$$b \leq x \leq 2R$$

$$M = W(x) \cdot l(x) - W_A \cdot (x-a) - W_B \cdot (x-b).$$

Gravitational stresses for the bending moment were calculated by M/Z (Z : section coefficient). They were converted to resolved shear stresses by multiplying maximum Schmidt factor ($1/\sqrt{6}$) on the $\{111\}$ plane and in the $\langle 110 \rangle$ directions. The section coefficient (Z) is given by $y_n t^{2/6}$, where y_n is n -th small element along y direction and

(1)

t is the thickness of the wafer. Thus, the gravitational stress is proportional to the inverse of t^2 ⁽²⁸⁾.

5. Extension of the thermoelastic model to the vertical type of furnace

In the present investigation, the prediction of dislocation onset during heat treatments in vertical furnaces was carried out using the thermoelastic wafer model which was first developed by Matsuba *et al.* ⁽¹⁵⁾⁽¹⁷⁾ for the horizontal furnace on the basis of Hu's mathematical model ⁽⁹⁾. By analogy with the heat transfer in a horizontal furnace ⁽¹⁵⁾⁽¹⁷⁾, the transient wafer temperature T_w is given for a vertical furnace by the following partial differential equation:

$$\partial T_w / \partial t = -\phi_1 + \phi_2 + \phi_3 + \phi_4. \quad (2)$$

Here, $\partial T_w / \partial t$ indicates a time derivative. Heat flows between the wafers and the furnace are schematically shown in Fig. 4. ϕ_1 is the surface radiation loss from the wafer on both sides, ϕ_2 is the radiant heat from both neighboring wafers, ϕ_3 is the radiant heat from the furnace wall to the wafer, ϕ_4 is the heat diffusion over the wafer surface. As wafers are assumed to be supported at point in a quartz jig in the vertical furnace, the heat capacity of the jig can be ignored in calculating the temperature variation. The thickness of the wafer is also assumed to be sufficiently small, compared with wafer diameter, that the temperature can be regarded as uniform across the thickness. In calculation, the target wafer was assumed to be set between five dummy wafers. Equation (2) gives the temperature variation in wafers with time as follows ⁽¹⁵⁾⁽¹⁷⁾:

$$\begin{aligned} \ell c \rho \frac{\partial \tilde{T}_{wi}(\tilde{r}, \tilde{t})}{\partial \tilde{t}} = & -2\epsilon \sigma \tilde{T}_{wi}^4(\tilde{r}, \tilde{t}) \\ & + \sum_{j=i \pm 1, 0} \int_{s_w} \epsilon \sigma a \tilde{T}_{wj}^4(\tilde{r}, \tilde{t}) \sum_{n=0}^{\infty} G_{nj}(\tilde{r}, \tilde{r}') dS_w \\ & + \int_{s_f} \epsilon_f \sigma a \tilde{T}_f^4(\tilde{r}') \sum_{n=0}^{\infty} F_n(\tilde{r}, \tilde{r}') dS_f \\ & + \ell \nabla \{K(\tilde{T}_{wi}) \nabla \tilde{T}_{wi}(\tilde{r}, \tilde{t})\} \end{aligned} \quad (3)$$

Fig. 4 Heat transfer between a row of wafers and the heater, schematically shown in a vertical-type furnace.

$\tilde{T}_{wi}(\tilde{r}, \tilde{t})$ is i -th wafer temperature in a row, ℓ is the wafer thickness, c is the wafer heat capacity, ρ is the wafer density, ϵ and ϵ_f are the radiation coefficient of wafer and furnace tube, a is the absorption coefficient from wafer radiation, $K(\tilde{T}_{wi})$ is the thermal conductivity dependent on temperature, σ is the Stefan Boltzman constant. dS_w and dS_f are the elements of wafer and furnace tube surfaces, ∇ is the differential operator.

Numerical calculation of thermal stresses is based on the following equation in cylindrical coordinates ⁽²⁹⁾:

$$\begin{aligned} \sigma_{rr}(r) = & \alpha E \left[1/R^2 \int_0^R T(r) r dr - 1/r^2 \int_0^r T(r) r dr \right], \\ \sigma_{\theta\theta}(r) = & \alpha E \left[1/R^2 \int_0^R T(r) r dr - 1/r^2 \right. \\ & \left. \times \int_0^r T(r) r dr - T(r) \right], \\ \sigma_{r\theta}(r) = & 0 \end{aligned} \quad (4)$$

and where α is the thermal expansion coefficient ($4 \times 10^{-6} / ^\circ\text{C}$); E , Young's modulus ($1.5 \times 10^{11} \text{ N/m}^2$); R , the radius of the wafer; r , the radial distance from the wafer center; and $T(r)$, the radial temperature profile of the wafer solved by eq. (3). Here, thermal stresses were practically calculated using the finite-element method (FEM) under plane stress conditions ⁽¹⁷⁾. Figure 5 shows the triangle elements used to calculate thermal stresses from the temperature distribution in wafers. In the vertical furnace, the radial temperature variation in the wafer can be assumed to be axially symmetrical with respect to the wafer center. This assumption differs from the case of the horizontal furnace ⁽¹⁷⁾. Thus, only a quarter of a wafer is taken into account.

The calculated thermal stresses were converted to resolved shear stresses on slip planes $\{111\}$ in slip directions $\langle 110 \rangle$, which are well defined crystallographic directions in the diamond lattice ⁽¹⁷⁾. The critical stress for slip bands was experimentally deduced on the basis of the mechanical yield stress obtained by either tensile or compressive tests ⁽⁴⁾⁽⁶⁾⁽⁷⁾, as previously reported ⁽¹³⁾⁽¹⁴⁾.

Fig. 5 Divided element for finite element method required to calculate thermal stresses.

III. Simulation Results and Discussions

1. Slip propagation in 200-mm-dia wafers due to gravitational stresses

Figure 6(a) shows an X-ray topograph of the 200-mm-dia wafer that was kept at a temperature of 1473 K for several hours in the quartz jig following the sequence shown in Fig. 1(b). This picture was taken using the (220) reflection and demonstrates slip bands propagating along $\langle 110 \rangle$ directions. This result implies that slip bands are nucleated at the four-point quartz jig, as schematically shown in Fig. 6(b). The induced dislocations were characterized chiefly to be an edge-type dislocation; detailed analysis is under investigation⁽³⁰⁾. If wafers were inserted into and withdrawn from the furnace at around 1123 K and then heated up at the speed of 7°C/min to a temperature of 1273 K and cooled down at 3°C/min to 1123 K, no slip bands were observed by X-ray topography. In this case, thermal stresses during the heating and cooling proc-

esses were considered to be negligibly small not enough to activate slip dislocations. Thus, this slip band propagation was confirmed to be induced by gravitational stress while wafers were held at around 1473 K (including the time during heating up and cooling down).

2. Gravitational stress in 300-mm-dia wafer

Figure 7 shows the calculated gravitational stress which is plotted against their distance from the rim of the 300-mm-dia wafer. In a numerical calculation, the wafer thickness was assumed to be 775 μm . This thickness is proposed as a candidate specification for 300-mm-dia wafers, following the extrapolation trend based on data for smaller wafers. The gravitational stress was maximum ($4.4 \times 10^5 \text{ N/m}^2 = 0.44 \text{ MPa}$) at the supported edge around the center, while the σ_M in the 200-mm-dia wafer was calculated to be $2.1 \times 10^5 \text{ N/m}^2$ (0.21 MPa).

Figure 8 shows the maximum resolved shear stress (σ_M) plotted against wafer thickness (t); as expected, σ_M decreases as thickness increases. In order to predict whether slip bands are initiated or not during repeated heat treatments, σ_M must be compared with the critical stresses of Si wafer for slip bands to start. In Section III-3, we will derive the critical stress curves as a function of microdefect density.

3. Determination of critical stress curves obtained as a function of microdefect density on the base of the thermoelastic model

The yield stress of semiconductor has been described by the following equation⁽³¹⁾:

$$\sigma(T, \dot{\epsilon}) = C\dot{\epsilon}^{1/n} \exp(U/nkT) \quad (5)$$

where U is the activation energy of the glide movement; T , wafer temperature; k , the Boltzmann constant; $\dot{\epsilon}$, strain rate; and n and C , constants depending on the

Fig. 6 Patterns of slip bands due to gravitational stress in 200-mm-dia wafer (a) an X-ray topograph, (b) a schematic picture of the wafer in which elongated slip bands propagate in $\langle 110 \rangle$ directions.

Fig. 7 Calculated gravitational stress, plotted against distance (x) from the edge of the 300-mm-dia wafer. Wafer thickness is 775 μm . The letter A and B correspond to those in Fig. 3(b).

Fig. 8 Maximum gravitational stresses (σ_M) plotted against wafer thickness (t).

Fig. 9 A critical resolved shear stress versus wafer temperature curve (D) obtained by using 125 mm wafers with microdefect density of $5 \times 10^{13} \text{ m}^{-3}$. The curve (A) corresponds to the yield stress of dislocation-free Si crystals⁽⁷⁾. The wafers under thermal stress curve (1) got dislocated, while those under (2) kept dislocation-free. The critical resolved stress curve (D) was interpolated between curves (1) and (2), maintaining the exponential dependence on wafer temperature indicated by eq. (5)⁽¹⁵⁾⁽¹⁷⁾.

material. The yield stress is influenced not only by temperature and strain rate, but also to a marked degree by microdefect density⁽³⁾⁽⁴⁾⁽⁶⁾. Thus, the yield stress is expected to shift depending on the thermal cycles in the device process. Figure 9 shows an example on how critical stress for dislocation multiplication was determined by both experiments and calculations based on the thermoelastic simulation method⁽¹⁵⁾⁽¹⁷⁾, as previously reported⁽¹⁶⁾. In Fig. 9, curve (A) is the lower yield stress of dislocation-free Si crystals determined by tensile testing⁽⁷⁾. The yield

stress could be reduced in terms of precipitation softening because 125 mm sample wafers underwent the pre-heat treatments as described in Section II-2. The microdefect density for the sample wafers was $5 \times 10^{13} \text{ m}^{-3}$. Experiments were performed on thermally stressed wafers in a row under several process conditions; the insertion and withdrawal rate into and from the high-temperature furnace, otherwise constant. The sample wafers were sandwiched with five dummy wafers on the front and back sides. First, wafers in a row were pushed into the furnace with 30 cm/min at 1173 K and the initiation of slip dislocation was confirmed by X-ray topography. The thermal stress curve for that condition was calculated simultaneously and is plotted by closed circles in Fig. 9. Second, wafers were inserted at the rate of 10 cm/min and no slip dislocation was observed and its equivalent thermal stress is plotted by open circles in Fig. 9. Another three cases were performed in the same way. If the thermal stress exceeds the mechanical strength of Si wafers, a slip dislocation occurs. This fact means that the thermal stress surmounts the yield stress curve in Fig. 9. Summing up these results, the yield stress was interpolated between the dotted circles and open circles, maintaining the exponential dependence on wafer temperature indicated by eq. (5)⁽¹⁵⁾⁽¹⁷⁾. The obtained stress curve (D) can be regarded as the critical stress to initiate slip dislocations for the wafers with different microdefect density⁽¹⁶⁾.

The other three (B, C, E) were critical resolved shear stress curves obtained in a similar way⁽¹⁶⁾, as shown in Fig. 10. Curve (B) for the 200-mm-dia processed wafers had a microdefect density of $1 \times 10^{11} \text{ m}^{-3}$, curve (C) for 100-mm-dia ones had $2 \times 10^{13} \text{ m}^{-3}$, curve (E) for 100-

Fig. 10 Critical resolved shear stress curves versus wafer temperature obtained for wafers with various microdefect densities. The curve (A) corresponds to the yield stress of dislocation-free Si crystals. Horizontal bar (0.44 MPa) shows the gravitational stress for 300-mm-dia wafer.

mm-dia ones had $2 \times 10^{15} \text{ m}^{-3}$, respectively. These results show that the critical stresses are also reduced, depending on the density of microdefect as well as the yield stress. In the following calculation to predict dislocation multiplications due to both thermal stress and gravitational stress, curve (B) (200-mm-dia wafer) is used for the simulation in 300-mm-dia wafers, as shown in Section III-3 and Section III-4.

4. Onset condition of slip bands due to gravitational stress in 300-mm-dia wafers

The maximum resolved shear stress numerically calculated in Section III-2 is $4.4 \times 10^5 \text{ N/m}^2$ (0.44 MPa) for the 300-mm-dia wafer. At 1473 K in Fig. 10, the critical stresses of the processed wafers are $4.0 \times 10^5 \text{ N/m}^2$ for curve (B) and $1.8 \times 10^5 \text{ N/m}^2$ for curve (E). Considering the effects of stress concentration caused by shaping irregularities on the jig surface, there is a good reason that slip bands have already occurred in 200-mm-dia wafers at high temperatures, as shown in Fig. 6. In the 300-mm-dia wafer, similarly, such dislocations are highly likely to emerge at high temperatures. If we compare the gravitational stress ($4.4 \times 10^5 \text{ N/m}^2$) with the critical stresses, the temperatures to cause slippage are 1450, 1420, 1380, and 1320 K, corresponding to microdefect densities of curves (B), (C), (D), and (E), respectively. In order to avoid the onset of such dislocation, the process temperature should be less than 1320 K, even if the microdefect density of wafers is around $1 \times 10^{11} \text{ m}^{-3}$.

5. Dislocation occurrence due to thermal stresses for 300-mm-dia wafers as a function of microdefect density

Figure 11 compares the obtained critical stress curve (B) and induced thermal stresses under the determined process conditions for 150-, 200-, and 300-mm-dia wafers. In calculating the thermal stresses, the wafer insertion rate was assumed to be 3.33 mm/s, the wafer pitch was 6.35 mm, and the furnace temperature was set at 1123 K. The larger the diameter, the larger the thermal stresses were induced. The thermal stress for 300-mm-dia wafers exceeded the critical stress curve (B), implying that slippage would occur. In Fig. 12, the thermal stresses are compared with the critical stress by changing the insertion rate, otherwise set constant, in 300-mm-dia wafers. As the insertion rate is reduced from 3.33 to 0.83 mm/s, the thermal stresses are on the decline; consequently, suppression of slip dislocations can be expected. In Fig. 13, the dependency on wafer pitch is examined for the insertion rate of 1.66 mm/s. The results indicate that widening the wafer pitch provides a larger practical margin for suppressing slippage dislocations than reducing the insertion rate. For heat treatment of larger-diameter wafers, optimization for both implementation and process conditions is a key point in maintaining dislocation-free state to produce higher-performance devices at lower cost.

Fig. 11 Comparison between the critical stress curves (B) and thermal stresses for 150-, 200- and 300-mm dia wafers. Curves (A) and (B) are those plotted in Fig. 10.

Fig. 12 Dependency of insertion rates on thermal stresses in 300-mm-dia wafers.

6. Comparison between upper yield stress and critical stress curve

Figure 14 plots the critical stress against the amount of precipitated oxygen: it also replots the upper yield stress obtained by Yonenaga and Sumino⁽³²⁾. The critical stress currently obtained is about five times smaller than the upper yield stress. Wafer warpage, defined by the difference between the initial bow and the final warped conditions, should be less than 10 to 30 μm after heat treatments⁽²¹⁾. The yielding phenomenon is a state in which a crystal is stretched or compressed beyond its elastic region, where many dislocations move like a landslide. Practically, it is

Fig. 13 Dependency of wafer pitches on thermal stresses in 300-mm-dia wafers.

Fig. 14 Critical stresses plotted against precipitated amount of oxygen (C) and the upper yield stress obtained by Yonenaga and Sumino⁽³²⁾.

defined as an inflection point in the stress-strain curve when a crystal is deformed at a constant rate⁽⁴⁾⁽³¹⁾. In Si, the dislocation density at the yield point usually reaches 10^{12} – $10^{14}/\text{m}^2$ when crystals are deformed at around 1173 K. However, the dislocation density currently emerging in device processing is around 10^7 – $10^{10}/\text{m}^2$, which is far lower than that in the well defined yield point. Physically, we can say that the critical stress that we have described is in the pre-yield stage. We conjecture that the dislocations nucleated first at the site of stress concentration and then propagated under gravitational stress. Thus, irregularities of damages on surface originating in mirror polishing or caused by handling play an important role in dislocation multiplication, as has been reported⁽¹⁾.

A high concentration of oxygen in the atmosphere surrounding dislocations is known to remarkably reduce

their moving speed at around 920 K, depending on oxygen concentration level⁽³³⁾⁽³⁴⁾. As a result, in CZ wafers the pinning effect of oxygen at dislocations might be expected to resist warpage. However, it has been reported that the interaction energy between the oxygen and the dislocation should be lower than about 0.5 eV, even if an impurity accompanying a large misfit strain is assumed in Si⁽³⁴⁾. According to Sumino⁽³⁵⁾, it has been concluded that an extended impurity-rich or -lean region (the Cottrell atmosphere)⁽³⁴⁾ never develops around a dislocation in thermal equilibrium through dislocation-impurity interaction at temperatures where the atomic diffusion is active, as long as impurity concentrations typical in Si (e.g., in the case of oxygen, 5×10^{23} atoms/ m^3 or less) are concerned. At a high temperature of 1473 K, interaction between oxygen and dislocation might be too small to be detected. Therefore, the pinning effect due to oxygen does not play an important role in suppression of slip bands.

IV. Conclusion

Onset conditions for dislocations during heat-treating of large-diameter silicon (Si) wafers are investigated in a vertical-type furnace, both experimentally and theoretically on the basis of computer simulation. We analyzed that the introduction of slip dislocations caused by thermal stresses resulting from transient temperature variation, and by weight-related stresses due to bending moment, which have become prominent in 200-mm-dia wafers. We obtained several curves for the critical stress to predict slip initiation as a function of microdefect density on the basis of a thermoelastic model. Using the obtained critical curves we predicted, the conditions necessary to suppress slip dislocations in 300-mm-dia wafers, the wafer size for ULSI in the next generation. This is done by comparing the calculated thermal stresses originating from the transient temperature variations. Furthermore, we calculated the self-gravity-related stress due to the bending moment in the currently used wafer jig. We discussed the possibilities for slip occurrence for 300-mm-dia wafers when they are held at high temperature. Lastly, the physical meaning of the critical stress curve is discussed on the basis of the upper yield stress obtained in the conventional tensile tests.

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REFERENCES

- (1) K. Minowa and K. Sumino: *Phys. Rev. Lett.*, **69** (1992), 320.
- (2) J. R. Patel: *Discuss. Faraday Soc.*, **38** (1964), 201.
- (3) I. Yonenaga and K. Sumino: *Jpn. J. Appl. Phys.*, **21** (1982), 47.
- (4) K. Sumino: *Handbook on Semiconductors Materials*, Properties and Preparation, ed. by T. S. Moss and S. Mahajan, Elsevier

- Science B. V., North-Holland, 1994, vol. 3A (1994), p. 73.
- (5) J. R. Patel and A. R. Chaudhuri: *J. Appl. Phys.*, **34** (1963), 2788.
 - (6) I. Yonenaga and K. Sumino: *Phys. Status Solidi*, (a) **50** (1978), 685.
 - (7) W. Schröter, H. G. Brion and H. Sietoff: *J. Appl. Phys.*, **54** (1983), 1816.
 - (8) K. Morizane and P. S. Gleim: *J. Appl. Phys.*, **40** (1969), 4104.
 - (9) S. M. Hu: *J. Appl. Phys.*, **40** (1969), 4413.
 - (10) H. R. Huff, R. C. Bracken and S. N. Rea: *J. Electrochem. Soc.*, **118** (1971), 143.
 - (11) S. M. Hu, S. P. Klepner, R. O. Schwenker and D. K. Seto: *J. Appl. Phys.*, **47** (1976), 4098.
 - (12) B. Leroy and C. Plougonven: *J. Electrochem. Soc.*, **127** (1980), 961.
 - (13) G. Bentini, L. Corraera and C. Donolato: *J. Appl. Phys.*, **56** (1984), 2922.
 - (14) A. E. Widmer and W. Rehwald: *J. Electrochem. Soc.*, **47** (1976), 4098.
 - (15) I. Matsuba, K. Mokuya and T. Aoshima: *Proc. IEEE Int. Electron Devices Meeting*, IEEE, New York, (1986), p. 530.
 - (16) H. Shimizu and T. Aoshima: *Jpn. J. Appl. Phys.*, **27** (1988), 2315.
 - (17) K. Mokuya and I. Matsuba: *IEEE Trans. Electron Devices*, **36** (1989), 319.
 - (18) S. Hirasawa, T. Torii and T. Takagaki: *Heat Transfer Manufacturing and Materials Processing*, ASME, **113** (1989), 77.
 - (19) Y. Kosaka and A. Yoshinaka: The 52th Autumn Meeting of the Japan Society of Applied Physics, Okayama, October, 1992; (Advance Abstracts, vol. 1, 10a-SY-17, p. 262).
 - (20) Xin: Japan Society for the Promotion of Science, 145 Committee, Thermal Behavior of Si, Kohsaikaikan, Tokyo, Dec., 1994, p. 36.
 - (21) H. Shimizu, T. Watanabe and Y. Kakui: *Jpn. J. Appl. Phys.*, **24** (1985), 815.
 - (22) Chang-Ou Lee and P. J. Tobin: *J. Electrochem. Soc.*, **133** (1986), 2147.
 - (23) F. Shimura, H. Tsuya and T. Kawamura: *J. Appl. Phys.*, **51** (1980), 269.
 - (24) S. Kishino, Y. Matsushita, M. Kanamori and T. Iizuka: *Jpn. J. Appl. Phys.*, **21** (1982), 1.
 - (25) H. Bender: *Phys. Status Solidi*, (a) **86** (1984), 245.
 - (26) H. Shimizu, T. Naganuma, A. Kanai and N. Umemura: *Jpn. J. Appl. Phys.*, **32** (1993), 758.
 - (27) S. Timoshenko and D. H. Young: *Elements of Strength of Materials*, D. van Nostrand Co. Inc., Maruzenn Company, Ltd., Tokyo, 1976.
 - (28) S. K. Griffiths and R. H. Nilson: *Semicon/West*, 1995, Third 300 mm wafer specification workshop, San Francisco, California, July, (1995), attachment 8.
 - (29) S. Timoshenko and J. N. Goodier: *Theory of Elasticity*, McGraw-Hill Book Company, Inc., New York, (1951), p. 398.
 - (30) H. Shimizu *et al.*: to be published.
 - (31) H. Alexander and P. Haasen: *Solid State Phys.*, **22** (1968), 28.
 - (32) I. Yonenaga, K. Sumino and K. Hoshi: *J. Appl. Phys.*, **56** (1984), 2346.
 - (33) M. Imai and K. Sumino: *Philos. Mag.*, **A 47** (1983), 599.
 - (34) K. Sumino and M. Imai: *Philos. Mag.*, **A 47** (1983), 753.
 - (35) K. Sumino: *Materials Sci. Forum*, **105-110** (1992), p. 139.