1. Introduction

In 33-Mpixel 120-fps CMOS image sensors for full-spec Super Hi-Vision (SHV), a column-parallel high resolution (>12 bits) analog-to-digital converter (ADC) is the key element for low power and high quality imaging while realizing high pixel rate of 4 Gpixel/s. To meet this specification, a column-parallel 2-stage cyclic ADC has been developed, and a prototype sensor employing this ADC shows a sufficient image quality while consuming low power of 2.45W at 120 fps1, 2.

For further reduction of power consumption and area-efficient design, digitally calibrated ADC technique is useful3-5. The use of small capacitance in the ADC design leads to a reduction of power consumption and area of the column ADC. On the other hand, the small capacitance causes large non-linearity in the ADC because of a variety of errors generated in the analog circuits. Effectiveness of a calibration technique for improving a column-parallel cyclic ADC has been reported to overcome these problems6. However, the technique is dedicated for a single-stage fully differential cyclic ADC and the details of the calibration algorithm have not been reported.

This paper proposes a digital calibration algorithm for the 2-stage single-ended cyclic ADC suitable for SHV image sensors. The detailed calibration algorithm considering the error terms due to the 2-stage single-ended operation and the verification of the calibration algorithm by using simulation are described.

This paper is organized as follows: Section 2 describes a design and operation of the 2-stage cyclic ADC. Section 3 discusses the algorithm to compensate for the respective errors caused in the ADC in detail, and Section 4 describes the evaluation of the proposed algorithm by simulations. Finally, Section 5 presents concluding remarks.

2. 2-Stage Cyclic ADC

A schematic diagram of the 2-stage cyclic ADC with 12-bit resolution is shown in Fig. 1. An internal reference generation and return-to-zero (RTZ) digital-signal feedback technique6 are used in each stage of the ADC. Each stage uses 1.5-bit architecture, which generates 3-state redundant binary (RB) codes expressed with two decision levels (2 bits) for each cycle to relax the comparator’s precision demand7. The ADC consists of a single-ended amplifier, two capacitors ($C_{CA}$ and $C_{CB}$) for the first-stage ADC; $C_{CB}$ and $C_{CB}$ for the second-stage ADC.
ADC), sub-ADC with two comparators, switch transistors, and a digital-to-analog converter (DAC) with a decoder. The sampling capacitor \(C_{cA}\) is divided into \(C_{c1A}\) and \(C_{c2A}\), and \(C_{cB}\) is divided into \(C_{c1B}\) and \(C_{c2B}\) for generating internal reference with high accuracy.

The operation of the 2-stage cyclic ADC is as follows. 1) After all the capacitors in the first-stage ADC are reset, the analog input signal is sampled by turning on the \(S_{SA}\) and \(S_{S}\) to introduce the signal into the sub-ADC that outputs the most significant digit. 2) Then, the code controls the switches in the DAC that must be turned on, and the input is multiplied by a gain of two and subtracted from a reference level which is determined by the combination of the output of the sub-ADC and the reference voltages, \(V_{RH}\) and \(V_{RL}\), connected to DAC. 3) After the amplification phase, the residual signal is returned to the input node of the first-stage ADC and the second significant digit is determined by the sub-ADC.

The amplification and the feedback phases are repeated three times to obtain the first 4 bits of resolution in the first-stage ADC. During the amplification phase of the last cycle, the amplifier’s output of the first-stage ADC is connected to the second-stage ADC by turning on the switch \(S_{SB}\) to transfer the analog residue of the first-stage ADC to the second-stage ADC. After this sampling phase of the second-stage ADC, \(S_{SB}\) is turned off and the amplification and feedback phases are repeated eight times in the second-stage ADC to obtain the last 8 bits of conversion, for a total of 12 bits. While the second-stage ADC processes the AD conversion, the first-stage ADC samples and converts the next pixel signal, which means these two ADC stages work as pipelined fashion to accelerate the AD conversion.

3. Digital Calibration

Assuming that \(V_{RH} = V_i\) and \(V_{RL} = 0\) in the amplification phase described above, the ideal transfer curve of the single-ended cyclic ADC is shown in Fig. 2. The relationship between the input \(V_{in}\) and output \(V_{out}\) is expressed as

\[ V_{out} = 2V_{in} - DV \]

(1)

where \(D\) denotes the output RB code of the sub-ADC that takes 0, 1/2, and 1.

As the analog components in the ADC have a variety of errors, the actual output is not expressed as Eq. (1). Fig. 3 shows the cause of these errors in a single-stage cyclic ADC. These errors include the mismatch between the capacitor pair \((C_c, C_p, C_{c1},\) and \(C_{c2})\), finite gain error and incomplete settling error of the amplifier as described in Ref [8]. In addition to these errors, an incomplete settling error caused in the period when the
analog residue of the first-stage ADC is transferred to the second-stage ADC is considered in this paper.

### 3.1 Capacitor mismatch

In the amplification phase, an actual output including the capacitor mismatch could be written by

\[ V_{\text{out}} = \left( 1 + \frac{C_f + \Delta C}{C_f} \right) V_r - \frac{C_f + \Delta C}{C_f} \cdot DV \left( 1 + D_s \cdot \frac{1}{2} \right) \]  

where \( \Delta C \) denotes the capacitor mismatch between \( C_f \) and \( C_s \), which is defined as \( \Delta C = C_s - C_f \). \( \Delta C_s \) denotes the capacitor mismatch between \( C_{s1} \) and \( C_{s2} \), which is defined as \( \Delta C_s = C_{s1} - C_{s2} \), and \( D_s \) is a constant that is equal to 0 as \( D = 0 \) or 1 and equal to 1 as \( D = 1/2 \). Let the capacitor mismatch errors be defined as \( e_m = \Delta C / C_f \) and \( e_{mc} = \Delta C_s / C_s \), then Eq. (2) is expressed as

\[ V_{\text{out}} = \left( 2 + e_m V_r \right) - \left( 1 + e_m D \right) \left( 1 + D_s \cdot \frac{e_{mc}}{2} \right) \]  

By dividing \( V_r \) for both side of Eq. (3), Eq. (4) is given by

\[ X_{\text{in}} = \frac{V_i}{V_r} \]  

where \( X_{\text{out}} = V_{\text{out}} / V_r \) and \( X_{\text{out}} = V_{\text{out}} / V_r \). In the cyclic ADC, \( X_{\text{in}} \) is defined as \( X(i+1) \). Therefore, from Eq. (4), \( X(i+1) \) is expressed as

\[ X(i+1) = (2 + e_m)X(i) - (1 + e_m)D(i) \left( 1 + D_s \cdot \frac{e_{mc}}{2} \right) \]  

where \( D(i) \) and \( D_s(i) \) are \( D \) and \( D_s \) for the \( i \)-th conversion step, respectively. The ideal output for the \( i \)-th conversion step is 2X(i) - D(i), so the error \( E_m(i+1) \) for the \( i \)-th conversion step caused by the capacitor mismatch is given by

\[ E_m(i+1) = e_m(X(i) - D(i)) - \frac{e_{mc}}{2}(D(i)D_s(i)) \]  

Total error due to capacitor mismatch is given by summing up \( E_m(i+1) \) for \( i = 1 \) to 12. In the 2-stage cyclic ADC, the two stages have different capacitor mismatches. Therefore, an input-referred total error \( E_{m,t} \) due to the capacitor mismatch for the case that the first 3 cycles and the rest of 8 cycles are performed by the first and second stages, respectively, is expressed as

\[ E_{m,t} = \sum_{i=1}^{3} e_{mc}(X(i) - D(i)) - \frac{e_{mc}}{2}(D(i)D_s(i)) + \sum_{i=4}^{12} e_{mc}(X(i) - D(i)) - \frac{e_{mc}}{2}(D(i)D_s(i)) \]  

where \( e_{mcA} \) and \( e_{mcB} \) denote the capacitor mismatch error between \( C_{s1} \) and \( C_{fA} \) for the first-stage ADC and \( C_{s2} \) and \( C_{fB} \) for the second-stage ADC, \( e_{mcA} \) and \( e_{mcB} \) denote the capacitor mismatch error between \( C_{s1A} \) and \( C_{fA} \) for the first-stage ADC, and \( C_{s2B} \) and \( C_{fB} \) for the second-stage ADC, respectively. If the error of the raw digital output is small enough, \( X(i) \) can be approximated as

\[ X(i) = D(i)2^{-1} + D(i+1)2^{-2} + D(i+2)2^{-3} + \cdots + D(i+11)2^{-12} \]  

where \( i \) takes the integer ranging from 1 to 12 due to the ADC resolution of 12 bits. By substituting Eq. (8) to Eq. (7), \( E_{m,t} \) is obtained as follows.

\[ E_{m,t} = e_{mc}2^{-1}(-D(4)+D(5)2^{-1}+D(3)2^{-2}+\sum_{i=4}^{12} D(i)2^{-i-1}) \]

\[ + e_{mc}2^{-2}(-D(4)+2^{-1}\sum_{i=4}^{12} D(i)2^{-i}) \]

\[ - e_{mc}2^{-3}\sum_{i=4}^{12} D_s(i)2^{-i-1} - e_{mc}2^{-2}\sum_{i=4}^{12} D_s(i)2^{-i} \]  

### 3.2 Finite gain error of the amplifier

The finite gain of the amplifier causes the non-linearity error. In the amplification phase, an actual output including the finite gain error could be written by

\[ V_{\text{out}} = \left( 2 - e_{fg}V_r \right) - \left( 1 + e_{fg}D \right) \left( 1 + D_s \cdot \frac{e_{mc}}{2} \right) \]  

where \( G_o \) is an open loop gain and \( C_f \) is an input capacitance of the amplifier. Let the finite amplifier's gain error be defined as \( e_{fg} = (C_s + C_f) / C_f G_o \). In a cyclic ADC, the error \( E_{fg}(i+1) \) for the \( i \)-th conversion step caused by the finite gain of the amplifier is given by

\[ E_{fg}(i+1) = e_{fg}(-2X(i) + D(i)) \]  

which is obtained by the same manner as mentioned in subsection 3.1. In the 2-stage 12-bit cyclic ADC, the input-referred total error \( E_{fg,t} \) due to the finite gain of the amplifier is also calculated as

\[ E_{fg,t} = -e_{fg} \left( \sum_{i=2}^{12} (i-1)D(i)2^{-i} + \sum_{i=4}^{12} D(i)2^{-i} \right) \]

\[ - e_{fg} \left( \sum_{i=4}^{12} (i-4)D(i)2^{-i} \right) \]

where \( e_{fgA} \) and \( e_{fgB} \) denote the finite amplifier's gain error of the first-stage ADC and the second-stage ADC, respectively.

### 3.3 Incomplete settling error of the amplifier

The finite bandwidth of the amplifier causes the incomplete settling error. The actual output including the finite settling time \( t_s \) could be written by

\[ V_{\text{out}} = 2(1 - e_s)\left( 1 - e_s \right) \]  

where \( e_s \) is the finite amplifier's gain error. In a cyclic ADC, the error \( E_s(i+1) \) for the \( i \)-th conversion step caused by the incomplete settling is given by

\[ E_s(i+1) = e_s(-2X(i) + D(i)) \]
If the influence of slewing is ignored, the settling error \( e_{st} \) is expressed as \( e_{st} = \exp(-\omega pt_{st}) \) with the bandwidth of the amplifier \( \omega_p \) and the settling time \( t_{st} \). It is affected by both the feedback factor and the effective load capacitance. During the third amplification phase in the first-stage ADC, the first-stage ADC is connected to the second-stage ADC operated in the sampling phase, as shown in Fig. 4, so effective load capacitance of the amplifier in the first-stage ADC is increased by adding the capacitance of \( C_{cB} \) and \( C_{fB} \) in the second-stage ADC. Therefore, the incomplete settling error in the last cycle of the first-stage ADC is larger than that in the first two cycles. The input-referred total error \( E_{st,j} \) due to the incomplete settling is calculated in the same manner as Eq. (9).

\[
E_{st,j} = -e_{st}2^{-j} \left[ D(2) + D(3) + 2 \sum_{i=4}^{12} D(i)2^{-i} \right] - e_{stB} \sum_{i=1}^{12} D(i)2^{-i} - e_{st} \sum_{i=4}^{12} D(i)2^{-i} \tag{15}
\]

where \( e_{st} \) and \( e_{stB} \) denote the settling errors of the first-stage ADC and the second-stage ADC, respectively, and \( e_{stAB} \) denotes the settling error of the first-stage ADC at the third amplification phase.

### 3.4 Calibration method

The three kinds of errors mentioned in subsections 3.1-3.3 are assumed to be small enough to ignore the higher order terms. Therefore, the error factor \( E_{total} \), which means the resulting input-referred total error due to the capacitor mismatch, the finite gain error and the incomplete settling error is the summation of each input-referred total errors calculated by Eqs. (9), (12), and (15) as

\[
E_{total} = E_{st,j} + E_{og,j} + E_{st,t}
\tag{16}
\]

The calibrated digital output \( D_{calib} \) is calculated by subtracting the error factor \( E_{total} \) from the raw digitized output.

\[
D_{calib} = \sum_{j=1}^{12} D(i)2^{-j} - E_{total}
\tag{17}
\]

where \( D(i) \) is a RB code expressed with two decision level \( (D_1, D_0) \), that is, \( (0, 0) \) for \( D(i) = 0 \), \( (0, 1) \) for \( D(i) = 1/2 \), and \( (1, 0) \) for \( D(i) = 1 \). Therefore, the output code has 13-bit word length after performing RB to binary (B) conversion. The calibrated output given by Eq. (17) has 13-bit resolution. The final 12-bit calibrated output is obtained by rounding the least significant bit of the 13-bit code.

### 4. Calibration Performance

Simulations are conducted to verify the effectiveness of the proposed calibration method. Table 1 shows the values of errors that we set in this simulation. A several errors written in red letters are set large enough to make the input-referred errors larger than \( 1/2 \) LSB for verifying the digital calibration algorithm performance.

Fig. 5 (a) shows the simulation results of the DNL with errors whose values are shown in Table 1. Because of the large values of errors that we set for simulation, the maximum DNL is \( +4.5 / -1.5 \) LSB, and many missing codes are occurred due to the errors. Fig. 5 (b) shows the simulation results after the digital calibration. As mentioned in the subsection 3.4, digital calibration is performed with 13-bit output code, which is one bit longer than the desired resolution of 12 bits. With this one extra bit for the digital calibration, the DNL is theoretically improved within a half of LSB. The maximum DNL is reduced to \( +0.49 / -0.48 \) LSB and there is no missing code.

The maximum INL before calibration is \( +7.5 / -1.5 \) LSB which is caused by the large values of errors, as shown in Fig. 6 (a). In this simulation result, offset and overall gain error are included. On the other hand, the maximum INL after calibration is improved drastically.

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**Table 1** Values of errors that we set in the simulation.

The values written in red letters are large enough to make the input-referred errors larger than \( 1/2 \) LSB.

<table>
<thead>
<tr>
<th>Errors</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>( e_{stA} )</td>
<td>( 3.8 \times 10^5 )</td>
</tr>
<tr>
<td>( e_{stB} )</td>
<td>( 7.5 \times 10^5 )</td>
</tr>
<tr>
<td>( e_{ogA} )</td>
<td>( 2.7 \times 10^5 )</td>
</tr>
<tr>
<td>( e_{ogB} )</td>
<td>( 5.4 \times 10^5 )</td>
</tr>
<tr>
<td>( e_{stAB} )</td>
<td>( 3.0 \times 10^5 )</td>
</tr>
<tr>
<td>( e_{ogAB} )</td>
<td>( 8.7 \times 10^5 )</td>
</tr>
<tr>
<td>( e_{st} )</td>
<td>( 8.3 \times 10^5 )</td>
</tr>
<tr>
<td>( e_{stB} )</td>
<td>( 9.1 \times 10^5 )</td>
</tr>
<tr>
<td>( e_{stAB} )</td>
<td>( 3.0 \times 10^5 )</td>
</tr>
</tbody>
</table>
to +0.23/–0.27 LSB, as shown in Fig. 6 (b).

The capacitor mismatch errors, and the incomplete settling error caused in the last cycle of the first-stage ADC (e_{CA1}) are set large enough to make the input-referred errors larger than 1/2 LSB as shown in Table 1. Therefore, the simulation results show the capacitance C_{CA}, C_{FA}, C_{CB}, and the bias current of the amplifier I_{RA} (first-stage ADC), I_{RB} (second-stage ADC) are designed smaller than those in Ref [1][2], which means that the proposed digital calibration method not only improves the output characteristics but also reduces the power consumption and layout area of the ADC in the image sensor.

5. Conclusion

In this paper, we have proposed a digital calibration algorithm for a 2-stage cyclic ADC with 12-bit resolution used in a 33-Mpixel, 120-fps CMOS image sensor for full-spec Super Hi-Vision. The algorithm can compensate for errors due to the capacitor mismatch, the finite gain error, and the incomplete settling error, and it dramatically improves the nonlinearity of the ADC. This technique enables the sensitivity against non-idealities of the analog circuits in the ADC to be reduced, which results in the reduction of power consumption and layout area of the ADC in the image sensor.

References


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