Dark Current Characterization of Low-noise CMOS Global Shutter Pixels Using Pinned Storage Diodes

Keita Yasutomi (member)†, Taishi Takasawa †, Shoji Kawahito (fellow)†

Abstract This paper describes dark current characterization of two-stage charge transfer pixels, which enable a global shuttering and kTC noise canceling. The proposed pixel uses pinned diode structures for the photodiode (PD) as well as the storage diode (SD), thereby a very low dark current is expected. In this paper, effects of negative gate biasing and temperature dependency are discussed with device simulations and measurement results. The measured dark current of the PD and SD with the negative gate bias results in 19.5 e-/s and 7.3 e-/s (totally 26.8 e-/s) at ambient temperature of 25°C (the chip temperature is approximately 30°C). This value is much smaller than that of conventional global shutter pixels, showing the effectiveness of use of the pinned storage diode.

Key words: CMOS Image Sensor, dark current, global shutter, two-stage charge transfer, kTC noise free.

1. Introduction

Recently, true-correlated double sampling (CDS) global shutter (GS) pixels\textsuperscript{1}–\textsuperscript{4} have been developed, and the noise level of GS CMOS image sensors (CISs) has been improved to a few electrons. Taking advantage of such a low noise performance requires low dark current less than 100e-/s in order to keep the noise floor from the shot noise of dark current\textsuperscript{5}. However, no CMOS GS pixels which can satisfy low dark current characteristic have been reported.

A five-transistor (5T)-GS pixel\textsuperscript{1} with a correlated quadruple sampling (CQS) technique offers kTC noise canceling while suppressing 1/f noise at the cost of the frame rate to be half. The pixel, however, suffers from high dark current at a charge storage node due to the use of a floating diffusion as an analog memory. In the eight transistor (8T) pixel\textsuperscript{2}, the kTC noise is cancelled by a CDS with in-pixel sample-and-hold capacitors. Since the sampling capacitors should be small to maintain a high fill factor, causing relatively high leakage and the thermal noise induced by the sampling capacitors. The two-stage charge transfer pixels\textsuperscript{3,4} using a pinned storage diode have demonstrated its low-noise performance and a high shutter efficiency. Though the pixel structure is suitable for reduced dark current, the measured dark current is still higher than rolling shutter CISs.

This paper describes dark current characterization of the two-stage charge transfer pixels using pinned storage diodes under negative gate bias conditions for charge transfer gates. The negative gate biasing\textsuperscript{7}–\textsuperscript{10} is a well known method to suppress dark current due to Shockley-Read-Hall (SRH) surface generation process. In this paper, temperature dependence of the photodiode (PD) and storage diode (SD) dark current under negative gate biasing is also described.

The remainder of the present paper is organized as follows. In Section 2, the pixel structure and operation are shown. Section 3 describes measurement methods and conditions for dark current characterization. Section 4 presents the experimental results and discussion about effects of temperature dependency and negative gate biasing. Conclusions are presented in Section 5.

2. Pixel implementation

Figs.1 and 2 show the proposed pixel structure, the potential profile and the layout. Compared with the previous design for the dual global shutter\textsuperscript{3,4}, the pixel is simplified for a single global shutter and consists of six transistors and two pinned diodes: a PD and SD. The PD has a role of photoelectron generation and storage, while the SD has a role of charge storage only.

The pixel introduces a dual doping technique and shielding structure to meet a high charge transfer efficiency and shutter efficiency. By means of the dual doping technique, the PD and SD have different con-
centrations of n-type dopant: \(n_1\) and \(n_2\), and the potential difference between the PD and SD are built to be higher charge transfer efficiency (CTE). Stepwise potential created by \(p_1\) under the GS gate also enhances the CTE. It has another p-type doping (\(p_2\)) beneath the \(n_2\) layer for charge shielding. This shielding layer improves the shutter efficiency to be 99.7% at incident light wavelength of 550nm\(^4\). The dominant source of shutter leakage is carriers which are generated at deep substrate and diffuse into the SD. Therefore, the shutter efficiency can be improved with higher concentration of \(p_2\) doping than that of the p-type substrate\(^11\).

**Fig. 3** shows the timing diagram of the pixel. For every pixel, a signal charge accumulated in the PD is transferred to the SD with the GS gate. The SD stores the charge until the pixel row is selected to be read. The signal charge is transferred to a floating diffusion (FD), and is read out in the same manner as that of rolling-shutter-based four transistor (4T) pixel, i.e., a true CDS is accomplished. Since the kTC noise is canceled, the noise level is as low as that of rolling shutter CMOS imagers.

Generally, there are three components in dark current: the generation current generated in depletion layer (depletion dark current), the generation current at Si-surface (surface dark current), and the diffusion current generated in the bulk neutral region (diffusion dark current). In the proposed pixel, both the PD and SD employ a pinned-diode structure, which can suppress surface dark current.

In pinned diode structures, it is well known that edges of the transfer gates and shallow trench isolation (STI) become the primary source of dark current\(^9\)\(^{12}\)\(^{13}\). The edges of PD are covered by \(p_1\) layer, which helps to attract holes there. Also in the SD, STI edges are covered by \(p_1\) layer to reduce the depletion dark current as shown in Fig.2. While, the channels both under the GS gate (along A-A’) and under TX gate (along B-B’) is not covered by \(p_1\) layer, causing large depletion dark current. This depletion dark current can be suppressed by applying the negative gate bias technique discussed in Section 4.

### 3. Measurements

A test chip with the proposed pixels is fabricated in a 0.18um CIS technology shown as **Fig.4**. In this paper, measurement results of 3 (H) × 480 (V), totally 1440 pixels are described. The pixel size is 7.5 × 7.5 \(\mu\)m\(^2\), and the fill factors of the PD and SD area are approximately 20% and 14%, respectively. The signal from a pixel is digitized by a 13-bit column cyclic ADC, and then, the digital code is read out.

The dark currents are measured by the gradient of the plot of the dark signal versus integration time of the PD and SD. As shown in **Fig.3**, only the integration time of the PD, \(T_{a,PD}\), is varied from approximately 15s to 30s to measure the PD dark current. Similarly, only the integration time of the SD, \(T_{a,SD}\), is varied for the measurements of SD dark current. These measurement methods allow us to measure the PD and SD dark currents separately. Although the exact integration time of SD dark signal is different from row to row as shown in Fig.3, the time difference (e.g. \(\Delta T_{a,SD}(1 - 2)\)) is much smaller than the common integration time, \(T_{a,SD}\), thereby making it negligible.
4. Results and Discussion

4.1 Effects of negative gate biases

Fig. 5 shows the measured SD dark current as a function of $V_{GSL}$ or $V_{TXL}$ where, $V_{GSL}$ and $V_{TXL}$ are low levels of GS and TX gate pulses, respectively. In the measurements, either $V_{GSL}$ or $V_{TXL}$ is varied from 0V to -1.0V in order to measure the effect of the negative gate biasing on the SD dark current. The ambient temperature is 25°C, and the chip temperature is approximately 30°C. As shown in Fig.5, the negative gate bias of the TX gate effectively suppresses the SD dark current, and the dark current with $V_{TXL} = -1.0V$ is measured to 1/3 of that of $V_{TXL} = 0V$.

Fig.6(a) shows the simulation results of potential distribution along B-B’ in Fig.2. In Fig.6(b), magnified views at various $V_{TXL}$ are shown. At the $V_{TXL}$ of 0V, the depletion region is extended to beneath the TX gate, resulting in the SD dark current to be large. As the $V_{TXL}$ become negative, the surface beneath the TX gate become gradually a pinning condition, resulting in the SD dark current to be small. The surface potential rapidly decreases up to the $V_{TXL}$ of -0.6V. When $V_{TXL}$ is less than -0.6V, the surface is sufficiently pinned, and a region in which the depletion region touch the surface at the edge of TX is slightly reduced.

Fig.7 shows the simulation results of potential distribution along A-A’. Similar to the negative bias on TX gate, as the $V_{GSL}$ become more negative, the depletion region of SD become shallow at the edge of GS gate. As the surface potential beneath the GS gate is negative, the region is filled with holes, reducing the SD dark current. As shown in Fig.5, the dark current reduction effect of negative gate bias on GS gate is smaller than that of the TX gate. This is because the region without the $p_1$ layer under the GS gate is about half of that under the TX gate.

The cumulative probabilities of the SD dark current at various biases of $V_{TXL}$ and $V_{GSL}$ are shown in Figs.8-9. The negative gate bias effectively reduces the number of “hot” pixels. For instance, in Fig.8, the number of pixels which have dark current of over 200e-/s is 2% of entire pixels at $V_{TXL}=0V$, and it is reduced to be approximately 0.3% at $V_{TXL}=-1.0V$. Similarly, in Fig.9, the number of pixels with the SD dark current of over 200e-/s at $V_{GSL}=-1.0V$ is reduced to half of that at $V_{GSL}=0V$.

Figs.10 and 11 show the measured PD dark current as a function of $V_{GSL}$ and the cumulative probability, respectively. The negative gate bias of the GS gate has no significant effect to the PD dark current. As shown in Fig.7, the surface potential at the PD-side edge of GS gate is negative even at $V_{GSL}=0V$. Therefore the
p1 layer creating the stepwise-potential under GS gates helps to attract a hole accumulation at Si-surface, and the surface dark current is suppressed sufficiently.

The large negative gate bias leads to the increase of another dark current component due to Gate-Induced-Leak (GIL) Trap Assisted Tunneling (TAT) process \[^{10}\], which appear in a region with large electric field. Fig. 10 and Fig. 11, however, do not show significant increase in the PD dark current for $V_{GSL}$ of up to -1.0V. This is because the potential profile at PD-side beneath the GS gate is almost unchanged in the range of -0.4V to -1.0V as shown in Fig. 7. Therefore, the PD dark current generated from GIL-TAT process was not observed in this sensor.

### 4.2 Temperature dependency

Temperature dependency of dark current gives its activation energies, which are useful to clarify their physical reason of the dark current generation. The activation energy is found from the Arrhenius plot\[^{14}\] expressed by

\[
D = D_{e0,\text{diff}}T^3 \exp \left( \frac{-E_{a,\text{diff}}}{kT} \right) + D_{e0,\text{dep}}T^{3/2} \exp \left( \frac{-E_{a,\text{dep}}}{kT} \right)
\]

where $D_{e0,\text{diff}}$ and $D_{e0,\text{gen}}$ denote pre-factors in e-/s of diffusion and depletion dark current, respectively. $k$ and $T$, respectively, represent Boltzmann coefficient and absolute temperature. $E_{a,\text{diff}}$ and $E_{a,\text{gen}}$ stand for activation energy of diffusion and depletion dark current, respectively.

Fig. 12 shows the temperature dependence of PD and
SD dark current distributions for various $V_{GSL}$ voltages. In this measurement, both $V_{GSL}$ and $V_{TXL}$ are set to -1.0V. The activation energy of PD dark current is 1.12eV, which is the same as the band-gap energy of Si, $E_g$. Therefore, the diffusion current is dominant in the PD dark current. On the other hand, the dominant sources of SD dark current are different at operating temperatures. At low temperatures below 25°C, the activation energy of SD dark current is $E_g/2$, which indicates that the depletion dark current is dominant. At high temperatures over 50°C, the activation energy equals to $E_g$. Therefore the diffusion dark current of the SD is ten times smaller than that of the PD by the use of shielding structure.

As shown in Figs.5 and 12, the depletion current of SD is larger than that of PD even when the negative gate biasing is applied. The residual depletion current of SD may be due to imperfect hole accumulation at the surface of pinned diode structure and transfer gates, which can be reduced by increasing doping concentration of the pinned layer (p+) and minimizing area of the charge-transfer channel under transfer gates.

5. Conclusions

In this paper, the dark current characteristics of the two-stage charge transfer global shutter pixel are presented. By means of the negative bias technique, total dark current is reduced to 26.8 e-/s (PD:19.5 e-/s, SD: 7.3 e-/s) at ambient temperature of 25°C (the chip temperature is approximately 30°C), which is much smaller than that of other global shutter pixels.

From the Arrhenius plot, the diffusion dark current of the SD is reduced to be ten times smaller than that of the PD, showing an advantage of the proposed pixel
for reduced dark current. In the present structure, the diffusion current in the PD is dominant. Therefore, the further reduced dark current can be achieved by using other structures such as an n-substrate and thin epi substrate.

References

1) B Fowler, C. Liu, S. Mims, J. Balicki, W. Li, H. Do, J. Appelbaum, P. Vu, “A 5.5Mpixel 100 frames/sec wide dynamic range low noise CMOS image sensor for scientific applications” in Proc. of SPIE-IS&T, pp. 753607-1-753607-7 (Feb. 2010)