A Highly Ultraviolet Light Sensitive and Highly Robust Image Sensor Technology Based on Flattened Si Surface

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Abstract In this paper, an ultraviolet light (UV-light) sensitive and highly robust Si photodiode technology based on atomically flattened Si surface is summarized and its application to a CMOS image sensor is demonstrated. By forming a surface high concentration layer of photodiode with steep dopant profile uniformly on flattened Si surface, the almost 100% internal quantum efficiency to UV-light waveband and negligibly small degradation of photo-sensitivity were achieved for both n+pn and p+np photodiodes. The developed photodiode technology was applied to a 5.6 µm pixel pitch front-side-illuminated CMOS image sensor. The fabricated sensor chip exhibited a spectral response to a wide light waveband of 200-1000 nm, and the sensitivity degradation did not occur after the strong UV-light exposure stress.

Keywords: photodiode, CMOS image sensor, ultraviolet light, Si surface.

1. Introduction

Photodiode (PD) light sensors, PD arrays and image sensors with a wide spectral response, including ultraviolet light (UV-light) waveband of 200-380 nm, are strongly required in the fields of various spectrophotometric analysis, biological phenomena analysis, environmental assessment and space vision1)~4). For the image sensor development, an improvement of UV-light sensitivity and an improvement of sensitivity robustness to UV-light exposure have been challenges5) 6). Especially, due to the short penetration depth of UV-light in Si, an atomic scale control of the dopant profile of the light incident side Si surface region to form a photo-generated carrier drift layer is required7). UV-light sensitive backside illuminated (BSI)-CCD, BSI-CMOS with additional backside surface treatment process, and detector-on-Si type CMOS imagers with UV-light sensitive materials as detector have been reported8)~10). In this paper, a PD technology based on an atomically flattened Si surface for the formation of the thin surface high concentration layer with a steep dopant profile uniformly is summarized, and its application to a CMOS image sensor in-pixel PD is demonstrated. In the next section, the PD concept, experimental results and discussions of n+pn and p+np PDs are shown. In addition, evaluation results of the electrical characteristics of SiO2/Si system at various UV-light irradiation times are summarized to discuss the origin of sensitivity change due to UV-light exposure. In section 3, a 5.6 µm pixel pitch front-side-illuminated (FSI) CMOS image sensor with the developed PD technology is demonstrated.

2. Photodiode Technology

2.1 The Concept

Fig.1 shows the depth from Si surface where the integrated amount of incident light decreases to 90% and 37% due to the absorption as a function of the wavelength.
wavelength, calculated by the absorption coefficient in Si. The photo-generated carriers within top few atomic layers of Si must be collected to sufficiently increase the UV-light sensitivity. However, if the interface states of the SiO₂/Si system are activated, these act as sensitivity loss and dark current generation spots through recombination/generation processes. Therefore, it is required for the surface high concentration layer of buried PD to generated electric field that drift photo-generated carriers and to form surface neutral region to passivate the interface states. For this purpose, a thin surface high concentration layer with steep dopant profile must be formed. In order to form such dopant profile uniformly with an ion implantation process, Si surface flatness is one of the most crucial parameter. Fig.2 (a) shows the typical Si surface after RCA cleaning which employs alkali solution and hot water. Conventionally, Si surface contains unsuitable roughness such as the peak-to-valley of the micro-roughness of about 1 nm. In the developed PD technology, the atomically flattened Si surface shown in Fig.2 (b) obtained by ultrapure Ar ambient annealing process is employed[9]~11).

2.2 Experimental Results and Discussions

In order to evaluate the effect of the dopant profile of surface high concentration layer and the impact of the Si surface flatness to PD characteristics, n’pn PDs were fabricated either on conventional Si surface or atomically flattened Si surface with various ion implantation conditions for surface n⁺ high concentration layer formation. The fabrication process flow and ion implantation condition are summarized in Fig.3 and Table 1, respectively. The illustration of cross-sectional view of PD is shown in Fig.4. All of the fabricated PDs’ area in this section is 1.0 mm² with the circle shape. For the Si surface atomically flattening process, an ultrapure Ar ambient annealing process was carried out[9]~11). The ion implantations for the buried p layer and the surface n⁺ layer were carried out through an oxide film formed by oxygen radical oxidation process. With this oxidation technology, the atomic flatness at the SiO₂/Si interface is preserved[9] 10). Here, the thickness of the ion implantation through oxide was 7.0 nm. The projected ranges of As⁺ were within the oxide film for both 3 and 10 keV cases. A spike rapid thermal annealing (RTA) was carried out at 950 °C in order to activate the n⁺ dopant while maintaining the steep dopant profile. A 190 nm-thick non-doped silicate glass (NSG) film was deposited above the PD by an atmospheric pressure chemical vapor deposition process at 400 °C. Fig.5 shows the dopant profile of the fabricated PDs measured by secondary ion mass

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**Table 1** Process conditions of the fabricated n’pn PDs.

<table>
<thead>
<tr>
<th>Sample</th>
<th>SiO₂/Si interface flatness</th>
<th>As⁺ implantation condition</th>
<th>Average surface n⁺ layer thickness [nm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Conventional</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>B</td>
<td>Conventional</td>
<td>3</td>
<td>6.8 x 10¹³</td>
</tr>
<tr>
<td>C</td>
<td>Atomically Flat</td>
<td>3</td>
<td>6.8 x 10¹³</td>
</tr>
<tr>
<td>D</td>
<td>Atomically Flat</td>
<td>10</td>
<td>3.4 x 10¹³</td>
</tr>
</tbody>
</table>

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**Fig.2** AFM images of (a) a typical Si(100) surface after RCA cleaning and (b) an atomically flat Si(100) surface.

**Fig.3** n’pn PD fabrication flow.

**Fig.4** Schematic illustration of the cross-sectional view of the fabricated n’pn PDs.

**Fig.5** Depth profiles of arsenic and boron from the Si surface for the fabricated n’pn PDs measured by SIMS.
spectrometry (SIMS). Steep dopant profiles were formed for both cases of As⁺ implantation energy of 3 and 10 keV. The dopant concentration of 3 keV case is smaller than that of 10 keV case due to the shallower implanted dopant profile by the through-oxide implantation process. Note that the difference between the sample B and C was not confirmed in SIMS result, indicating the average dopant profile is the same in these samples. The quantum efficiencies (Q.E.) of the fabricated PDs were evaluated before and after the UV-light exposure stress using an on-wafer characterization system, where the measured wavelength is 200-1000 nm. For the UV-light exposure stress, a super high pressure mercury discharge lamp was employed. Typical UV-light intensities were 2.0, 4.4, 8.8 and 17.6 mW/cm² for the wavelengths of 254, 303, 313 and 365 nm, respectively. The spectral distribution of the employed UV-light source is shown elsewhere.

**Fig.6** Q.E. as a function of wavelength of the fabricated n⁺pn PDs (samples A-D) measured at various UV-light irradiation times.

Fig.6 shows the Q.E. as a function of wavelength for the fabricated PDs measured at various UV-light irradiation times. **Fig.7** shows the Q.E. before the UV-light exposure at the wavelength of 250 nm. As initial characteristics, PDs formed on the atomically flat Si surface exhibit a high sensitivity to UV-light waveband: almost 100 % internal Q.E. levels for 200-300 nm. Comparing the data of samples B and C in Fig.7, the impact of the atomically flatness is clearly confirmed in the average values and the variations.

This result indicates that the atomically flat Si surface can enlarge the process margin for the formation of suitable surface high concentration layer. For the sample D, the sensitivity degradation due to the UV-light exposure stress was negligibly small across the whole measurement waveband. On the contrary in other samples, changes of Q.E. were clearly confirmed after the UV-light exposure stress. In sample A, the UV-light sensitivity is initially low, and it increased after the UV-light exposure stress. In samples B and C, the UV-light sensitivity is initially at an intermediate level and high, respectively, and they decreased after the UV-light exposure stress. With the result of Fig.6 (c), assuming the initial internal Q.E. for 200-300 nm is 100 %, the width of surface sensitivity dead zone was calculated using the following equation.

$$\frac{\int_{X_D}^{\infty} \exp(-ax)\,dx}{\int_{0}^{\infty} \exp(-ax)\,dx} = \frac{Q.E. \text{ after UV–light exposure}}{\text{initial Q.E.}}$$

(1)

where, $X_D$ and $\alpha$ are the width of the surface sensitivity dead zone and absorption coefficient, respectively. After UV-light irradiation for 10000 min, the $X_D$ for the wavelength of 200-300 nm were almost identical, and the value was 7 nm. To investigate the origin of UV-light sensitivity change, electrical characteristics of the SiO₂/Si system were evaluated at various UV-light irradiation times using capacitance-voltage (C-V) measurements of MOS capacitors with a physically detachable mercury probe. Here, the mercury probe was attached at the top of the NSG film only during the C-V measurement. For this experiment, the thickness of interfacial oxide film formed by oxygen radical oxidation was varied from 2.4 to 10 nm. **Fig.8** (a) shows the fixed charge density as a function of the UV-light irradiation time for the interfacial oxide film thickness of 7.0 nm.

The negative fixed charges and its variation increased as increasing the UV-light irradiation time. **Fig.8** (b) shows the fixed charge as a function of the interfacial oxide thickness after the UV-light irradiation for 100
The negative fixed charge and its variation increased as decreasing the interfacial oxide thickness. In addition, an increase of interface state was confirmed as increasing the UV-light irradiation time for all the conditions from the C-V curves. These results indicate that for the fabricated SiO₂ films above Si, negative fixed charges tend to be accumulated by the UV-light exposure, and the position of the fixed charges is in the NSG film. The trapping of the excited electron by UV-light into existing electron traps in the NSG film which is supposed to be greater than hole traps is considered to explain this effect. These fixed charges induce a potential change in Si. When the surface high concentration layer does not exist or, the total dopant concentration is not sufficient to encounter the electrical flux of the fixed charges, Si energy band is bent, and this induces the changes of UV-light sensitivity. The detailed energy band bending and its relationship to the sensitivity change for each case are discussed in 13). The quality of the SiO₂/Si system especially around the interfacial region is thus important in addition to the surface dopant profile. The following samples were fabricated to verify this experimentally. For the sample E: n⁺pn PD, an additional oxygen radical oxidation process was carried out between the surface As⁺ ion implantation and the NSG deposition processes shown in Fig.3. By this additional oxidation process, interfacial oxide film was grown 1.0 nm more than the initial value (7.0 nm). The aims of this process are following: to form a high quality SiO₂/Si interface which was possibly damaged by the As⁺ ion implantation, and also to increase the interfacial oxide thickness to reduce the fixed charge increment during the UV-light exposure.

For the sample E, the As⁺ ion implantation condition was modified to result in forming the same arsenic dopant profile as the sample D after the fabrication process. Also, as sample F, a p⁺np PD was fabricated. In the sample F, the ion implantation conditions for the buried n layer and the surface p⁺ layer were, P⁺ 36 keV 3.0 x 10¹² cm⁻² and BF₂⁺ 9 keV 5.0 x 10¹³ cm⁻², respectively. For the sample F, the additional interfacial oxidation process was also carried out. The boron SIMS profile of the sample F is shown in Fig.9. The Q.E. characteristics were evaluated for the samples E and F. For sample E, the obtained Q.E. curve was almost identical to that of the sample D. For the sample F, the result is shown in Fig.10. Figs.11 (a) Q.E. over initial Q.E. and (b) dark current of fabricated PDs (samples D~F) as functions of UV-light irradiation time.
The characteristics of sample D is shown as reference. Both samples E and F show stable Q.E. characteristics to the UV-light exposure stress with negligible degradations. An increase of dark current confirmed in the sample D was significantly improved in the sample E. This is considered to be due to the improved integrity of SiO₂/Si interface by the additional interfacial oxidation process. In the sample F, the dark current was the smallest of all the fabricated samples, i.e., 2~4 x 10⁻¹⁰ A/cm² and no degradation was observed after the UV-light exposure stress. As shown in Fig.8, negative fixed charges increases in the oxide film above the fabricated PDs in these experiments. This induces hole accumulation at the SiO₂/Si interface in the case of p⁺np PD fabricated in this work, which results in passivating the interface states. This is considered to be the reason why the better dark current performance was obtained for p⁺np PDs in comparison to the n⁺pn counterparts. Fig.12 shows the summary of the PDs structure achieving the high UV-light sensitivity and the high stability to the strong UV-light exposure. Followings are the key features and technologies.

1. Sufficiently high dopant concentration at the top few nanometer Si surface to form a thin neutral region to passivate the interface states. For an example, in order to sufficiently suppress the energy band bending within three atomic layers in Si due to the electric flux of the increased fixed charges in the order of 10¹² cm⁻², the dopant concentration at the surface should be higher than 4 x 10¹⁹ cm⁻³.
2. Steep dopant profile of the surface high concentration layer to form an electric field to drift photo-generated carriers to the buried layer. The electric field of this surface high concentration layer is induced by space charges of depletion layer and gradient of the carrier concentration of top neutral region.
3. Low concentration junction between the surface high concentration layer and the buried layer. The purpose of this is to reduce the electric field at the pn junction to suppress the dark current. In addition, the junction depth (Xj) and dopant concentration at the junction should be designed so that the depletion layer does not reach the incident light side Si surface.
4. Atomic scale flatness of SiO₂/Si interface. It is required so as to form the above mentioned thin and steep dopant profile uniformly.
5. Small trap density insulator film above the PD suppressing the fixed charge generation due to trapping of the carriers excited by high photon energy UV-light.

In addition, following process technologies are also important; a low energy ion implantation process for steep surface high concentration layer dopant profile formation, and a low thermal budget annealing process for activation of the steep-profile dopant and defect recovery. The above mentioned key features are to be important for both FSI and BSI cases.

3. CMOS Image Sensor Application

3.1 Chip Design and Fabrication

A 5.6 µm pixel pitch FSI CMOS image sensor with buried pinned-PD having the surface photo-generated electron drift layer explained in the previous section was fabricated. The lateral overflow integration capacitor (LOFIC) pixel architecture was employed for a high conversion gain (CG) and a high full well capacity (FWC) performance¹⁴) ¹⁵). A wide dynamic range and high sensitivity linear response imaging is achieved with a single exposure by CMOS image sensor with LOFIC¹⁴) ¹⁵). The image sensor chip was fabricated using a 0.18 µm 1P3M CMOS process technology. The employed Si wafer substrate has 20 µm-thick p-type epitaxial layer on n-type substrate. The final Si wafer thickness after the fabrication was 600 µm. For the formation of thin and steep p⁺ layer, process conditions related to the Si surface flatness, ion implantation for PD and activation anneal were tuned to integrate the highly UV-light sensitive and highly stable PD: the SiO₂/Si interface flatness was maintained at the same level as the gate oxide/Si interface, the shallow BF₂⁺ implantation was carried out through a thin oxide film, and a rapid thermal annealing process equivalent to the activation process of the S/D high concentration region was applied.
as the dopant activation anneal for the surface high concentration layer of PD. The $X_j$ of the PD was about 80 nm. **Fig.13** and **Table 2** show the micrograph and the design specification of the developed chip, respectively. The chip did not have microlens.

### 3.2 Evaluation Results

From the measured photoelectric conversion and the signal/noise characteristics, the CG, the dark random noise, and the FWC were 110 $\mu$V/e-, 2.1 e-, and $1.6 \times 10^5$ e-, respectively. The dynamic range was 97 dB. Due to the small floating diffusion (FD) capacitance and a large LOFIC capacitance, high CG and FWC were simultaneously obtained. The PD dark current at 60 °C was 6.4 e-/sec-µm² which is normalized by the pixel area, and no increase of dark current was detected due to the UV-light exposure stress explained next. The fabricated chip was exposed to the UV-light stress to evaluate the sensitivity and dark current stabilities. The same UV-light source explained in the previous section was employed for this experiment. Spectral response and dark current were measured before and after the UV-light exposure. **Fig.14** shows the spectral response of the fabricated CMOS image sensor measured before and after the UV-light irradiation for 1000 min.

**Table 2** Design specifications of the fabricated CMOS image sensor.

<table>
<thead>
<tr>
<th>Process technology</th>
<th>0.18 $\mu$m 1P3M CMOS with buried pinned-PD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Die size</td>
<td>$9.5H \times 9.5V$ mm²</td>
</tr>
<tr>
<td>Pixel size</td>
<td>$5.6H \times 5.6V$ µm²</td>
</tr>
<tr>
<td>Number of pixels</td>
<td>Total $1312H \times 968V$</td>
</tr>
<tr>
<td></td>
<td>Effective $1280H \times 960V$</td>
</tr>
<tr>
<td>Fill factor</td>
<td>26 %</td>
</tr>
</tbody>
</table>

shows the captured sample images of a stuffed doll, fruit and other objects, an incandescent lamp and a white paper with a picture (the Musubimaru) drawn by a sun block cream containing a UV-light absorbent. (a) the image taken with a D65 lamp without optical filters and (b) the image taken with a germicidal lamp having the center wavelength of 254 nm and an UV-light transmission filter. Both images were taken with an UV-light transmission lens, PENTAX B2528UV.

**Fig.15** Captured sample images of a stuffed doll, fruit and other objects, an incandescent lamp and a white paper with a picture (the Musubimaru) drawn by a sun block cream containing a UV-light absorbent. Two different ambient light conditions were applied during the image capturing. For Fig.15 (a), D65 lamp was exposed to the samples and no optical filters were attached to the camera lens. The ambient light contains a broad spectral distribution from 300 to at least 800 nm. For Fig.15 (b), germicidal lamp was exposed to the samples and an UV
transmission filter having a narrow transmittance distribution at around 254 nm was attached to the camera lens. For both cases, an UV-light transmission lens: PENTAX B2528UV was employed in the camera. The picture on the white paper is clearly observed when the germicidal lamp was irradiated showing the fabricated CMOS image sensor successfully captured the UV-light image.

4. Conclusions

In this paper, key features and the process technologies of PD to achieve almost 100 % internal Q.E. to UV-light waveband with a high stability of light sensitivity and dark current to strong UV-light exposure were summarized based on the experimental results. The degradation of light sensitivity of PD occurs due to the interface state and fixed charge generation that induces the surface dead zone ranging about 7 nm. Both n’pn and p’np PDs with the structure having the surface high concentration neutral region and steep dopant profile formed on atomically flattened Si surface solve this stability issue and exhibit high UV-light sensitivity and high stability of sensitivity and dark current to strong UV-light exposure. The developed PD process technology was applied to the buried pinned-PD of a 5.6 µm pixel pitch CMOS image sensor, and a wide spectral sensitivity of 200-1000 nm as well as no degradation of photo-sensitivity were successfully achieved. The developed PD technology is applicable to various types of Si image sensors and array sensors for wide waveband light detection and imaging.

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References

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