A Low Noise CMOS Image Sensor with Pixel Optimization and Noise Robust Column-parallel Readout Circuits for Low-light Levels

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Abstract  A low noise high sensitivity CMOS image sensor (CIS) is developed for low-light levels. The prototype sensor contains the optimized 1-Mpixel with the noise robust column-parallel readout circuits. The measured maximum quantum efficiency is approximately 60% at 660nm, and the long-wavelength sensitivity is also enhanced by a large sensing area and an optimized process. In addition, a low dark current of 0.96pA/cm² at 292 K, a low temporal random noise in a readout circuitry of 1.17e⁻rms, and a high pixel conversion gain of 124 µV/e⁻ are achieved. The implemented CMOS imager using 0.11 µm CIS technology with a pinned photodiode has a very high sensitivity of 87V/lx·sec that is suitable for the scientific applications such as medical imaging, bioimaging, surveillance cameras, and so on.

Keywords: CMOS image sensor, low noise, high sensitivity, folding-integration/cyclic analog-to-digital converter (ADC).

1. Introduction

CMOS image sensors (CISs)¹-³ should satisfy several prerequisite conditions for scientific applications such as a high sensitivity, a fast readout speeds, a low noise, and a wide spectral response. A variety of challenges and try for improving the performances of CMOS imagers have been studying in many institutes, academics, and companies. For example, the high performance column analog-to-digital converters (ADCs)⁴-⁷ for increasing the signal-to-noise ratio (SNR), the novel pixel structures⁸-¹¹ for reducing the in-pixel noises and improving the sensitivity, and the optimization of CIS process¹²-¹³ are developing and implementing. To achieve all requirements for the scientific cameras, we used the optimized CIS process, the efficient chip architecture, and the high performance column-parallel ADC¹⁴-¹⁵. In addition, the developed imager keeps a quite large pixel size for obtaining the enough fill factor. Simultaneously, the doping concentration of the p-type epixial layer is modified for expanding the detecting range, particularly, the longer wavelength lights, and a low temporal noise performance is achieved by the powerful noise reduction capability of readout circuitry.

In this paper, a high performance CMOS image sensor is introduced and evaluated for demonstrating the suitability as the scientific and industrial applications.

2. Architecture and operation of developed image sensor

Fig. 1 shows a block diagram of the developed CMOS image sensor. The prototype chip consists of a pixel array (pixel pitch: 11.2 µm), a hybrid (analog/digital) correlated double sampling (CDS) circuit, a column-parallel folding-integration (FI)/cyclic ADC array, a scanner for addressing, a timing generator (TG), a serial parallel interface (SPI) block, a reference voltage and current block, and a low voltage differential signaling (LVDS) for buffering the signal. The pixel type is a typical four-transistor active pixel sensor (APS) with pinned photodiode (PPD) and it has a sufficiently large fill factor of 44%. As can be seen in Fig. 1, the developed imager is based on the high performance column-parallel folding-integration/cyclic ADCs¹⁴-¹⁵. This helps significantly to reduce the temporal random noise in the readout circuitry as well as keeping the dynamic range without any signal loss.

Fig. 2 shows a simplified block diagram of the column-parallel FI/cyclic ADC with its timing diagram in one horizontal period. The analog core for both ADCs is composed of an amplifier, a capacitor, and switches. Both
ADCs are implemented once in the reset period and signal period, respectively. RT is a control signal for the initialization at the floating diffusion (FD) node and TX is for the accumulated charge transfer in active pixels. During the reset period, the output signal \( V_p \) from the pixel is sampled multiple (M) times by the switch \( \Phi_{FI-ADC} \), and the FI-ADC is carried out. After FI-ADC operation for the reset level sampling, the configuration of the analog core is changed by turning on the switch \( \Phi_{C-ADC} \). In the cyclic ADC mode, the final integrator output in the FI-ADC mode is converted into the digital codes. The operation of the folding-integration and cyclic ADCs for the signal level is the same as that of the reset level sampling.

Fig. 3 shows the more detailed operation of the folding-integration and cyclic ADCs. In Fig. 3(a), one cycle is composed of a sampling phase and a charge-transfer phase. In the sampling phase, one comparator is used, and the amplifier output is compared with a reference of \( (V_{RH} + V_{RL})/2 \), where \( V_{RH} \) and \( V_{RL} \) are the high and low level reference voltages, respectively. In order to attain the gain of half in each sampling, only one capacitor \( C_{1a} \) is used in the FI-ADC mode. This is
necessary to control the output signal range of the folding integration to be the same as that of the cyclic ADC. The operation phases, a feedback sampling phase and an amplification phase, for the cyclic ADC are shown in Fig. 3(b). Unlike the FI-ADC mode, in the cyclic ADC mode, two comparators are used for the 1.5b sub-ADC, and the sub-A/D conversion is performed during the feedback sampling phase. Then the charge-amplification is implemented. For obtaining the 13 bits resolution in the cyclic ADC, the switched analog core performs 12 cycles of the cyclic A/D conversion.

In the conventional integration, the output increases linearly in small input signal region, and then saturates. In the folding integration, however, the analog signal amplitude is controlled to a limited range by the folding, while applying a high gain by the integration. The folded number is counted by a digital counter in column circuitry, and the digital code of the counter output is used for the most significant bit (MSB) side of the final digital output. The digital code by the cyclic ADC is used for least significant bit (LSB) side. Using these digital codes which are obtained in reset and signal period, respectively, the digital CDS operation is performed on chip to achieve greatly reduced vertical fixed pattern noise (vFPN). The used column-parallel readout circuits make possible to improve the noise performance, sensitivity, and dynamic range of the developed CMOS image sensor.

Fig. 4 shows the layout block diagram for high-speed signal readout. The pitch of the column readout circuitry is 5.6 µm. Each column in pixel array has two column readout units, and it makes to increase the readout speed twice as fast as a typical column-parallel readout type CISs. For example, normally total integration time is \( i \text{ rows} \times 1 \text{ horizontal period} (1H) \). By using the proposed manner, however, total integration time can be reduced by half \( (0.5 \cdot i \text{ rows} \times 1H) \). In other words, the signal can be slowly read out compared to the CISs with the typical column-parallel readout circuitry under the same conditions, especially, the operation speed of imagers. The pixel signal is sampled with an enough settling time and it assists to reduce the sensor’s error.

3. Measurement results and discussion

A 1-megapixel (1024 x 1024) CIS chip is implemented with 0.11-µm standard CMOS technology with pinned photodiode. The photograph of the prototype CMOS camera with developed imager is shown in Fig. 5.

The noise as the equivalent number of electrons is calculated with the measured pixel conversion gain which is determined with photon shot noise measurement. Fig. 6 shows the measurement random and photon shot noise as a function of the signal level. The conversion gain is measured to be 124 µV/e\(^-\) at \( \Delta V_{R}=1.0V \) and \( M=128 \). Fig. 7 shows the cumulative probability of the pixel dark current at 292K. The dark current of the developed imager is measured to be 7.55 e\(^-\)/s (median), which corresponds to a current density of 0.96pA/cm\(^2\). The photodiode is far away from the pixel isolator, e.g., shallow trench isolation (STI) structures. This structural feature helps to remove the dark signal components resulting from the interface defects around the isolation.

The monochrome quantum efficiency (QE) curve (at 400 to 1000nm) measured by the prototype sensor is shown in Fig. 8. As mentioned before, the doping concentration of the p-type epitaxial layer is optimized for expanding the detection range. Consequently, the
developed imager achieves a peak QE of 57% at 660nm and relatively wide spectral sensitivity; the imager has a good enough spectral characteristic for targeted applications. Fig. 9 demonstrates the superiority of the developed image sensor’s sensitivity at the longer wavelength compared with the previous work.14) Especially, at the wavelength range from 780 to 1000nm, the relative QE of the developed imager is approximately twice as good as the conventional one.

Fig. 10 shows the captured image at very low light level 0.01 lx with M=128 in the FI-ADC. In this setting the total ADC resolution is 19 bits with the 13 bits from the cyclic ADC. The developed imager has a low temporal random noise in readout circuitry of $1.17e^{-}$ rms. As a result, we have obtained a very clean still image under the dark scene without any off-chip processing. But a few white pixel defects are observed in a part of the captured image. This problem can be solved by using the advanced process technology. Table I summarizes the performance of the prototype chip. The imager has a relatively large pixel (11.2 x 11.2 µm²) with the large fill factor and the wide spectral sensitivity (see Fig. 9). These characteristics make possible to achieve a high sensitivity of 87V/lx · sec at 3746K light source with IR cut filter and a high full well capacity of the PPD.

4. Conclusion
A low noise and high sensitivity CMOS image sensor is introduced and demonstrated in this paper. For high-end measurement applications, the CMOS imagers are required to meet the several key parameters. The developed imager has the high peak QE of 57% with
wide spectral sensitivity, high conversion gain of 124 μV/e-, large well capacity of 40 ke-, good enough low noise performance, and relatively wide dynamic range of 70.5 dB. From these results, we confirmed that the developed imager can be sufficiently used for scientific and industrial applications.

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References


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