1. Introduction

Image sensors are utilized in various fields such as food analysis, biological science, remote sensing and so on\(^1\)-\(^5\). As for the image sensor in this field, a wide spectral sensitivity, a high robustness to ultraviolet (UV) light, a high input referred conversion gain (CG) and a high full well capacity (FWC) are important as basic performances. The image sensor that achieves these performances is utilized not only for image measurement, emission and absorption analyses, but also spectral imaging which obtain spectral information in two dimensional image.

Light sensing for various wavelength such as a UV and a near-infrared (NIR) light and various light intensity conditions has following challenges.

Regarding UV light, the penetration depth of UV light in Si is short. In order to increase the UV light sensitivity, the photo electrons generated within several nanometers from Si surface must be collected. Therefore it is required to form electric filed in the surface penetration region of UV light. However, if the interface states of the SiO\(_2\)/Si are activated, it causes a loss of sensitivity and generation of the dark current\(^6\)-\(^7\). Thus the dopant profile of a Si surface must be carefully adjusted to improve UV light sensitivity without degradation. When Si is irradiated by UV light, the photo carriers have sufficient energy to be injected to SiO\(_2\). Thus some of the excited photo carriers are trapped in SiO\(_2\) and become fixed charges. This charging of SiO\(_2\) causes a change of potential near the photodiode (PD) surface. In addition, interface states are generated by UV light irradiation. Due to these fixed charges and interface states, UV light sensitivity tends to be degraded\(^6\)-\(^7\). To solve these issues, it has been reported that forming a high concentration p\(^+\) layer with steep dopant concentration profile on the flattened Si surface in the PD is effective to consistently achieve high UV light sensitivity and high robustness to UV light exposure\(^8\)-\(^9\).

Regarding NIR light, in order to increase the NIR light sensitivity, the electrons generated over several micron meters from Si surface must be collected. Therefore it is required to form sensible region deeply in Si.

In addition, for spectrophotometric analyses and spectral imaging, incident light levels for a wide
waveband often vary significantly. For instance, low and high intensity light of different wavelength emitted by different samples should be detected simultaneously in the emission analysis. Therefore an image sensor is required to achieve a high sensitivity and a wide DR at the same time. However, in case of forming floating diffusion (FD) capacitance \( C_{FD} \) small in the conventional four-transistor-pixel (4T-pixel), a high input referred CG can be obtained whereas transferred photoelectrons from a PD would be overflowed. Hence a full well capacity (FWC) is restricted. Therefore it is challenging issue to achieve a high CG and a high FWC simultaneously. In order to solve this issue, many solutions have been reported\(^{10-22}\). A lateral overflow integration capacitor (LOFIC) CMOS image sensor is one of its solutions\(^{23,24}\). In a LOFIC CMOS image sensor, saturated photoelectrons from PD during integration period are integrated at large capacitance LOFIC. Therefore it achieves high CG signal under a low illumination and high FWC signal under high illumination in one exposure.

A CMOS image sensor which has high sensitivity and high robustness to UV light, a high CG and a wide DR simultaneously has been already reported\(^{25}\). In this sensor, in order to achieve high sensitivity and high robustness to UV light, above mentioned dopant profile was formed on the flattened Si surface. Also, in order to achieve a high CG and a wide DR, a LOFIC was introduced. It has achieved performances of a high sensitivity for a wide waveband of 190-1000 nm, a high robustness to super high pressure mercury discharge lamp irradiation used as a UV light, a input referred CG of 110 \( \mu \text{V/e}^- \) and a DR of 97 dB.

In this paper, the technology and performance results of the developed CMOS image sensor with improved CG and high robustness to deuterium lamp will be described. The developed CMOS image sensor has sufficiently high concentration in Si surface to maintain the sensitivity and dark current robustness against the deuterium lamp irradiation. Furthermore, the \( C_{FD} \) was reduced by omitting the LDD implantation process before sidewall formation to reduce gate overlap capacitance. In the next section, key technologies and structure of the developed CMOS image sensor are summarized. In section 3, chip measurement results are described. Finally conclusion is presented in section 4.

2. Design of Fabricated CMOS Image Sensor

2.1 PD Structure of Wide Spectral Response and High Robustness

Fig. 1 and 2 show a layout and cross sectional view of the pixels of general 4T-pixel CMOS image sensor and developed CMOS image sensor in this work.

Regarding the robustness of UV light sensitivity and dark current toward UV light exposure, deuterium lamp which has light intensity peak at around 200 nm is employed for stress evaluation in this work as described in section 3. Here, the deuterium lamp is often used for absorption spectrophotometric analyses. For the surface p\(^+\) layer, terminating the line of electric force with fixed charge and passivating interface states generated by deuterium lamp irradiation stress should be considered. Therefore the dopant concentration of top surface neutral region is tuned sufficiently high to fulfill them. Also, steep dopant concentration profile of p\(^+\) layer was formed in order to generate a drift field for photo electrons generated by UV light. In addition, the concentration of the junction between the surface high concentration p\(^+\) layer and the buried n layer was tuned low. This structure reduces the electric field to suppress the dark current.
In the CMOS image sensor fabrication flow in this work, process steps related to the Si surface flatness, the implantation and the activation annealing of high concentration layer on the Si surface were modified from the conventional ones to achieve the above mentioned characteristics. The flatness of the PD's Si surface was maintained as the same level as the gate insulator film/Si surface in order to form the high concentration p⁺ layer on the Si surface uniformly. The CMOS image sensor was fabricated on p-epitaxial layer on n-type Si substrate. In order to improve the sensitivity to NIR light, the thickness of the p-epitaxial layer was 20 µm.

2.2 Pixel Structure of High CG and High FWC

In order to reduce the $C_{PD}$ for achieving high CG, various ways have been reported\(^2\)\(^4\)-\(^2\)\(^6\)-\(^2\)\(^7\). As for the result from analysis of $C_{PD}$ components with the similar structure and process technology to developed CMOS image sensor, a gate overlap capacitance, a p–n junction capacitance and a metal capacitance account for $C_{PD}$ in decreasing order\(^2\)\(^7\). Therefore, it is critical to reduce the gate overlap capacitance accounting for the highest percentage of $C_{PD}$. In the FD and the drain of the pixel SF in this work, the implantation process of a lightly doped drain (LDD) was not carried out. Therefore, a self-aligned n⁺ diffusion was formed with reduced overlap. It leads to the reduction of gate overlap capacitance. Also, the implantation process of channel stop under FD was not carried out. This contributes to the reduction of p–n junction capacitance. Regarding the metal capacitance, the wiring between FD and the pixel SF was connected short, and the other wirings near the FD were separated from it. It leads to the reduction of metal capacitance. Then the transferred photoelectrons from the PD can be converted to the high voltage.

However, under high illumination condition, transferred photoelectrons from the PD would be overflown from the small PD. Hence a FWC is restricted low. For solving this tradeoff, a large capacitance LOFIC was connected to the FD through the S gate as shown in Fig. 2. Then, under a low illumination condition, integrated photoelectrons are completely transferred from the PD to the small capacitance FD, and high sensible signal is read out. On the other hand, under a high illumination condition, saturated photoelectrons overflow from the PD to small capacitance FD and the large capacitance LOFIC. Therefore the integrated photoelectrons are completely transferred from the PD to FD+LOFIC. In this circuit, two signals from FD, FD+LOFIC are read out in one time exposure. Since the CG and the FWC can be determined independently, it is possible to achieve high CG and wide DR simultaneously.

2.3 Process Technology for Integrating Independent Devices

In this work, a PD with high concentration p⁺ layer with steep dopant concentration profile on the flattened Si surface, a FD without LDD implantation, a pixel SF with buried channel and LOFIC with MOS capacitor must be integrated into a CMOS image sensor. We have developed a CMOS image sensor process technology that integrated all of the above mentioned device components in a series of process flow. The activation annealing is carried out to the whole devices. Then the orders of ion implantations and activation annealing process steps and their conditions must be carefully tailored to optimize all of the performances simultaneously.

For the pixel circuit architecture, vertical and horizontal shift registers and analog memories were placed in the peripheral region surrounding the pixel array as shown in Fig. 3. The outputs from analog memories are amplified by column source follower drivers. The high CG signals: N1 and N1+S1 and high FWC signals: N2 and N2+S2 read out from each pixel are subtracted respectively at the correlated double sampling circuit outside the chip, where N1 and S1 indicate the reset noise and photo-signal at FD, and N2 and S2 indicate reset noise and photo signal at FD+LOFIC, respectively. The fabricated chip micrograph is shown in Fig. 4. The supply voltage is 3.3 V. The pixel pitch is 5.6 µm. The number of effective pixels is 1280×960 pixels, and the fill factor is 30.4 %.

![Fig. 3 Block diagram with pixel and column circuits.](image-url)
The process technology was 0.18 µm 1-poly-Si and 3-metal CMOS image sensor process with buried pinned PD. The quartz was attached as the package lid to transmit wide light waveband to the sensor.

3. Measurement Results and Discussion

Fig. 5 shows the photoelectric conversion characteristics of the fabricated chip. The vertical and horizontal axes indicate input referred effective signal electron and the relative illuminance, respectively. The light source is HDF-51F: Dainippon printing company using four fluorescent lights: FL15W. This graph consists of the S1 and S2 signals obtained under low and high illumination, respectively. The device performances resulted in a high CG of 240 µV/e–, a high FWC of 200 ke– and wide DR of 101 dB. It was confirmed that a good linear response was obtained by one time exposure.

Fig. 6 shows the measurement system of spectral response. The light source is ultra-high brightness and high stability broadband source EQ-99: Energetiq Technology Inc. The bandwidth of the light source is 190-1100 nm using the monochromator SPG-120UV: Shimadzu Corporation. Light passes through a second order optical cut filter. Fig. 7 shows the spectral distribution of the X2D2 lamp used for the UV light exposure stress. The typical UV light intensities are 82.9, 120.6 and 31.7 µW/cm² for the wavelength of 180, 204 and 300 nm, respectively. UV light irradiation stress was applied up to 220 hours of irradiation time. The total amount of the light source after 220 hour was 65.7, 95.5 and 25.1 J/cm² for the wavelength of 180, 204 and 300 nm, respectively. Fig. 8 shows the spectral response of the fabricated CMOS image sensor before and after X2D2 lamp irradiation. For reference, quantum efficiency (QE) characteristic of the W pixel of formerly reported WRGB LOFIC CMOS image sensor is also shown. These QE were normalized by the maximum QE of each sensor. For all cases, high QE was obtained for a wide light waveband of 190-1000 nm. Especially the internal QE was almost 100% in UV light waveband while the conventional sensor is beginning to show a sensitivity over 300 nm. Furthermore, a NIR sensitivity
of conventional sensor is decreasing steeply over 520 nm. The local swing of the spectral response is due to transmission characteristic of the oxide film. For both results of before and after the stress, the high photo sensitivity was confirmed for a wide waveband of 190-1000 nm. In addition, the sensitivity degradation after strong UV light exposure was negligibly small. Dark current degradation due to strong UV light exposure was not detected as shown in Fig. 9.

Fig. 10 shows sample images under various conditions. The light conditions during image capturing were, (a) black light with band pass filter having a narrow distribution of waveband from 300 to 370 nm, (b) D65 lamp with IR cut filter having a broad distribution from 300 to at least 800nm, and (c) NIR light without optical filter having a distribution peak at 940 nm. An UV light transmission lens, PENTAX B2528UV was employed for capturing image (a). The left column images show a hand. In image (a), it was clearly observed that many spots absorbed UV light and in image (c) the blood vessel absorbed NIR light. On the other hand, the right column images show a flower. It was clearly observed that in image (a) the nectar guide absorbed UV light and in image (c) the flower reflects NIR light. The developed CMOS image sensor has successfully captured images under UV light, Visible light and NIR light with high sensitivity and high FWC performance.

Table 1 shows the design specifications and performances of the fabricated chip. The input referred CG is 240 µV/e−, the total dark random noise is 1.7 e−, the FWC is $2.0 \times 10^5$ e−, and the DR is 101 dB. The spectral response range is for 190-1000 nm. During each measurement, the frame rate was 5 frames per second.

4. Conclusion

A CMOS image sensor with input referred CG of 240 µV/e−, FWC of 200 ke−, spectral response of 190-1000 nm and high robustness to UV light was demonstrated by introducing the following key technologies; small capacitance of FD structure with LOFIC pixel and surface high concentration p+ layer with steep dopant concentration profile in PD. The developed CMOS image sensor described in this work is expected to be utilized in various food and biological science fields.

References

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<th>(b) Visible light</th>
<th>(c) NIR light (940nm)</th>
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**Fig.10** Sample images under various light conditions. The light conditions during image capturing were, (a) black light with band pass filter having a narrow distribution of waveband from 300 to 370 nm, (b) D65 lamp with IR cut filter having a broad distribution from 300 to at least 800 nm, and (c) NIR light without optical filter having a distribution peak at 940 nm. An UV light transmission lens, PENTAX B2528UV was employed for capturing image (a).

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