Floating Capacitor Load Readout Operation for Small, Low Power Consumption and High S/N Ratio CMOS Image Sensors

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Abstract Floating capacitor load readout operation for small, low power consumption and high S/N ratio CMOS image sensors and its effects are demonstrated. This readout operation utilizes a floating capacitor load instead of a constant current load as pixel SF driver, and the parasitic capacitor of pixel output vertical signal line as column sample/hold capacitor. Using a 0.18 μm CMOS image sensor technology, two CMOS image sensors were fabricated to verify the effects. The ratio of pixel area to the total effective area is over 92 %. The power consumption for pixel signal readout and pixel readout noise were decreased by over 97 % and 63.8 %, respectively. Also a higher readout gain and a wider linear response range were obtained. Furthermore, it was confirmed that this readout operation becomes more advantageous when decreasing the power supply voltage, which is favorable for ultra-low power sensor network system applications.

Keywords: CMOS image sensor, floating capacitor load readout operation, small chip size, low power consumption, low noise, RTN.

1. Introduction

In recent years, small, low power consumption and high S/N ratio image sensors are highly desired in many fields such as medical, factory automation, mobile application and so on. In the fields that require small image sensor, conventionally, CCD image sensors have been used because they have smaller chip size than CMOS image sensors. A small chip size is easily achieved with a CCD image sensors especially an interline transfer CCD (ITCCD) sensor, because the ITCCD image sensor consists of a pixel array of photodiodes (PDs) and vertical CCDs, a horizontal CCD and an output buffer only. However, CCD image sensors consume large power because they have to drive all CCD to transfer charge simultaneously. On the other hand, CMOS image sensors consume lower power than CCD image sensor because their signals are readout from pixels in the form of voltage. However, CMOS image sensor has large chip size because they consist of pixel array and large size peripheral circuits of vertical and horizontal shift registers, output buffers, current sources and analog memories. Consequently, it is difficult for conventional image sensors to achieve simultaneously small chip size and low power consumption. In the last few years, stacked CMOS image sensor technologies, which enable CMOS image sensor to achieve more functionality in a smaller chip size were reported. The stacked CMOS image sensors consist of two stacked substrates. One substrate includes a pixel array and a part of readout circuits, and the other substrate includes the main part of readout circuits and image signal processing circuits. Additionally, in the field of low power consumption, imagers using pulse width modulation (PWM) technology were reported to be effective. In PWM imagers, pixel signals are readout by density of pulse waves. In the field of high S/N ratio image sensor, the column parallel high gain amplifiers, column parallel analog-digital converter (ADC), correlated multiple sampling (CMS) technology have been reported to be useful for CMOS image sensors.

In this paper, a pixel signal readout operation that transfers a voltage of floating diffusion to column readout circuit, namely floating capacitor load readout operation is demonstrated for small, low power consumption and high S/N ratio CMOS image sensors. This operation utilizes a floating capacitor load instead of a constant current load as pixel SF driver, and the
parasitic capacitor of pixel output vertical signal line ($C_V$) as column sample/hold capacitor. In section 2, a working principle of the floating capacitor load readout operation is described. In section 3, two fabricated CMOS image sensors, their measurement results and effects of floating capacitor load readout operation on chip size, power consumption, readout noise, readout gain, pixel signal readout linear response range are shown. Conclusions are presented in section 4.

2. Working Principle of Floating Capacitor Load Readout Operation

2.1 Floating Capacitor Load with Pixel SF

Fig.1 shows the readout circuits of one column for (a) conventional readout operation and (b) floating capacitor load readout operation, respectively. In the conventional readout operation, when signal is read out, pixel SF drives the current, which value is determined by the $I_{pix}$ which becomes constant current at the end of readout; the pixel signal is read out to sample/hold capacitor by source follower operation. In this operation, even after the charging of the sample/hold capacitor is finished, there is a constant current from the power supply to the ground. On the other hand, in the floating capacitor load readout operation, pixel SF drives a $C_V$ which is pre-reset to a low voltage, instead of a constant current load. The pixel signal is readout by integrating the current in the capacitor. It was formerly utilized in bipolar imaging devices\(^{1,4,15}\). During readout, the drain current of pixel SF, which is determined by the gate-to-source voltage, is integrated in $C_V$, decreases drastically and approaches zero. Then, the voltage that is corresponding to the floating diffusion (FD) appears in $C_V$. There is only current for charging $C_V$ and unnecessary current is dissipated, therefore the power consumption for pixel signal readout becomes minimal. Additionally, since the output voltage is stored in $C_V$. The column circuit for sample/hold capacitor and current source are removed and the area of peripheral circuits becomes minimal.

In the floating capacitor load readout operation, the pixel current at the end of readout is determined by load capacitance and readout time. Fig.2 shows the readout timing for correlated double sampling (CDS) and temporal behaviors of output voltage and pixel current for conventional readout operation and floating capacitor load readout operation. Here, $\phi_T$, $\phi_R$, $\phi_X$, $\theta$VCLR drive transfer transistor, FD reset transistor, pixel select transistor (SEL), and switch for reset pixel output vertical signal line (VCLR), respectively. As shown in Fig.2, pixel current at the beginning of readout are different, that are corresponding to the FD voltage. $C_V$ capacitance is generally several pF and after a sufficiently long readout time of several µs (2 µs in this work), the pixel current at the end of readout are about 10 nA for all FD voltages. Pixel current at the end of readout are theoretically different for the FD voltage, however, the difference is quite small and negligible with comparison to total current that is integrated in $C_V$. Therefore, the linear response is achieved. Also, even if readout times for N signal and S+N signal are slightly different due to jitter, the effects to the noise performance and linearity are negligibly small because of the same reason.

In the floating capacitor load readout operation, since the current decreases as the readout time proceeds, the fluctuation of the current is integrated and averaged. Channel resistance of pixel SF increases as the readout time proceeds, the effective bandwidth becomes narrower. Also, the 1/f noise, which is known to induce a larger noise power in a larger current, is decreased. Due to these effects, the output noise becomes small. Furthermore, because the pixel signal is readout by the
form of voltage which is same as the conventional readout operation, the floating capacitor load readout operation can be used together with other high S/N ratio technologies\(^1\) such as column high gain amplifier, column ADC and CMS.

In the floating capacitor load readout operation, there are two possible issues that should be clarified and overcome if necessary. The first issue is the changing of signal voltage held in \(C_V\) which is attached to the column number of SEL, a VCLR and a switch for horizontal scan. Fig.3 shows equivalent circuit and cross-section view of pixels. The effect of leakage current of VCLR and a switch for horizontal scan are negligible because the number of these switch is one, respectively. However, as indicated by the arrow A in the cross-section view, the p–n junction reverse leakage current appears between the n + diffusion of SEL and p–well. The p–n junction reverse leakage current of one transistor is small. However, because SEL for the number of rows are connected to sample/hold capacitor \(C_V\), a considerable change of \(C_V\) voltage may occur. Here, the change of \(C_V\) voltage by p–n junction reverse leakage current is proportional to the holding time of pixel signal at \(C_V\). In addition, if some pixels are illuminated with strong light and a lot of electrons are generated in the neutral region under PD, then a part of generated electrons may not be collected by the n region of the PD and diffuse, and leak into the sample/hold capacitor \(C_V\) through n + diffusion of SEL, as indicated by the arrow B in the cross-section view. If this leakage of generated electrons occurs during the readout of a pixel signal or holding signal in \(C_V\), the leakage may affect whole signals of the column and a smear may occur. In conventional readout operation, because pixel signals are read out using current sources and held in analog memories connected to pixel output vertical signal line through switches, these issues are not the matters. Therefore, the time range of which p–n junction reverse leakage current does not affect the readout signal as well as, the operation condition that the smear does not occur should be clarified quantitatively for the floating capacitor load readout operation. The second issue is an increase on random telegraph noise (RTN) amplitude. RTN is caused by the capture/emission of an electron between channel and traps that exist in the insulator film. Although, the probability of RTN occurrence is low, their noise amplitude is larger than amplitude of 1/f noise and thermal noise. In CMOS image sensors, RTN occurs at pixel SF and induces a degradation of image quality. It has been also reported that the amplitude of RTN becomes larger with the decrease of drain current\(^1\)\(^7\)\(^8\). Therefore, it is expected that the floating capacitor load readout operation makes RTN larger because their drain current of pixel SF becomes some orders of magnitude smaller than that of conventional readout operation at the end of readout. For the first issue, we experimentally confirmed the conditions where the effects of signal voltage change in \(C_V\) are acceptable; for the second issue, we experimentally confirmed the impacts of RTN in the floating capacitor load readout operation in comparison to the conventional readout operation, and introduced the buried channel transistor to pixel SF transistors to reduce RTN\(^1\)\(^6\)–\(^2\)\(^1\). These results are described in section 3.

**2.2 Readout Gain and Linear Response Range of Floating Capacitor Load Readout Operation**

In conventional readout operation, about several 10µA is used for the constant current load. During the readout, if the output voltage is lower than the steady level, pixel SF drives large current from power supply and output voltage increases, and if the output voltage is higher than the steady level, the output voltage decreases by constant current of column current source. The value of column current is generally determined by the voltage swing and readout time in use, and it is usually several 10 µA.

Firstly, we evaluated the relationship between readout gain and pixel current by using a circuit simulation\(^2\)\(^2\). The simulations were carried out with transistor parameters and parasitic capacitance and resistance of the 2.8 µm pixel CMOS image sensor mentioned in section 3. A buried channel transistor pixel SF was implemented for reducing low frequency noise. The gate width and length were 0.34 µm and 0.60 µm, respectively. The gate length is relatively long to suppress the increase of RTN by short channel effect\(^2\)\(^3\). Fig.4 shows (a) equivalent circuits of pixel signal readout and (b) simulation results of readout gain as a
The conditions of the readout gain simulation are as follows; the resistance of current source ($R_L$) is from 1 MΩ to infinite with SEL and infinite $R_L$ without SEL. For the latter condition, the readout gain is determined by pixel SF transistor only. Here, the plotted readout gain is the averaged value in the range from $V_{IN} = 1.5$ V to $V_{IN} = 2.0$ V. Even when $R_L$ is sufficiently large, readout gain decreases by the effect of SEL when pixel current is larger than 1 µA. Therefore in conventional readout operation, if small current is used to avoid the degradation of readout gain by SEL, a longer readout time is necessary, i.e., there is a trade-off between readout gain and readout speed.

In the floating capacitor load readout operation, since $R_L$ approaches infinity because column current source is not used and pixel current is quite little at the end of readout time, the decrease of readout gain caused by SEL is suppressed. Therefore, near ideal readout gain depending only on pixel SF transistor is achieved. Furthermore, since the pixel current at the beginning of readout time is large and the output voltage rises rapidly, the trade-off between readout gain and readout speed is resolved. And in conventional readout operation, if wider transistor is used to achieve the degradation of readout gain by SEL as small as the floating capacitor load readout operation, a 6.8 µm of gate width is necessary. This size is too large to use in pixel.

The linear response range of pixel output voltage is an important factor for the full well capacity (FWC). Furthermore, linear response range becomes narrower and FWC becomes smaller when decreasing the power supply voltage. In conventional readout operation, column current source is necessary and the lower limit of linear response range is restricted by the voltage for driving column current source in the saturation region. Meanwhile, in floating capacitor load readout operation, since no current source is needed, the lower limits of linear response range become lower. Additionally, because the pixel current is some orders of magnitude smaller, the voltage drops in pixel SF and SEL of floating capacitor load readout operation is smaller than those of conventional readout operation. Therefore, the linear response range of floating capacitor load readout operation is considered to be wider than that of conventional readout operation. This effect was experimentally evaluated by the measurement results of fabricated chip and the results are described in section 3.
3. Fabricated Chips and Measurement Results

3.1 Fabricated Chips

We fabricated two CMOS image sensor chips with the floating capacitor load readout operation. One has 4.5 µm pixels and the other has 2.8 µm pixels. Fig.7 shows chip micrographs and block diagrams of (a) the 4.5 µm pixel CMOS image sensor and (b) the 2.8 µm pixel CMOS image sensor. These image sensors were fabricated using a 0.18 µm 1-Poly 3-Metal CMOS technology with pinned PD. The chip size and number of pixels of 4.5 µm and 2.8 µm pixel CMOS image sensors are 2.5 mmH x 2.5 mmV and 400H x 300V, 3.4 mmH x 2.5 mmV and 1140H x 768V, respectively. These image sensors use column SFs for larger readout gain from column by increasing chip height of only some rows. Both chips output analog signals.

Using the floating capacitor load readout operation, these image sensors removed column constant current sources and analog memories, which are necessary in conventional readout operation, and consist of only pixel array, vertical and horizontal shift registers, output buffers, column reset switches and column SFs. For measuring comparison data using conventional readout operation, the column reset switches were utilized as current sources. In the 4.5 µm pixel CMOS image sensor, the area of pixel array is 2.43 mm² and the area of peripheral circuits is 0.23 mm²; the ratio of pixel array to total area that is necessary for operation is 95.3 %. In the 2.8 µm pixel CMOS image sensor, the area of pixel array is 6.86 mm² and the area of peripheral circuits is 0.253 mm²; the ratio of pixel array to total area is 92.9 %. It is calculated that the area of peripheral circuits of conventional image sensors using the same process technology are 0.92 mm² and 2.80 mm² for 4.5 µm and 2.8 µm CMOS image sensors, respectively. By the introduction of floating capacitor load readout operation, the area of peripheral circuits decreases by 87.0 % and 81.2 % for the 4.5 µm and 2.8 µm pixel CMOS image sensors respectively, and the pixel array occupies almost all of the total area which is necessary for operation.

3.2 Measurement Results and Discussions

The measurement results of the fabricated chips are discussed. Fig.8 shows (a) the sample image and (b) photoelectric conversion characteristic obtained by the 4.5 µm pixel CMOS image sensor. The sample image was taken under the conditions that the F number of 1.4, exposure time of 0.8 msec, and signal holding time in CV of 20 µsec. This image sensor exhibited a 72 dB of dynamic range, 2.7 e⁻rms readout noise, 11 ke⁻ FWC and a 67 µV/e⁻ of conversion gain. It was confirmed that floating capacitor load readout operation has a good linearity to the light intensity.

We also measured the effect of p-n junction reverse leakage current on the signal hold at CV. We measured the change of CV voltage with varying the signal holding time after resetting voltage of CV. The initial voltage of the CV was reset to 2.1 V assuming the output of the dark pixel, where the reverse bias of p-n junction of SEL is the largest. The measurement temperature was 60 °C.

This is a sufficiently smaller value than the 1 LSB of 12 bit ADC used for this image sensor and it does not affect the input-output linearity.

We measured the effect of leakage of generated electron by a strong light on the signal hold in CV. Fig.9 shows the change of CV voltage as a function of the signal holding time. The change of CV voltage was proportional to the signal holding time in CV, and the slope was ~1.17 mV/msec. It was calculated that the change of CV voltage is ~23.4 µV for 20 µsec, which is the actual signal holding time in CV during image capturing.

This is a sufficiently smaller value than the 1 LSB of 12 bit ADC used for this image sensor and it does not affect the input-output linearity.

We also measured the effect of leakage of generated electron by a strong light on the signal hold in CV.

Fig.10 shows diagrammatic illustration of the
measurement method. Using a laser diode, we irradiated a bottom part of the pixel array, and we measured output signals of the upper row of the pixel array. This allows us to measure the effect of leakage of generated electron only. **Fig.11** shows signal voltage as a function of column number for (a) before CDS operation and (b) after CDS operation. The light intensity of laser diode is about $8 \times 10^5$ times higher than the intensity of saturation. In **Fig.11(a)**, variation of threshold voltage at pixel SF transistors and kTC reset noise appear. Also, the smear was observed near the column number of 280. And in **Fig.11(b)**, the effect of leakage of generated electron was not observed. Furthermore, when the light intensity of laser diode is lower than about $2 \times 10^5$ times of intensity of saturation, the effect of leakage of generated electron was buried in the variation of threshold voltage of pixel SF transistor and kTC reset noise of FD, and not observed in data even before CDS operation. In the floating capacitor load readout operation, since pixel SF amplifies the signals in the charge level by the ratio of $C_V$ to capacitance of FD, the tolerance to smear is higher than CCD image sensor. Also, because pixel signals are readout by form of voltage, CDS is used and eliminates the smear. Therefore, the effect of leakage of generated electron is little and even if it appears, it can be canceled by CDS operation with variation of threshold voltage of pixel SF transistor and kTC reset noise of FD.

Next, we describe the measurement results of dark random noise. **Fig.12** shows the distribution of dark random noise voltage of 60,000 pixels in the Gumbel plot. Black plots show conventional readout operation with surface channel transistor, red plots show floating capacitor load readout operation with surface channel transistor, and blue plots show floating capacitor load readout operation with buried channel transistor. Measurements were carried out with the 4.5 µm pixel CMOS image sensor. The frame period and the number of sampling were 24.6 msec and 1000. To compare the noise of pixels only, the plotted values were calculated by subtracting the random noise of the latter readout path assuming the noise sources in pixel and the latter parts of the readout path are independent. **Fig.13** shows temporal output behavior of the pixels at the cumulative probability of 50 % and 99.99 % of three measurements shown in **Fig.12**. The temporal output behavior of the pixels at the cumulative probability of 50 % is fairly constant. However, three discrete levels are found at pixels of cumulative probability of 99.99 % because of RTN after CDS. In **Fig.12**, comparing conventional readout operation with surface channel transistor and floating capacitor load readout operation with surface channel transistor, the noise level below the cumulative probability of about 90 % is smaller for the floating
capacitor load readout operation. It is considered to be due to the current integration effect. However, the other 10% of all pixels which have RTN as shown in Fig.13 show larger noise levels than the conventional readout operation. As expected, it is considered to be caused by the decrease of drain current. The noise voltage of floating capacitor load readout operation with buried channel transistor reduces the noise of pixels of which RTN is dominant noise source. It is confirmed that floating capacitor load readout operation is able to be used with buried channel transistor and the all pixels of cumulative probability achieved lower noise than conventional readout operation with surface channel transistor. The averaged values of dark random noise voltage of all pixels floating capacitor load readout operation with buried channel transistor and conventional readout operation with surface channel transistor were 168 µVrms and 466 µVrms, respectively; 63.8% reduction was achieved.

Next, we describe the measurement results of readout gain and linear response range comparing floating capacitor load readout operation and conventional readout operation under various power supply voltages. Fig.14 shows the pixel readout gain of floating capacitor load readout operation and conventional readout operation measured at various power supply voltages; (a) 3.3 V, (b) 2.5 V and (c) 2.0 V. The measurement was carried out with the 2.8 µm pixel CMOS image sensor and 15 µA was used for constant current with conventional readout operation as reference. The buried channel transistors are used for pixel SF transistors. To compare pixel readout gain and linear response range only, plotted readout gain is divided by the readout gain of latter signal readout path including non-linear range. In floating capacitor load readout operation, higher readout gain and wider linear response ranges than those of conventional readout operation were obtained in all measurement power supply voltages. When power supply voltage becomes lower, the linear response range becomes narrower in both readout operations. However, the amount of decrease in the floating capacitor load readout operation is smaller than that of conventional readout operation. Furthermore, although the readout gain of conventional readout operation decreases with decreasing power supply voltage, the readout gains of floating capacitor load readout operation are almost the same. Therefore, the floating capacitor load readout operation becomes more advantageous when decreasing the power supply voltage for lower power consumption. Fig.15 shows
power supply voltage dependency of (a) readout gain and (b) linear response range. Regarding the voltage range between lower and higher saturation levels of readout gain, the floating capacitor load readout operation has wider range than conventional readout operation. However, depend on the choice of permitted gain variation value to determine the range, conventional readout operation may result in having a wider range than that of the floating capacitor load readout operation. It is because in the floating capacitor load readout operation, gain value slight increases as input voltage increases. Although further investigation is needed both analytically and experimentally, we consider the reason of slight change is caused by the bias dependency of body effect of the pixel SF. And we also consider it can be reduced by the optimizing the well dopant concentration. Therefore, in this time, to compare the range between the voltages at which the readout gain drastically decreases, the linear response range was determined by a range of accuracy of less than 8 %. When power supply voltage was 2.0 V, the readout gain was increased by 7.7 %, and the linear response range was enlarged by 47.3 % by floating capacitor load readout operation in comparison to conventional readout operation. Furthermore since the floating capacitor load readout operation has linear response range extended lower pixel output voltage, this operation has a good match with lateral overflow integration capacitor technology\(^{16,27}\) of which full well capacity is not restricted by PD and enables PD pinned voltage to be decreased.

**Fig.15** Power supply voltage dependency of (a) readout gain and (b) linear response range.

readout operation become darker and their contrasts become lower, the images of floating capacitor load readout operation are same at various power supply voltages.

**Fig.17** shows comparison results of power consumption in pixel array of floating capacitor load readout operation and conventional readout operation with various power supply voltages. To compare the power consumption in pixel array only, the values were calculated using circuit simulation. The simulation of floating capacitor load readout operation was carried out with 2 µsec for N signal and N+S signal, respectively. The pixel voltage was set to the upper edge voltage of linear response range which consumes the largest power to read. The simulation of conventional readout operation was carried out with 15 µA pixel constant current, 3 pF of column sample/hold capacitors and 5 µs

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**Fig.16** Sample images captured at various power supply voltages.

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**Fig.17** Power consumption in pixel array of floating capacitor load readout operation and conventional readout operation with various power supply voltages.
of readout time, which contains 2 µsec for N signal readout time, 1 µsec for transfer charge time and 2 µsec for S+N signal readout time. And in both readout operations, the number of pixels was 1140H × 768V. The initial voltage of sample/hold capacitor was 0 V, the total time to drive a row which includes horizontal scan was 77.6 µsec, and frame period was 59.8 msec. When decreasing power supply voltage, the power consumption of conventional readout operation decreases in proportion to power supply voltage, on the other hand, the power consumption of floating capacitor load readout operation decreases further since pixel current becomes smaller by decreasing output voltage. When power supply voltage is 2.0 V, floating capacitor load readout operation achieved a 97.7 % reduction of power consumption in the pixel array.

The comparison results between floating capacitor load readout operation and conventional readout operation are summarized in Table 1. It was confirmed that the floating capacitor load readout operation has advantages in chip size, readout noise, readout gain, linear response range, and power consumption with comparison to the conventional readout operation.

### Table 1 Comparison results of floating capacitor load readout operation and conventional readout operation.

<table>
<thead>
<tr>
<th>Peripheral circuits area @ 2.8um pitch pixel, 1140 columns</th>
<th>Conventional readout operation</th>
<th>Floating capacitor load readout operation</th>
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<tr>
<td>Pixel signal readout time with 1140×768 pixels, 16bps, VDD=2.0V</td>
<td>3.6pW/frame-pixel 1.35V PWM CMOS Imager with Dynamic Pixel Readout and no Static Bias Current</td>
<td>0.16pW/frame-pixel 1.35V PWM CMOS Imager with Dynamic Pixel Readout and no Static Bias Current</td>
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4. Conclusion

In this paper, the operation principle and the effects of floating capacitor load readout operation for small, low power consumption, readout gain and linear response range were described. We confirmed that the floating capacitor load readout operation has advantages for small chip size, low power consumption and high S/N ratio with comparison to conventional readout operation by the measurement results of the fabricated two CMOS image sensor chips which use a 0.18 µm CMOS process with pinned PD and the ratio of pixel area to the total area that is necessary for operation is over 92 %. Using floating capacitor load readout operation, power consumption for pixel signal readout decreased by 97.7 %, and using with buried channel transistor, the readout noise of all pixels of cumulative probability decreased and the averaged value of all pixel reduced 63.8 %. Additionally, it has higher readout gain and wider linear response range than conventional readout operation. Furthermore, it becomes more advantageous when decreasing the power supply voltage. When the power supply voltage is 2.0 V, floating capacitor load readout operation increased readout gain by 7.7 %, enlarged linear response range by 47.3 %, respectively. Floating capacitor load readout operation enables CMOS image sensors to achieve small peripheral circuits, low power consumption and high S/N ratio.

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