A low voltage CMOS rectifier for low power battery-less devices

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Abstract: This paper presents a low voltage CMOS full-wave rectifier for transcutaneous power transmission in low power battery-less devices such as biomedical implants. By using a simple comparator-controlled switch which needs a small supply voltage, the lowest input voltage amplitude can be reduced to 0.7V with a standard CMOS 0.18μm process. With only one comparator, the proposed design dramatically reduces the power loss and the production cost. In combination with current offset which minimize the reverse current of the rectifier under different input amplitudes, the proposed rectifier can achieve a maximum peak voltage conversion efficiency of more than 93% and a power efficiency of approximately 87%.

Key Words: Low power battery-less devices, biomedical implant, low voltage, comparator-controlled switch.

1. Introduction

With the rapid development of microelectronics, high performance low power battery-less devices such as biomedical implant devices [1-4] play a more and more important role in modern medical treatments [5] such as measurement of internal blood pressure and monitoring of organs. These devices must be small in size to ease the implantation and be free of feedthrough wires to reduce the infection risk while increasing the portability such as a 4mm × 5mm system [1]. Batteries are not optional choice for implantable devices, because their lifetime is limited, and they are usually large and leaks can pose a hazard to tissues. In recent years, inductive coupling links is commonly used to deliver power and information to these implantable devices[6], [7]. Fig. 1 shows the block diagram of power transmission of biomedical implants. The inductive coil captures the signal from the reader with a carrier frequency of ranging from 200kHz to 1.5MHz for reducing energy loss during body penetration and not causing

Fig. 1. Schematic of a power transmission system of biomedical implants.
any danger to tissues [11]. The couple energy is then passed to the receiver circuit to generate a high AC voltage, followed by a rectifier to convert it into a DC voltage, while the regulator performs DC to DC conversion to provide stable supply voltage for the load system. In order to reduce power loss and enhance the efficiency, the power transmission used has to have sufficient power and data rate to be transmitted to the implant. The efficiency of the power transmission \( \eta_s \) is given as

\[
\eta_s = \eta_{\text{link}} \times \eta_{\text{rectifier}} \times \eta_{\text{regulator}},
\]

where \( \eta_{\text{link}}, \eta_{\text{rectifier}}, \eta_{\text{regulator}} \) are efficiencies of inductive coil, rectifier and regulator, respectively. Thus, the higher the rectifier efficiency \( \eta_{\text{rectifier}} \) is, the higher the overall system efficiency \( \eta_s \) of the power transmission can be achieved.

Conventional rectifiers are achieved by diodes and capacitors. The single-diode half-wave rectifier is simple and the full-wave rectifier with a diode bridge makes better use of the AC input and gives a smaller output ripple. They are commonly used in high voltage applications. However the diode forward voltage drop of 0.7V to 1V cannot be accepted in low voltage integrated systems. Schottky diodes with a low forward voltage drop can replace the common diode to improve the efficiency. However, the high production cost is a big problem. In CMOS-only implementation circuit, the diodes can be replaced by diode-connected MOS transistors. Low threshold voltage transistors can be used in advanced CMOS processes, requiring extra cost for additional masks and fabrication steps. In [8], two diodes of the diode bridge rectifier are replaced by two cross-coupled PMOS transistors. The gates of these PMOS transistors are driven by the input voltage. However, the other two diodes are still implemented by diode-connected NMOS transistors to block the reverse current, and the efficiency is not optimized for the voltage drop on the diode.

Recently, in order to achieve very high output voltage and high efficiency, an active diode [9] is used instead of the diode-connected PMOS and NMOS transistors in the conventional rectifier. The active diode works nearly as an ideal diode, with current flowing in only one direction and nearly no voltage drop. The active diode is composed of a comparator controlled MOS transistor, working as a switch. In [10] and [11], they use two active diodes to replace the diode-connected NMOS transistors in [8]. With active diodes instead of passive diodes, high output voltage and high efficiency can be achieved. Aiming at saving the chip area and making the circuit simpler, a rectifier with a negative voltage converter and just one active diode was proposed in [12]. However, there is a major bottleneck in the previous rectifiers. Firstly, for very low AC input voltage systems such as 0.7V, its rectification will not be feasible by using previous reported works. Secondly, even if rectification is feasible, the forward voltage drops and the reverse currents will cause a large amount of losses and make the power conversion very inefficient.

In this paper, a low voltage CMOS rectifier is proposed. In order to make the rectifier work with a small input voltage, a simple and low voltage active diode is developed to allow the rectifier to work with just 0.7V input which is far less than 1.2V[11]. Wide frequency range of operation makes the rectifier not only suited to biomedical implants but also vibration energy harvest systems [13].

This paper is organized as follows. In Section 2, the principle of a conventional negative voltage converter will be given. In Section 3, the principle of the operation of proposed low voltage rectifier is presented, including the low supply voltage active diode, the reverse current consideration and current offset. Simulation results are given in Section 4, followed by the conclusions in Section 5.

2. The principle of a negative voltage converter

Recently the negative voltage converter published in [12] is utilized to convert the negative half waves of the input sinusoidal wave into positive ones, which is done with two PMOS and two NMOS transistors shown in Fig. 2. During the positive half period of the input \((V_{in1} > V_{in2})\), MP1 and MN1 will be conductive when the input voltage increases and gets larger than \( |V_{thp}| \) and \( V_{thn} \). Thus, terminal 1 will be connected to the high potential and terminal 2 to the low potential. When the input wave is in the opposite half, MP2 and MN2 are conductive to connect terminal 1 to \( V_{in2} \) and terminal 2 to \( V_{in1} \). Therefore terminal 1 is always the high potential and terminal 2 the low potential.
Consequently, the bulk of the PMOS transistor can be directly connected to terminal 1 and the NMOS to terminal 2.

In this case, during each conductive branch, the voltage drop is only $|V_{dsp}| + V_{dsn}$, where $|V_{dsp}|$ and $V_{dsn}$ are the dropout voltages of PMOS transistors MP1/MP2 and NMOS transistors MN1/MN2, respectively. The dropout voltages $|V_{dsp}|$ and $|V_{dsn}|$ can be minimized by using large transistor size to decrease the resistance so as to get a small voltage drop. The simulation results show that the voltage drop in this stage can be less than 10 mV. Though the converter has nearly no voltage drop, it cannot control the current direction, therefore an active diode is necessary to block the reverse current.

3. Proposed low voltage rectifier

The main goals of this novel rectifier are the reduction of the input voltage amplitude and the achievement of a high efficiency. Fig. 3 shows the structure of the proposed rectifier. This rectifier can be divided into two stages: the negative voltage converter [12] and the simple low voltage active diode. The negative voltage converter has been described in Section 2.

3.1 Low operation voltage active diode

The main merit of this stage is to control the current direction and to work nearly as an ideal diode with only $|V_{dsp}|$ voltage drop and a low supply voltage as well. The proposed circuit includes a novel comparator controlled switch, making the structure simple and the minimum input voltage smaller. Fig. 4 II shows the circuit implementation of the proposed simple low voltage active diode. The output voltage $V_{con}$ of the converter serves as an input of the active diode. Transistors M4 - M9 work as a comparator to control the gate voltage of transistor M1. Transistors M10, M11, and M12 are two current mirrors to supply a small and stable current. In order to reduce the voltage drop, M1 is expected to turn on and turn off completely to prevent the reverse current. Set R1 a large resistance (in our design, $R1=40K\Omega$ is used), and then the currents through M10, M11, and M12 are very small. A small $I_D$ (the source to drain current) means $V_{GS} \approx V_{th}$, where $V_{GS}$ is gate to source voltage and $V_{th}$ is the threshold voltage. The gate voltage of M7 and M4 is around $V_{out} - |V_{th7}|$, where $|V_{th7}|$ is the threshold voltage of M7 and $V_{out}$ is the output voltage of the rectifier. Thus,
M4 turns on if $V_{con} > V_{out} - |V_{th7}| + |V_{th4}|$. Assuming that $|V_{th7}| = |V_{th4}| = |V_{th6}|$, when $V_{con} > V_{out}$, M4 turns on. Meanwhile, M5 turns off and the gate voltage of M9 is pulled high to connect the gate of M1 to the ground. Then M1 turns on to charge the capacitor C1. Similarly, M5 turns on if $V_{out} > V_{con} - |V_{th6}| + |V_{th5}|$, and the gate of M1 is connected to $V_{out}$ which is high potential. Thus, M1 turns off to prevent the reverse current from C1 to the input.

A dynamic bulk regulator is added to M1, connecting the substrate of M1, M4, M6 to the highest potential which prevents the parasitic vertical PNP transistors and avoids the chance for latch-up. Furthermore, the body effect on M1 is reduced and meanwhile reduces the rectifier’s dropout voltage and power dissipation.

3.2 Reverse current consideration and current offset

There will be reverse current from $V_{out}$ to $V_{con}$ if the switch M1 is still on when $V_{out} > V_{con}$ and reverse current can severely degrade the power efficiency of the rectifier. As shown in Fig. 5, when $V_{con}$ decreases and gets smaller than $V_{out}$, the gate voltage of M1 does not change to high potential until a delay time $\Delta T$. It means M1 is still on in the time interval $\Delta T$ and there will be reverse current, for $V_{out} > V_{con}$. In order to avoid the time delay $\Delta T$, we set the transistor sizes $W/L_{M12} > W/L_{M11}$, thus the current through the branch of M12 will be larger than that of M11 because of the current mirror. As in the saturation region, a larger $I_D$ makes the overdrive voltage of M6 larger than M7, which makes an offset voltage $V_{offset}$ in the comparator. Thus, the transistor switch turns off when $V_{out} \geq V_{con} + V_{offset}$, where the $V_{offset}$ is negative. This will compensate the $\Delta T$ and eliminate reverse current. When $V_{out}$ changes from 0.7V to 1.8V, the current through M11 and M12 will also

![Fig. 4. Circuit diagram of the proposed rectifier with (I) negative voltage converter, (II) low voltage active diode.](image)

![Fig. 5. Simulated waveforms of the delay time problem in the rectifier under $W/L_{M12} = W/L_{M11}$.](image)
increase which results in the value increasing of $|V_{offset}|$. Thus, we should adjust the ratio of $W/L_{M12}/W/L_{M11}$ to promise that there is no time delay with a 0.7V input. Figs. 6 and 7 show the performance under different input amplitudes. Additionally, taking into account the fabrication tolerances, we set the size of $W/L_{M12}$ a little larger than the required value to compensate this influence. Comparing Figs. 6 and 7 with Fig. 5, the rectifier has even no time to delay. It indicates that there is no reverse current. Therefore, higher power efficiency of the proposed rectifier can be maintained under different input amplitudes.

Moreover, the minimum input amplitude for the proposed rectifier is determined by the operation voltage of the comparator, since the comparator is supplied by the output dc voltage. Therefore, the rectifier output voltage should be larger than the minimum supply voltage requirement of the comparator, and a small operation voltage comparator is necessary.

As shown in Fig. 4 II, there are only one PMOS transistor and one NMOS transistor connected together in each path from $V_{out}$ or $V_{con}$ to the ground. Consequently, the minimum supply voltage of the comparator can be given as

$$V_{out_{min}} = \max(|V_{thp}| + V_{dsn} + V_{ov}, V_{thn} + |V_{dsp}|), \quad (2)$$

where the $V_{ov}$ is the over-dropout voltage of PMOS transistor. It means that the comparator can work well when both the voltages of $V_{con}$ and $V_{out}$ are larger than $V_{out_{min}}$, where $|V_{thp}|$ is threshold voltage of PMOS and the dropout voltage of NMOS transistor is assumed to $V_{dsn}$. Since there is also $|V_{dsp}| + V_{dsn}$ voltage drop through the first stage (negative converter), the minimum input voltage of the rectifier can be expressed as

Fig. 6. Simulated waveforms using current offset when $|V_{in}|_{peak} = 1.7V$.

Fig. 7. Simulated waveforms using current offset when $|V_{in}|_{peak} = 0.7V$. 
Table I. Circuit transistor sizes.

<table>
<thead>
<tr>
<th>Unit Size</th>
<th>Multiply Factor</th>
<th>Unit Size</th>
<th>Multiply Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP1 100μm/0.2μm</td>
<td>100</td>
<td>M5 40μm/0.5μm</td>
<td>50</td>
</tr>
<tr>
<td>MP2 100μm/0.2μm</td>
<td>100</td>
<td>M6 40μm/0.5μm</td>
<td>50</td>
</tr>
<tr>
<td>MN1 100μm/0.2μm</td>
<td>100</td>
<td>M7 40μm/0.5μm</td>
<td>50</td>
</tr>
<tr>
<td>MN2 100μm/0.2μm</td>
<td>100</td>
<td>M8 5μm/0.5μm</td>
<td>1</td>
</tr>
<tr>
<td>M1 100μm/0.2μm</td>
<td>50</td>
<td>M9 5μm/0.5μm</td>
<td>1</td>
</tr>
<tr>
<td>M2 100μm/0.2μm</td>
<td>50</td>
<td>M10 100μm/1μm</td>
<td>10</td>
</tr>
<tr>
<td>M3 100μm/0.2μm</td>
<td>50</td>
<td>M11 100μm/1μm</td>
<td>20</td>
</tr>
<tr>
<td>M4 40μm/0.5μm</td>
<td>50</td>
<td>M12 100μm/1μm</td>
<td>40</td>
</tr>
</tbody>
</table>

\[
V_{in_{min}} = V_{out_{min}} + |V_{dsp}| + V_{dsn},
\]

where \( |V_{dsp}| \) is dropout voltage of PMOS transistor.

4. Simulation results
The main aspects of the rectifier are minimum input voltage \( V_{in_{min}} \), output voltage efficiency, and the power efficiency, which will be discussed respectively.

The circuit has been simulated with HSPICE using a standard 0.18μm CMOS process table 1. A pure sinusoidal waveform whose frequency changes from 100KHz to 1.5MHz is applied to the input of

![Fig. 8. Simulated output voltage under 100KHz, 0.7V input with RL=500Ω.](image)

![Fig. 9. Simulated output voltage under 1.5MHz, 0.7V input with RL=500Ω.](image)
the rectifier. Additionally, a capacitance of $1\mu F$ and a load of $500\Omega$ are used. Besides, the performance of the proposed rectifier under low frequency from 20Hz to 100Hz which is suited for vibration energy harvesting systems [13] is also simulated.

4.1 Minimum input voltage and voltage conversion efficiency

The minimum input voltage is very important especially for some low supply voltage systems. Figs. 8 and 9 show the simulated output voltage. It indicates that the proposed rectifier can work at a minimum input voltage $|V_{in}|$ of 0.7V from 100K to 1.5MHz and provides a peak voltage conversion efficiency $V_{out}/|V_{in}|$ larger than 84%. Fig. 10 further explores the peak voltage conversion efficiency

![Graph of Voltage conversion efficiency](image1)

**Fig. 10.** Voltage conversion efficiencies of the proposed rectifier under different input amplitudes with a 1.5MHz input frequency.

![Graph of Voltage conversion efficiency](image2)

**Fig. 11.** Voltage conversion efficiencies of the proposed rectifier under different input amplitudes with a 100KHz input frequency.

![Graph of Power efficiency](image3)

**Fig. 12.** Power efficiencies of the proposed rectifier under different input frequencies.
of the proposed rectifier under different input amplitudes with a 1.5MHz input. The performance in 100KHz is shown in Fig. 11. Under both two frequencies, the peak voltage conversion rate is above 91% in average when $|V_{in}|$ is from 0.7V to 1.8V.

4.2 Power efficiency

The power efficiency of the rectifier is calculated using

$$E_{ff} = \frac{\int_0^T V_{out}(t)I_{out}(t)dt}{\int_0^T V_{in}(t)I_{in}(t)dt} \times 100\%,$$

where $T$ is one period. Fig. 12 shows the power efficiencies of the rectifier under different frequencies. It indicates that the power efficiency of the rectifier is higher at the lower input frequency of 100KHz. This is due to the fact that the transistor switches of the negative voltage converter and of the comparator-controlled switch work as almost ideal switches. And high efficiency will result more power loss in these switches, especially of the negative voltage converter since its large transistor scales. The power efficiency of the proposed rectifier can achieve at least 81% under different frequency references less than or equal to 1.5MHz.

4.3 Performance in different process corners

The proposed rectifier has been simulated when the process corners are the typical (TT), fast (FF) and slow (SS) of the 0.18μm CMOS technology, respectively. The fluctuation of the voltage conversion rate is about ±3% between different process corners which can be accepted.

![Fig. 13. Voltage conversion efficiencies of the proposed rectifier under low input frequencies with RL=500Ω.](image)

![Fig. 14. Power efficiencies of the proposed rectifier under low input frequencies with RL=500Ω.](image)
4.4 Performance in low frequency
Simulation results have shown that the proposed rectifier can work well in the frequency range from 100KHz to 1.5MHz. Besides biomedical implants devices, rectifiers are also used in some vibration energy harvesting systems to convert an AC power to DC ones. The output of vibration generator such as piezoelectric generator is usually under 100Hz. In order to verify our design, we also simulate the proposed rectifier in low frequencies from 20Hz to 100Hz. Figs. 13 and 14 show that this circuit can work even better in low frequency. Thus, it can be used in some vibration energy harvesting systems as well.

4.5 Performance comparisons
Table 2 shows the performance comparisons of the work with other previously reported rectifiers. With even the same power efficiency, peak voltage conversion efficiency and range of frequency, the proposed rectifier can operate at a 0.7V input amplitude which is far smaller than the minimum input voltage proposed in [11]. Moreover, the proposed circuit can also work in low frequency.

5. Conclusions
A low voltage CMOS rectifier for low power battery-less devices is presented. The rectifier is well suited for an input amplitude as low as 0.7V by using a simple low supply voltage active diode. Additionally, by a small offset added in the comparator, the reverse current problem is removed, which is important for reducing the voltage drop and improving the power efficiency. The proposed rectifier can achieve a maximum peak voltage conversion efficiency of more than 93% and a power efficiency of approximately 87%. Moreover, it can work better under low frequency input and can work stably in different corner models.

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