

Paper

Transient thermal network model identification for power module packages

Shuhei Fukunaga^{1a)} and Tsuyoshi Funaki¹

¹ *Osaka Univ., Div. of Electrical, Electronic and Information Eng., Graduate school of Eng., Suita, Osaka 565-0781, Japan*

^{a)} *fukunaga@ps.eei.eng.osaka-u.ac.jp*

Received July 10, 2019; Revised October 29, 2019; Published April 1, 2020

Abstract: Transient thermal characterization of power modules plays an important role in designing power conversion systems for miniaturization. Transient thermal network model of power module packages is identified by deconvolution calculation for the time response of junction temperature in power semiconductor devices, which is obtained by static test method. This paper develops a signal processing algorithm using weighted discrete Fourier transformation and noise filtering in frequency domain for nonuniform time step data in the converted logarithmic time domain to apply deconvolution calculation. The developed algorithm suppresses the influence of noise superimposed on the measured signal and enables the accurate identification of transient thermal network model.

Key Words: power module, transient thermal network model, static test method, deconvolution, Fourier transformation

1. Introduction

Miniaturization of power conversion systems is expected especially in motor drive applications, such as electrical vehicles (EVs) and railways. Fast switching operation of wide bandgap (WBG) power semiconductor devices, which is superior to conventional high voltage silicon (Si) power semiconductor devices, enables to miniaturize devices and passive components in power conversion systems [1–5]. However, miniaturization increases heat dissipation per unit area/volume and makes thermal management difficult. Therefore, thermal design is a key factor for miniaturization of power conversion systems to maximize WBG power semiconductor device capability.

Thermal design of power modules aims at spreading and transferring heat dissipated in power semiconductor devices. Heat spreading and transferring mainly depends on structure and material property of power module constitutions. The conventional static thermal resistance model evaluates the temperature difference between junction to case of power modules in steady-state operation. However, a transient thermal network model represented by thermal resistance and thermal capacitance is needed to estimate the time response of junction temperature (T_J) in over or fault current condition [6–16]. References [9] and [10] assessed the dynamic thermal coupling effect for multi-chip power module packages. References [11–15] identified a transient thermal network model in the frequency domain using Fourier series expansion. Frequency domain modeling is also conducted for several thermal circuit models in [16]. Static test method [17] is the standard method for identifying the transient

thermal network model of power module packages. This method estimates T_J by the temperature dependency in $I - V$ characteristics of power semiconductor devices in power modules.

Reference [17] performs some numerical calculations such as deconvolution calculation to identify the transient thermal network model from the time response of T_J in cooling operation from thermal equilibrium in self heated condition. The precise numerical calculation procedure to identify the transient thermal network model is not clearly addressed in [17], and the conventional model identification algorithm has difficulty in eliminating the influence of noise in the measured signal. An additional filtering or another signal processing algorithm is necessary in order to achieve higher noise reduction capability for estimating the accurate time response of T_J from the obtained transient thermal network model. This paper develops an algorithm that uses weighted discrete Fourier transformation and noise filtering in frequency domain, which supersedes the conventional algorithm used in static test method. The influence of quantization error and noise in the measured signal is evaluated for the simulated time response of T_J with a given transient thermal network model. The accuracy of the identified transient thermal network model for a discrete power device and module package is experimentally evaluated.

2. Transient thermal network model of power module packages

This chapter summarizes the theory and the measurement setup of static test method. For more details on the method, the reader refers [17] and related references.

2.1 Structure function related to transient thermal networks

The typical structure of power module package with direct bonded copper (DBC) substrate is illustrated in Fig. 1a). The heat dissipated in junction of power semiconductor device approximately flows to heat sink through each layer of power module packages in one direction. The thermal equivalent circuit is modeled by the cascade connected pairs of thermal resistance and thermal capacitance as Cauer thermal network illustrated in Fig. 1b), by assuming that each layer of the power module package is uniform and heat spreading in the horizontal axis is integrated. The Protonotarius-Wing function [18], or structure function [19], represents the cumulative thermal capacitance as a function of the cumulative thermal resistance as illustrated in Fig. 1c). In other words, structure function

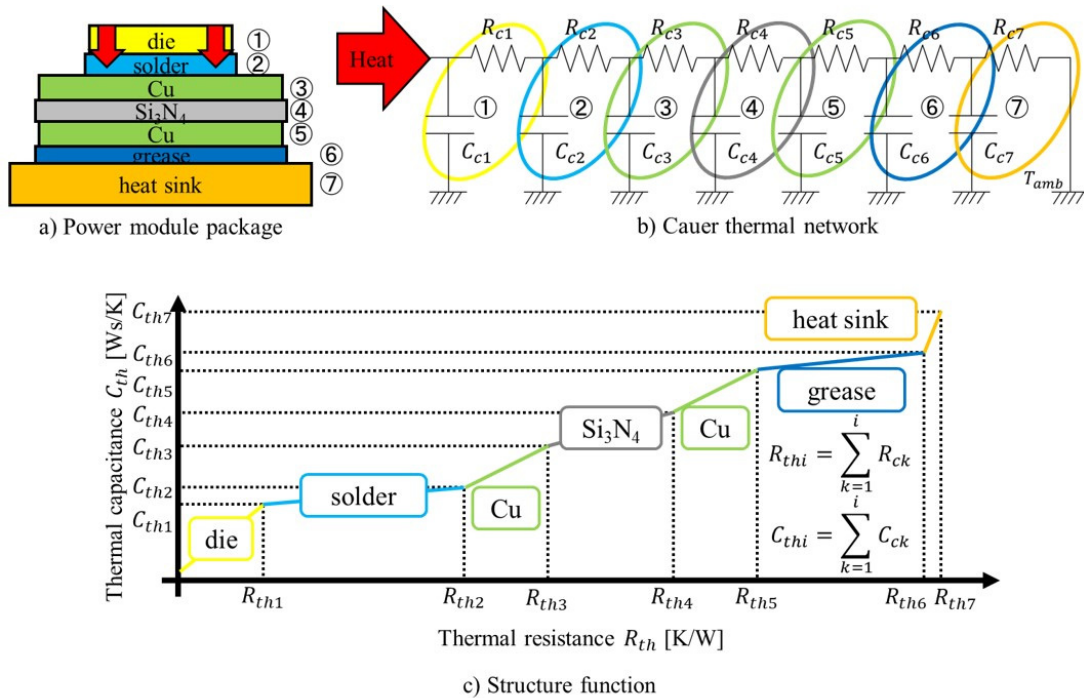


Fig. 1. Structure function related to actual power module package.

related to Cauer thermal network represents the transient thermal behavior of respective components in the power module.

Generally, the thermal impedance of an n th order Cauer thermal network $Z_{cauer}(s)$ in Laplace (s -)domain is given by the following equation with the parameters in Fig. 2a):

$$Z_{cauer}(s) = \frac{1}{sC_{c1} + \frac{1}{R_{c1} + \frac{1}{sC_{c2} + \frac{1}{R_{c2} + \cdots + \frac{1}{sC_{c(n-1)} + \frac{1}{R_{c(n-1)} + \frac{1}{sC_{cn} + \frac{1}{R_{cn}}}}}}}}}. \quad (1)$$

Although Cauer thermal network corresponds to the actual physical parameter and structure of power module packages, but parameter extraction directly from the measured time response of T_J is difficult. We therefore consider the numerical equivalent transient thermal network model illustrated in Fig. 2b). This network is known as Foster thermal network, and its parameters do not have physical correspondence to the model structure. The thermal impedance of an n th order Foster thermal network $Z_{foster}(s)$ in s -domain is given by the summation of fractional impedances with the parameters in Fig. 2b):

$$Z_{foster}(s) = \frac{R_{f1}}{1 + sR_{f1}C_{f1}} + \frac{R_{f2}}{1 + sR_{f2}C_{f2}} + \cdots + \frac{R_{fn}}{1 + sR_{fn}C_{fn}} = \sum_{i=1}^n \frac{R_{fi}}{1 + sR_{fi}C_{fi}}. \quad (2)$$

By converting Eq. (2) from s -domain to time domain, the time response of junction temperature $T_J(t)$ for ΔP_H power dissipation is calculated by the following equation:

$$T_J(t) = \Delta P_H \sum_{i=1}^n R_{fi} [1 - \exp(-t/\tau_{fi})]. \quad (3)$$

where, $\tau_{fi} = R_{fi}C_{fi}$ is the thermal time constant. This equation means that the time response of T_J , which is obtained experimentally from power semiconductor devices in power modules, is represented by the summation of exponential functions. Moreover, the desired Cauer thermal network is obtained from Foster thermal network by numerical equivalent transformation.

2.2 Foster thermal network model identification by deconvolution

The time response of T_J is experimentally obtained using static test method. The measurement procedure is summarized as follows, and illustrated in Fig. 3a). First, device under test (DUT) is attached on the temperature-controlled coldplate. A large current, which is sufficient to achieve self-heating, is forced to flow through DUT until it reaches thermal equilibrium condition. The heating current then shunts off and the time response of T_J in cooling operation is measured. T_J is obtained from the measured voltage drop to a small constant current, whose self-heating effect is negligible, and the temperature dependency in $I - V$ characteristics of power semiconductor devices. The measured time response of junction voltage (V_J) is converted to the time response of T_J using

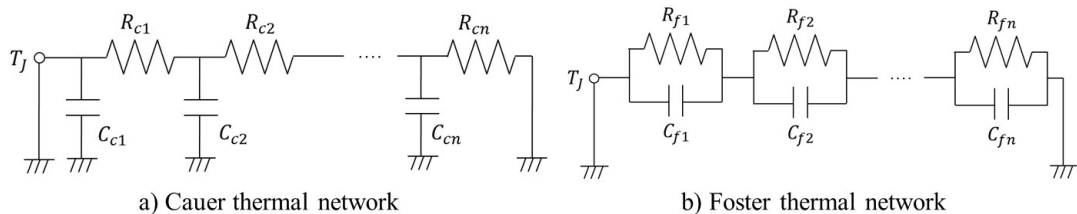


Fig. 2. Transient thermal network models.

temperature sensitive electrical parameter (TSEP) known as K factor. K factor is the relationship between the V_J and the temperature for a specified current, and experimentally obtained by electrical test method [20]. Figure 3b) shows the example of K factor for SiC Schottky barrier diode (SBD) C4D20120A (1200V/20A, CREE, TO-220 package) and S6305 (1200V/50A, ROHM, mounted on ceramic substrate).

Table I. The conventional algorithm for identifying transient thermal network model.

Step	Domain	Procedure
1	Time (t)	Measure the time response of V_J in the cooling operation
2	Time (t)	Convert $V_J(t)$ to $T_J(t)$ using K factor and divide it by the input power ΔP_H
3	Time (t)	$T_J(0)$ estimation by extrapolating [21]
4	Time (t)	Convert $a(t)$ from the linear time domain to the logarithmic time domain
5	Time (t)	Remove the noise with moving average filter and resample
6	Time (z)	Differentiate $a(z)$ with z to obtain $\frac{d}{dz}a(z)$
7	Time (z)	Calculate $w_z(z)$
8	Frequency	FFT of $\frac{d}{dz}a(z)$ and $w_z(z)$
9	Frequency	Deconvolution calculation
10	Time (z)	Obtain TCS by IFFT using the filter function with Fermi-Dirac function [17]
11	Time (z)	Determine Foster thermal network model from TCS
12	Time (z)	Determine Cauer thermal network model by Foster-Cauer transformation

Cauer thermal network model is identified from the measured time response of T_J using the procedure listed in Table I. In this paper, this procedure is referred as the conventional algorithm, which is implemented in the analysis software T3SterMaster (Mentor Graphics). Equation (3) is rewritten as the transfer function $a(t)$ for the unit power step input:

$$a(t) = \frac{T_J(t)}{\Delta P_H} = \sum_{i=1}^n R_{fi}[1 - \exp(-t/\tau_{fi})]. \quad (4)$$

$a(t)$ is transformed to $a(z)$ by introducing the logarithmic time scale $z = \ln t$, and $\zeta = \ln \tau$. Thermal time constant spectrum or TCS, $R(z)$, is given as the following equation with the deconvolution integral \otimes^{-1} :

$$R(z) = \frac{d}{dz}a(z) \otimes^{-1} w(z). \quad (5)$$

where, $w(z) = \exp(z - \exp(z))$ is the given weight function. The obtained Foster thermal network

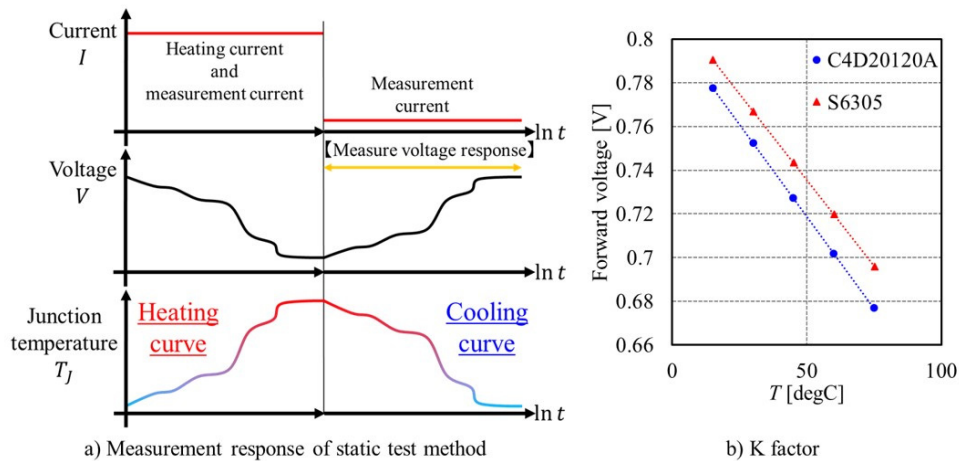


Fig. 3. Static test method.

model from TCS by deconvolution can be transformed to Cauer thermal network model by Foster-Cauer transformation.

3. Signal processing algorithm in logarithmic time domain

Table II shows the signal processing algorithm developed in this paper to identify Cauer thermal network model, and the difference in procedure from Table I is specified by bold number. The conventional algorithm eliminates noise in the measured signal using a moving average filter in the linear time domain. However, the moving average filter cannot fully eliminate the measurement noise, and the residual noise is emphasized in numerical differentiation of $a(z)$, which degrades the accuracy of the identified transient thermal network model. The developed algorithm adopts weighted discrete Fourier transformation and noise filtering in logarithmic frequency domain to suppress the influence of measurement noise. The details of each calculation is discussed in this chapter.

Table II. The developed algorithm for identifying transient thermal network model.

Step	Domain	Procedure
1	Time (t)	Measure the time response of V_J in the cooling operation
2	Time (t)	Convert $V_J(t)$ to $T_J(t)$ using K factor and divide it by the input power ΔP_H
3	Time (t)	$T_J(0)$ estimation by extrapolating [21]
4	Time (t)	Convert $a(t)$ from the linear time domain to the logarithmic time domain
5	Time (z)	Differentiate $a(z)$ with z to obtain $\frac{d}{dz}a(z)$
6	Frequency	Weighted DFT of $\frac{d}{dz}a(z)$
7	Frequency	Noise reduction with Fermi-Dirac function
8	Time (z)	IDFT for the filtered frequency response
9	Time (z)	Bayesian deconvolution to obtain TCS
10	Time (z)	Determine Foster thermal network model from TCS
11	Time (z)	Determine Cauer thermal network model by Foster-Cauer transformation

3.1 Transformation of time domain from linear to logarithmic

The phenomenon of heat transfer progresses exponentially in time, and transient thermal network model identification is processed in the logarithmic time domain as shown in Tables I and II. The measurement of V_J time response is sampled with uniform time step Δt in the linear time domain, and thus the converted data to the logarithmic time domain has nonuniform time step as illustrated in Fig. 4. This time step in the logarithmic time domain becomes small as time progresses. This leads to the excess samples in the logarithmic time domain and increases computational time in identifying the transient thermal network model. Decimation in the logarithmic time domain is required to reduce the number of data in the identification process. This paper decimates the measured data using uniform time step in the linear time domain by halving sampling frequency in the linear time domain, when the following condition is satisfied:

$$\frac{|z_{i+1} - z_i|}{z_1 - z_0} \leq \frac{1}{2Z}. \quad (6)$$

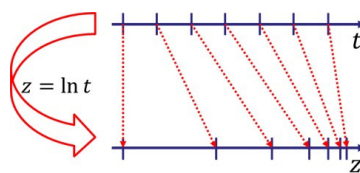


Fig. 4. Transformation of sampling point from the uniform time step in linear time domain to logarithmic time domain.

where z_i for $0 \leq i \leq N_{lin} - 1$ is the discretized logarithmic time converted from the linear time t_i . Z is a coefficient determined by users, and $z_0 > 0$ is the first time point of measurement. For example, the sampling frequency is halved to 500kHz, 250kHz, 125kHz, ..., for the initial sampling frequency of 1MHz, which reduces the number of data for identification to N ($N < N_{lin}$). Z is determined in terms of time resolution based on the time constant of interest. For example, 100000 numbers of 1sec data by 100kHz sampling reduces 1500 after decimation in $Z = 100$. The calculation time of the developed algorithm without and with decimation is 1344.21s and 1.13s, respectively for Core i7-8700K and DDR4-32GB memory system.

Though the conventional algorithm also adopts this method, but the decimated measured time response of T_J is filtered by the moving average filter, and then resampled to the uniform logarithmic time step. The noise elimination with the moving average filter to the decimated data is ineffective, and thus this filtering method in the conventional algorithm seems to occur large residual noise.

3.2 Noise reduction using weighted discrete Fourier transformation

Fourier transformation of a given function $x(z)$, and its inverse Fourier transformation are given by the following equations:

$$X(\Phi) = \int_{-\infty}^{\infty} x(z) e^{-j2\pi\Phi z} dz, \quad (7)$$

$$x(z) = \frac{1}{2\pi} \int_{-\infty}^{\infty} X(\Phi) e^{j2\pi\Phi z} d\Phi. \quad (8)$$

where, $j^2 = -1$. It should be noted that Φ denotes logarithmic frequency, which corresponds with logarithmic time domain z . We assume that $x(z)$ is the periodic function for $z = a$ to $z = b$, and discretizes in the nonuniform time step for the total number of data N . In this time, the fundamental frequency Φ_0 and Nyquist frequency Φ_c in the logarithmic frequency domain are given as follows:

$$\Phi_0 = \frac{1}{\Delta z_{max}}, \quad (9)$$

$$\Phi_c = \frac{1}{2\Delta z_{max}}. \quad (10)$$

where, $\Delta z_{max} = \max\{z_{i+1} - z_i\}$ for $0 \leq i \leq N - 1$ after decimation. Equation (7) is discretized as follows with $\Phi_k = k\Phi_0$:

$$X(\Phi_k) = \int_a^b x(z) e^{-j2\pi \left(\frac{k}{z_{N-1} - z_0} \right) z} dz. \quad (11)$$

Then, $X(\Phi_k)$ is rewritten by adopting the trapezoidal formula for Eq. (11):

$$X(\Phi_k) \simeq \sum_{n=0}^{N-2} \left(x_{n+1} e^{-j2\pi \frac{k}{z_{N-1} - z_0} (z_{n+1} - z_0)} + x_n e^{-j2\pi \frac{k}{z_{N-1} - z_0} (z_n - z_0)} \right) \frac{(z_{n+1} - z_n)}{2}. \quad (12)$$

Equation (12) is taken as weighted discrete Fourier transformation. In order to suppress the influence of noise in the measured signal, a low-pass filter is adopted in the frequency domain. In practice, Fermi-Dirac function F_{fd} [17] is used as the low-pass filter.

$$F_{fd}(\Phi_k) = \left[\exp \left(\frac{|\Phi_k| - \Phi_0}{\sigma} \right) \right]^{-1} \quad (13)$$

The shape of Fermi-Dirac function is determined by two parameters: the bandwidth Φ_0 and the edge steepness σ . The parameter is adjusted for the best compromise between resolution and noise enhancement. $\Phi_0 = 0.45$ and $\sigma = 0.05$ are good values as given in [17].

Inverse discrete Fourier transformation (IDFT) is processed for the noise eliminated signal for deconvolution calculation in the logarithmic time domain. The nonuniform time step of the measured

signal in the logarithmic time domain is transformed to the uniform time step by IDFT, i.e. the resynthesised signal is resampled. The conventional algorithm sets the output data to become 20 point samples per octave.

3.3 Bayesian deconvolution

Practical deconvolution algorithms have been applied for transient thermal characterization of power modules, such as Bayesian deconvolution [22, 23] and Fourier domain inverse filtering [24]. This paper performs Bayesian deconvolution for the low-pass filtered signal in logarithmic time domain.

$$R_i^{(m+1)} = R_i^{(m)} \sum_k \frac{w_{ki} \left(\frac{da}{dz} \Big|_i \right)}{\sum_j w_{kj} R_i^{(m)}} \quad (14)$$

where, R_i is the discretized TCS, $R_i^{(m)}$ is the estimated R_i after m iterations, and $w_{ki} = \exp(z_k - z_i - \exp(z_k - z_i))$. Convolution and correlation sums in Eq. (14) have to be recalculated for each iteration step. The iteration number m is estimated to be sufficient to the order of 1000 in [22].

4. Improvement of accuracy for the identified transient thermal network model using the developed algorithm

The developed algorithm is validated using an ideal time response of T_J shown in Fig. 5. This time response is numerically calculated from Eq. (3) for Foster thermal network model parameters, which is obtained by Causer-Foster transformation from the parameters listed in Table III. The evaluation is processed for a 1MHz sampling frequency, and a decimation coefficient $Z = 100$. The developed algorithm is programmed with C including GNU Multiple Precision Arithmetic Library (GMP).

Table III. Causer thermal network model parameters.

n	R_{ci}	C_{ci}	τ_{ci}
1	0.01	0.01	0.0001
2	0.02	0.05	0.001
3	0.05	0.20	0.01

The TCSs of $da(z)/dz$ in Fig. 5 are shown in Fig. 6. The number of Bayesian iteration m is 1000. The developed algorithm adopts $\Phi_0 = 0.45$ and $\sigma = 0.05$, while it is not disclosed for T3SterMaster. The blue solid and the red dotted lines in Fig. 6 are calculated by T3SterMaster and the developed algorithm, respectively. The black dot denotes the given Foster thermal network model parameter in Table III. The TCS calculated using the conventional and the developed algorithm coincides with the given time constant.

4.1 Quantization error

The sampling frequency and the bit length of A/D converter (ADC) in the discretization and the quantization of the measured data affects resolution and accuracy of the calculated transient thermal

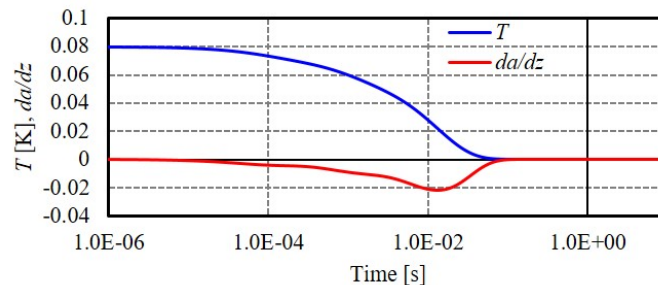


Fig. 5. Ideal time response of T_J .

network model. Generally, SNR of the quantization error to an ideal sinusoidal wave for full-scale input N_{bit} bit ADC is given as follow [26, 27]:

$$SNR[\text{dB}] = 6.02N_{bit} + 1.76 \quad (15)$$

From Eq. (15), for example, the SNR of a 12bit ADC is 74dB. Over sampling is the general method for suppressing the quantization error for the same bit length ADC [26–29]. The improved SNR for oversampled signal ratio (OSR) is redefined after low-pass filtering and decimation as given by Eq. (16) [26].

$$SNR[\text{dB}] = 6.02N_{bit} + 1.76 + 10 \log_{10}(OSR) \quad (16)$$

The power spectra of $da(z)/dz$ in Fig. 5 is shown in Fig. 7. Here, k is the order to the fundamental frequency, and the amplitude is normalized for $k = 0$. The bit length of ADC for full-scale input is given as the parameter for evaluating the influence of the quantization error, which appears as the difference in amplitude of power spectrum. This result shows that the longer bit length gives the lower floor noise level, and the amplitude of power spectrum coincides with the result calculated from Eq. (16). The power spectra larger than 10 bit are in agreement with its ideal spectra in full-scale input ADC. In actual measurement environment, the effective bit length of ADC for the input signal should be considered because this result assumes the full-scale input.

The power spectrum of $da(z)/dz$ in Fig. 5 is calculated as shown in Fig. 8. Sampling frequency and decimation coefficient Z are given as the parameters for 12bit full-scale input ADC in Fig. 8a) and b), respectively. Figure 8a) shows that higher sampling frequency gives lower floor noise level by suppressing the quantization error due to oversampling, which coincides with the value calculated by Eq. (16). It is noted that the number of the measured data becomes large for high sampling frequency. Figure 8b) reveals that Z does not influence on the power spectrum of $da(z)/dz$, and Z can be chosen as small as possible unless the resolution of TCS after decimation does not degrade.

4.2 Evaluation of robustness for the noise superimposed on the ideal signal

Figure 9 is the power spectra of $da(z)/dz$ with white noise superimposed on the ideal signal in Fig. 5. The quantization is not considered in this section. The amplitude of noise superimposed on the ideal

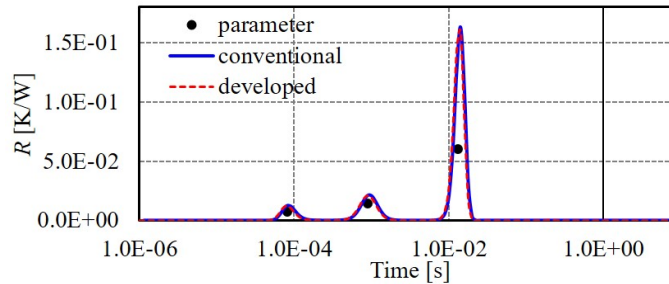


Fig. 6. TCS calculated from Fig. 5.

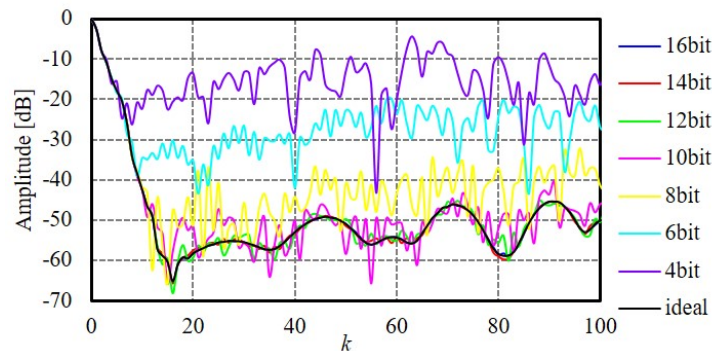


Fig. 7. Power spectra of the da/dz for the bit length of ADC (1MHz, $Z = 100$).

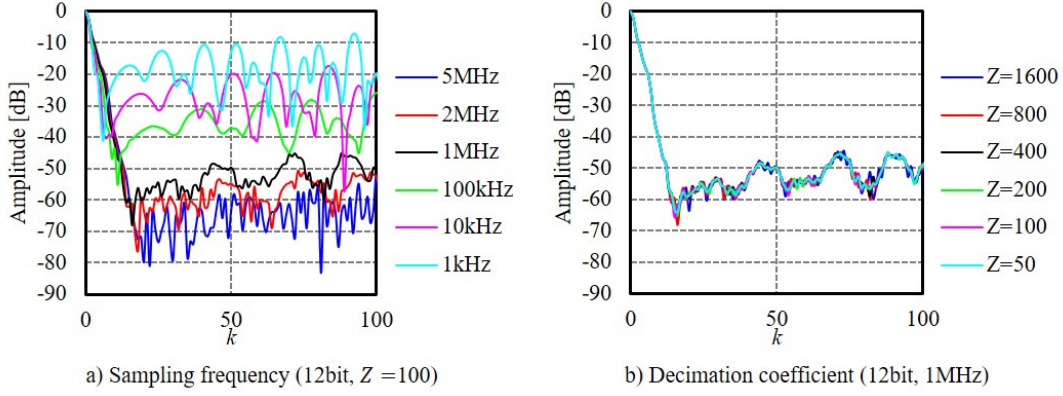


Fig. 8. Power spectrum of $da(z)/dz$ for the *OSR* (12bit).

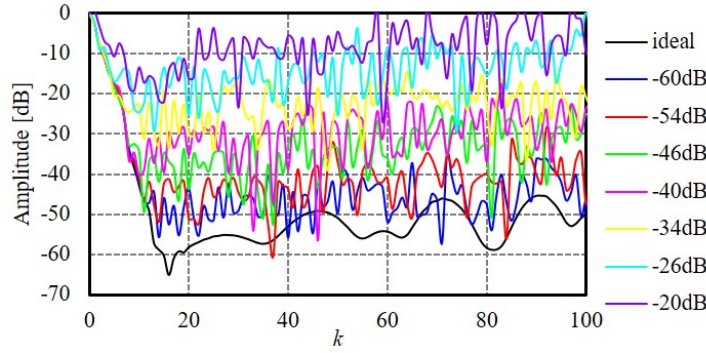


Fig. 9. Power spectrum of $da(z)/dz$ for white noise (1MHz, $Z = 100$).

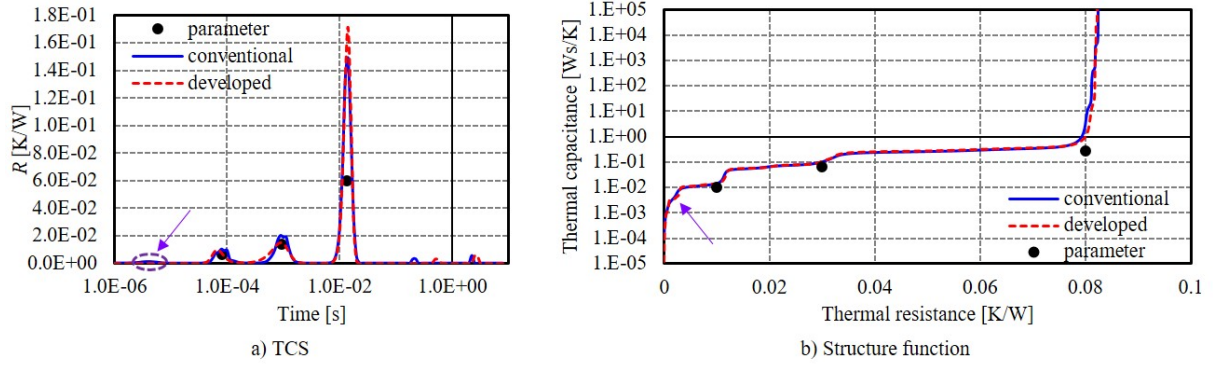


Fig. 10. TCS of da/dz for $\text{SNR} = -40\text{dB}$ and the structure function (1MHz, $Z = 100$).

signal is the parameter referred to as SNR for evaluating the effect of noise elimination using the developed algorithm. The amplitude of white noise clearly increases floor noise level in the power spectrum of $da(z)/dz$ as shown in Fig. 9.

The obtained TCS of $da(z)/dz$ with 40dB white noise superposition and its structure function is shown in Fig. 10. The conventional algorithm gives unintended peaks on TCS in small time constant as indicated by arrows in Fig. 10a), which is not in the given model parameter and makes the step shape of structure function obscure. The residual noise at large time constant appears as the undesired peak for both algorithm. The amplitude of the intended peak calculated by the developed algorithm is higher than by the conventional algorithm. This enables to clearly extract the transient thermal model parameters from structure function. The structure function calculated by the conventional and the developed algorithm in Fig. 10b) coincides with the given model parameter in Table III.

Table IV shows the root mean square (RMS) error of $da(z)/dz$ from the ideal $da(z)/dz$ for each

algorithm. The developed algorithm can suppress the influence of white noise, and improve the accuracy of obtained TCS and identified transient thermal network model.

4.3 Experimental validation for discrete power device and power module package

Transient thermal network model of discrete power device and power module package is experimentally identified with the conventional and the developed algorithm. Discrete power device package does not have insulation and bottom copper layer shown in Fig. 1a). Discrete package requires the external insulation material in power conversion system to attach heat sink, which has large thermal resistance. DBC substrate has high critical electric field and high thermal conductivity, and is often used for high density power module. The studied power module package with SiC SBD S6305 is attached on SiN power module substrate shown in Fig. 1a) by Pb free solder and Al wired with ϕ 300 μm .

The time response of estimated T_J for discrete SiC SBD C4D20120A (TO-247) and the studied power module is experimentally obtained by static test method using T3Ster (Mentor Graphics) with 12bit ADC at 1MHz sampling frequency as shown in Fig. 11. The time response of measured V_J for Fig. 11a) and b) in cooling operation is obtained to a small 10mA and 100mA constant current after self heated thermal equilibrium condition with a 15A and 20A heating current, respectively. T_J in Fig. 11 is estimated using the K factor in Fig. 3b). These packages are attached on a 20 °C coldplate with 10cN/m screw torque.

Figures 12 and 13 shows the calculated $da(z)/dz$ for the filtered measured signal to Fig. 11 and

Table IV. RMS error for $da(z)/dz$.

SNR	developed	conventional
-60dB	5.02×10^{-5}	2.24×10^{-4}
-46dB	2.40×10^{-4}	5.93×10^{-4}
-40dB	3.39×10^{-4}	1.08×10^{-3}
-26dB	8.02×10^{-3}	1.01×10^{-2}

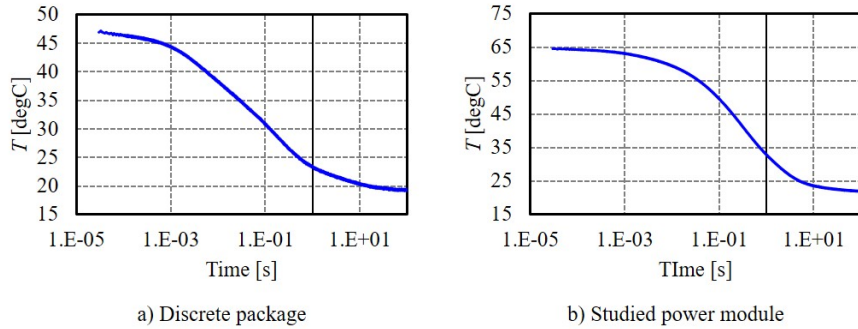


Fig. 11. The time response of estimated T_J .

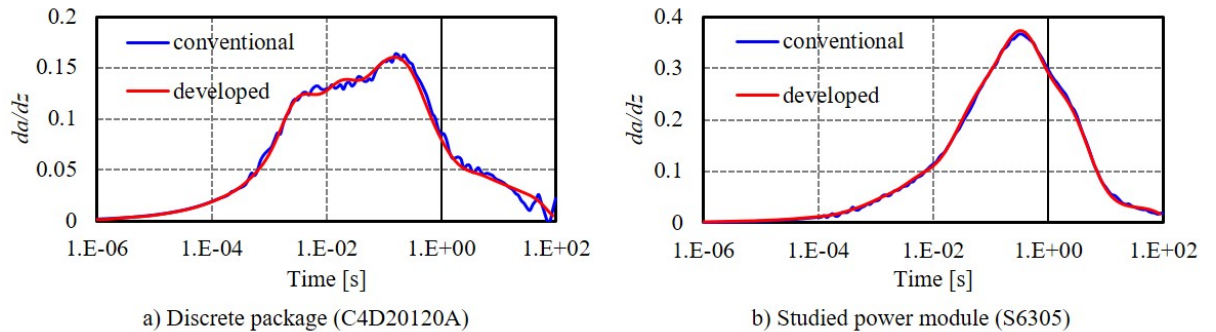


Fig. 12. The time response of da/dz .

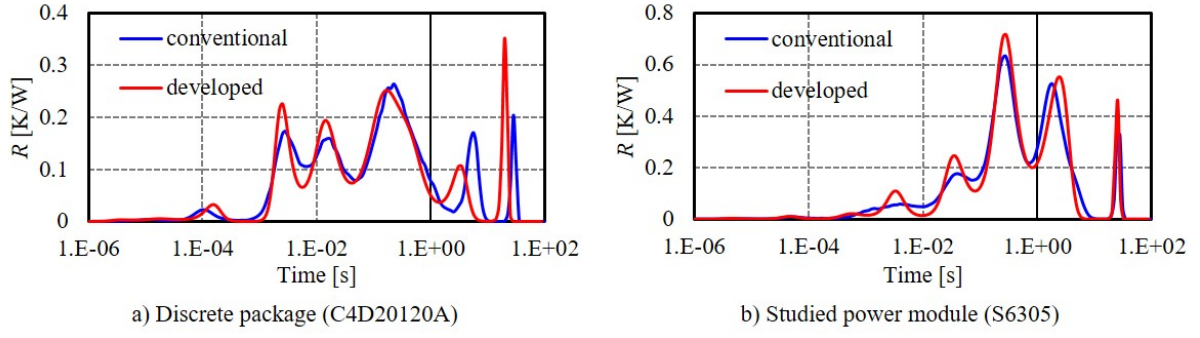
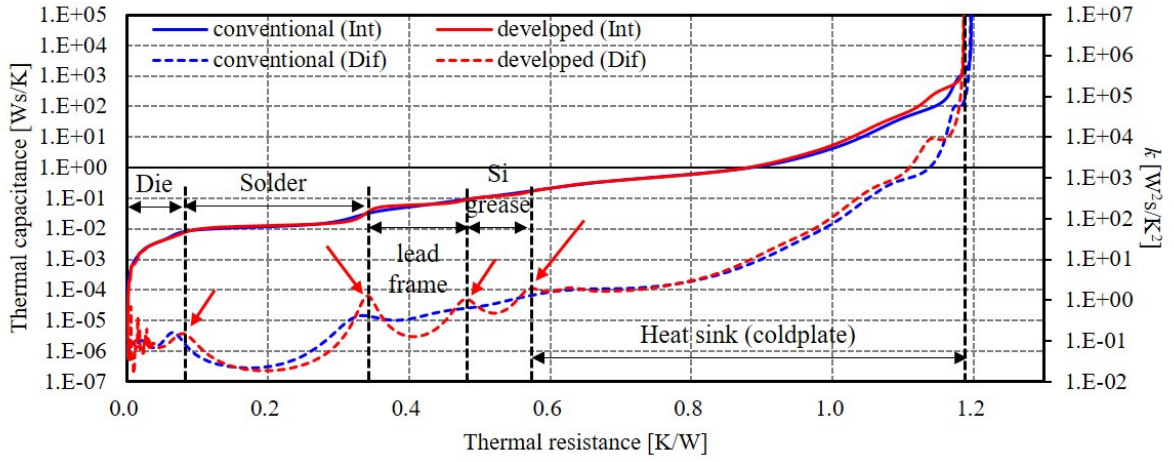
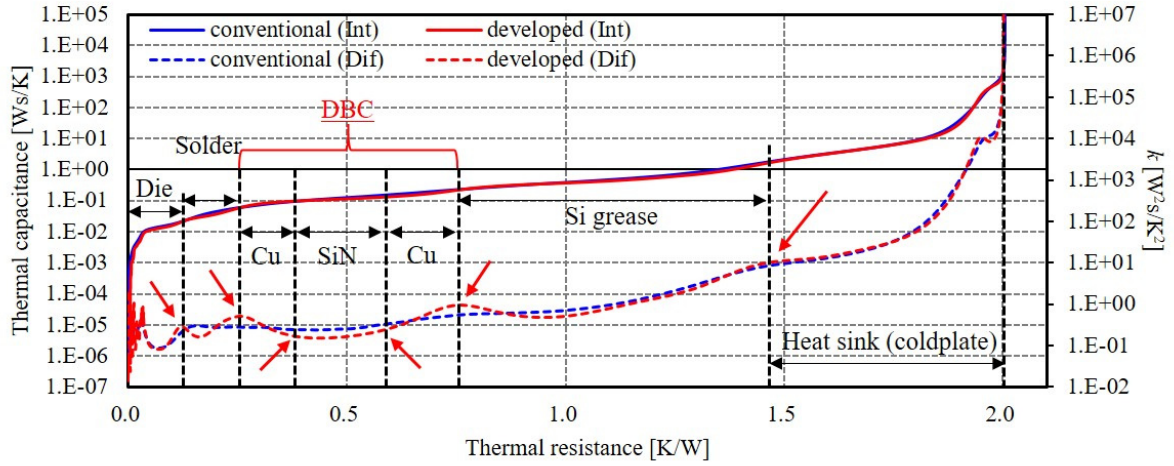


Fig. 13. TCS.



a) Discrete package (C4D20120A)



b) Studied power module (S6305)

Fig. 14. Structure function.

TCS with 1000 Bayesian iteration, respectively. The developed algorithm eliminates the measurement noise as shown in Fig. 12. The specific peak of TCS corresponding to its package is emphasized as shown in Fig. 13.

The structure function obtained from Fig. 13 is shown in Fig. 14. “Int” and “Dif” denote the integral and differential structure function, given as solid and dashed line, respectively. The inflection point of differential structure function for the developed algorithm is clear compared to the conventional algorithm indicated by red arrows in Fig. 14. The layer structure of tested discrete power device and

module package is identified as the structure function shown in Fig. 14. In general, it is difficult to clearly separate layers for low thermal resistance multi-layered structure e.g. DBC. The developed algorithm enables to identify DBC structure and obtain thermal resistance and capacitance of each layer. These results show that the developed algorithm enables the accurate extraction of transient thermal network model of power module packages.

5. Conclusions

This paper develops a signal processing algorithm to identify accurate transient thermal network model for power module packages. Measurement noise is eliminated in the logarithmic frequency domain after weighted discrete Fourier transformation. This paper evaluates the influence of quantization error and noise in the measured data using the developed algorithm. The high sampling frequency of ADC can suppress the influence of quantization error. Low-pass filtering in frequency domain using the developed algorithm eliminates the influence of measurement noise compared to the conventional algorithm. The transient thermal network model obtained by the developed algorithm for TO-247 discrete power device package and DBC substrate of power module package is easily extracted from the structure function. The developed signal processing algorithm enables to distinguish the boundaries of multi-layered substrate for power module in the structure function, and improve the accuracy of the identified transient thermal network model.

Acknowledgments

This work is partially supported by JST Open Innovation with Enterprises, Research Institute and Academia (OPERA) Program Grant Number JPMJOP1841, JAPAN.

References

- [1] J.L. Hudgins and G.S. Simin, *et al.*, “An Assessment of Wide Bandgap Semiconductors for Power Devices,” *IEEE Transaction on Power Electronics*, vol. 18, no. 3, pp. 907–914, May 2003.
- [2] T. Funaki and H. Inoue, *et al.*, “Characterization of SiC power module for high switching frequency operation,” *IEICE Electronics Express*, vol. 7, no. 14, pp. 1008–1013, July 2010.
- [3] J. Millam and P. Godignon, *et al.*, “A survey of wide bandgap power semiconductor devices,” *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2155–2163, May 2014.
- [4] H.A. Mantooth and M.D. Glover, *et al.*, “Wide bandgap technologies and their implications on miniaturizing power electronic systems,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 3, pp. 374–385, September 2014.
- [5] T. Kimoto and J.A. Cooper, *Fundamentals of silicon carbide technology: Growth, characterization, devices, and applications*, Wiley-IEEE Press, November 2014.
- [6] M. Carmona and S. Marco, *et al.*, “A time-domain method for the analysis of thermal impedance response preserving the convolution form,” *IEEE Transactions on Components and Packaging Technology*, vol. 22, no. 2, pp. 238–244, June 1999.
- [7] S. Yin and T. Wang, *et al.*, “Electro-thermal modeling of SiC power devices for circuit simulation,” *Proc. IECON 2013*, November 2013.
- [8] H. Chen and B. Ji, *et al.*, “Real-time temperature estimation for power MOSFETs considering thermal aging effects,” *IEEE Transactions on Device and Materials Reliability*, vol. 14, no. 1, pp. 220–228, March 2014.
- [9] J. Li and A. Castellazzi, *et al.*, “A physical RC network model for electrothermal analysis of a multichip SiC power module,” *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2494–2508, March 2018.
- [10] A.S. Bahman and K. Ma, *et al.*, “A lumped thermal model including thermal coupling and thermal boundary conditions for high-power IGBT modules,” *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2518–2530, March 2018.
- [11] Y. Mukunoki and T. Horiguchi, *et al.*, “Electro-thermal co-simulation of two parallel-connected SiC-MOSFETs under thermally-imbalanced conditions,” *Proc. 2018 APEC*, March 2018.

- [12] B. Du and J.L. Hudgins, *et al.*, “Transient electrothermal simulation of power semiconductor devices,” *IEEE Transactions on Power Electronics*, vol. 25, no. 1, pp. 237–248, January 2010.
- [13] A. Bryant and N.-A. Parker-Allotey, *et al.*, “A fast loss and temperature simulation method for power converters, part I: Electrothermal modeling and validation,” *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 248–257, January 2012.
- [14] A. Bryant and N.-A. Parker-Allotey, *et al.*, “A fast loss and temperature simulation method for power converters, part II: 3-D thermal model of power module,” *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 258–268, January 2012.
- [15] J. Reichl and J.M. Ortiz-Rodríguez, *et al.*, “3-D thermal component model for electrothermal analysis of multichip power modules with experimental validation,” *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 3300–3308, June 2015.
- [16] K. Ma and N. He, *et al.*, “Frequency-domain thermal modeling and characterization of power semiconductor devices,” *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 7183–7193, October 2016.
- [17] JESD51-14, “Transient dual interface test method for the measurement of the thermal resistance junction-to-case of semiconductor devices with heat flow through a single path,” *JEDEC*, November 2010.
- [18] E.N. Protonotarios and O. Wing, “Theory of nonuniform RC lines part I: Analytic properties and realizability conditions in the frequency domain,” *IEEE Transactions on Circuit Theory*, vol. 14, no. 1, pp. 2–12, March 1967.
- [19] V. Székely and T.V. Bien, “Fine structure of heat flow path in semiconductor devices; A measurement and identification method,” *Solid-State Electronics*, vol. 31, no. 9, pp. 1363–1368, September 1988.
- [20] JESD51-1, “Integrated circuits thermal measurement method - Electrical test method (single semiconductor device),” *JEDEC*, December 1995.
- [21] M. Glavanovics and H. Zitta, “Thermal destruction testing: an indirect approach to a simple dynamic thermal model of smart power switches,” *Proc. the 27th European Solid-State Circuits Conference*, September 2001.
- [22] T.J. Kennett and W.V. Prestwich, *et al.*, “Bayesian deconvolution I: convergent properties,” *Nuclear Instruments and Methods*, vol. 151, no. 1, pp. 285–292, May 1978.
- [23] T.J. Kennett and W.V. Prestwich, “On the deconvolution of exponential response functions,” *Physics in Medicine & Biology*, vol. 24, no. 6, pp. 1107–1122, November 1979.
- [24] T. Dabóczy and I. Kollár, “Multiparameter optimization of inverse filtering algorithms,” *IEEE Transactions on Instrumentation and Measurement*, vol. 45, no. 2, pp. 417–421, April 1996.
- [25] V. Székely, “Identification of RC networks by deconvolution: chances and limits,” *IEEE Transactions on Circuits and Systems -1: Fundamental Theory and Applications*, vol. 45, no. 3, pp. 244–258, March 1998.
- [26] SLAA323A, “Oversampling the ADC12 for higher resolution,” *Texas Instruments*, July 2018.
- [27] J.C. Candy, “Decimation for sigma delta modulation,” *IEEE Transactions on Communications*, vol. 34, no. 1, pp. 72–76, January 1986.
- [28] P.M. Aziz and H.V. Sorensen, *et al.*, “An overview of sigma-delta converters,” *IEEE Signal Processing Magazine*, vol. 13, no. 1, pp. 61–84, January 1996.
- [29] Z. Cvetkovic and I. Daubechies, *et al.*, “Single-bit oversampled A/D conversion with exponential accuracy in the bit rate,” *IEEE Transactions on Information Theory*, vol. 53, no. 11, pp. 3979–3989, November 2007.