Invited Paper

Cyclic reservoir neural network circuit for 3D IC implementation

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Abstract: Reservoir computing is a computational model inspired by the information processing of the brain. In particular, it shows high performance in time-series processing using recurrent neural network dynamics despite its simple structure. Furthermore, a simple learning algorithm only in the output layer is sufficient for training the entire network. Therefore, its efficient hardware implementation is highly expected. However, it is important for a reservoir network to have a rich variety of dynamics to deal with complex time-series information. To introduce rich dynamics in the reservoir network without degrading the network stability, a chaotic neural network reservoir was proposed. In this paper, we propose a cyclic reservoir neural network circuit suitable for a stacked three-dimensional (3D) integrated circuit (IC). Through 3D IC fabrication technology, in which several semiconductor substrates are vertically stacked and connected by through-silicon vias (TSVs), we can efficiently integrate the chaotic neural network reservoir circuit. We designed and fabricated a prototype IC chip of the proposed circuit with a TSMC 180 nm CMOS semiconductor process. We verified its operation through SPICE and MATLAB simulations and preliminary experiments with the fabricated prototype chip.

Key Words: reservoir neural network, chaotic neural network, 3D integrated circuit, analog neural network circuit

1. Introduction

Recently, Internet of Things (IoT) technology has connected various devices to the Internet and is expected to be applied in a wide range of fields such as medical [1], finance [2], automotive [3, 4], and agriculture [5, 6]. As a result of IoT technology, the amount of data processed by computers and information flowing through communication networks is rapidly increasing. Therefore, edge hardware, which will largely contribute to reducing the amount of information for data communication, has been actively developed. Edge hardware generally requires not only inference with high immediacy [7] but also local learning for personalized services [8–10]. Among the various computational models for edge hardware, models inspired by biological neural networks in the brain are suitable for edge devices because of their high efficiency in size and power consumption.

Reservoir computing [11, 12], which is a biologically motivated network model especially suitable for time-series processing, has attracted much attention. A reservoir neural network has a random recurrent network structure with sparse synaptic connections. Furthermore, it can be trained with a simple learning algorithm such as linear regression at the output layer only. Therefore, it is suitable for compact hardware implementation. On the other hand, it is preferable for reservoir networks to have high-dimensional complex dynamics such as chaotic dynamics to accommodate a rich variety of dynamics for efficient information processing. It is relatively easy to introduce chaotic dynamics in reservoir neural networks by appropriately setting synaptic connection weights among neurons in the reservoir layer. In this case, however, the reservoir neural network does not generally satisfy the “echo state property” (ESP) [11] because the network itself will be unstable. To solve this problem, a chaotic neural network reservoir [8, 13–21] consisting of chaotic neurons [22] was proposed.

Chaotic neural network reservoirs can achieve both reproducibility with robustness (consistency) and a rich variety of dynamics with sensitive responses to unknown inputs and abnormal internal states, which is considered important for high order processing in the brain, especially in the context of brainmorphic computation [8–10, 14, 17]. From a hardware point of view, the advantages of chaotic neural network reservoir are 1) ease of introducing complex dynamics with a small number of neurons [14, 17, 18, 23], and 2) the high-ability to solve certain problems with a smaller number of neurons in comparison with a normal reservoir neural network [14–16, 18–20, 23]. Therefore, a compact and efficient hardware system is highly possible with the use of chaotic neural network reservoir.

For efficient VLSI circuit implementation of a deep neural network (DNN), a cyclic neural network hardware architecture [24] suitable for vertically stacked (layered) three-dimensional (3D) integration [25–27] of feed-forward and back-propagating multi-layer neural networks was proposed. The integration method using the 3D IC stacking technology, in which several semiconductor substrates are vertically stacked, was considered disadvantageous for high-speed operation because the connection length between stacked IC chips increases with wiring, such as bonding wire and in-package wiring. However, wiring through silicon vias (TSVs) and microbumps can directly connect stacked IC chips without external wiring. Therefore, high-density integration of an IC system is possible, as illustrated in Fig. 1, where the circuits on different substrates are efficiently connected by TSVs. In addition, the TSV 3D IC stacking technology is relatively insensitive to noise because of the short connection distance, and the parasitic capacitance also decreases. Thus, the signal delay, attenuation, and waveform deterioration are reduced. Moreover, redundant circuits such as signal amplifiers for external wiring can be eliminated. As a result, the TSV 3D IC fabrication technology is highly expected to improve the overall performance of 3D integrated multi-layered neural networks, including the packaging density, operation speed, and power consumption [24–27].

Because the size of chaotic neural network reservoirs is much smaller than that of DNNs, the chaotic neural network reservoir can be effectively piggybacked with DNN using spare area in the 3D DNN system. Such a dual network system will be valuable because it will combine the superior pattern recognition abilities of DNNs with the high performance in time-series processing tasks that is characteristic of the chaotic neural network reservoirs. Neural networks consisting of neurons without internal dynamics such as ordinary DNNs can be freely constructed on a 3D cyclic neural network architecture [24]. However, recurrent neural networks with internal neuronal dynamics such as the

Fig. 1. Simplified schematic example of 3D stacked structure using TSVs.

chaotic neural network reservoir cannot be directly mapped on a 3D cyclic neural network architecture. To solve this problem, in this study, we propose a 3D IC technique that is compatible with recurrent neural networks such as the chaotic neural network reservoir [15, 18, 21].

In Section 2, we briefly introduce the chaotic neural network reservoir. In Section 3, we propose a cyclic recurrent neural network architecture suitable for a stacked TSV 3D IC structure. In addition, we show a strategy for mapping the chaotic neural network reservoir on the proposed 3D cyclic recurrent neural network IC architecture. In Section 4, a chaotic neural network reservoir circuit for the 3D cyclic network hardware architecture is proposed. In Section 5, we design and fabricate a prototype chip of the proposed cyclic chaotic neural network reservoir circuit using the TSMC 180 nm CMOS semiconductor process. We verify the proper operation of the prototype chip through bifurcation diagrams and return maps obtained from SPICE and MATLAB simulations, and circuit measurements of the fabricated prototype chip in Sections 6 and 7, respectively.

2. Chaotic neural network reservoir

Figure 2 illustrates the general construction of a reservoir neural network with an input, reservoir, and output layers [11, 12]. As shown in Fig. 2, the m -th neuron in the input layer is connected via input connection weight W_{im}^{in} to the i -th neuron in the reservoir layer. In the reservoir layer, the j -th neuron is connected through the internal connection weight W_{ij} to the i -th neuron. Typically, these connections are sparse, and their weight values are randomly set and fixed. By contrast, the output connection weight W_{qh}^{out} from the h -th neuron in the reservoir layer to the q -th neuron in the output layer is adjusted according to a simple learning algorithm such as a linear regression.

The chaotic neural network reservoir [8, 13, 14] uses a chaotic neural network [22, 28] for the reservoir layer. The state update equations of the i -th neuron in the chaotic neural network in the reservoir layer are given by

$$x_i(t+1) = kx_i(t) + \sum_{m=1}^M W_{im}^{\text{in}} u_m(t+1) + \sum_{j=1}^N W_{ij} f(x_j(t)) - \alpha f(x_i(t)) + \theta_i, \quad (1)$$

$$y_i(t+1) = f(x_i(t+1)), \quad (2)$$

$$f(x) = \frac{1}{1 + \exp(-x/\epsilon)}, \quad (3)$$

where $x_i(t)$ and $y_i(t)$ are the internal state and output of the i -th neuron at discrete time t , respectively; θ_i is the external bias to the i -th neuron; $u_m(t)$ is the m -th external input; k and α are refractoriness parameters; M is the number of input neurons in the input layer; N is the number of neurons in the

Fig. 2. General construction of reservoir neural network. Chaotic neural network reservoir employs a chaotic neural network for reservoir layers [8, 13, 14].

reservoir layer; and $f(\cdot)$ is the output function, for example, Eq. (3), where ϵ is the gain of the output function.

The output of the q -th neuron $y_q^{\text{out}}(t)$ in the output layer, which consists of Q neurons as shown in Fig. 2, is given by

$$y_q^{\text{out}}(t) = \sum_{h=1}^N W_{qh}^{\text{out}} y_h(t), \quad (4)$$

where $y_h(t)$ is the output of the h -th neuron in the reservoir layer. Furthermore, the output weight matrix $\mathbf{W}^{\text{out}}$ of W_{qh}^{out} for all q and h is trained using a linear regression as follows:

$$\mathbf{W}^{\text{out}} = f^{-1}(\mathbf{y}^{\text{teach}}) \mathbf{y}^{\text{out}^T} (\mathbf{y}^{\text{out}} \mathbf{y}^{\text{out}^T})^{-1}, \quad (5)$$

where $f^{-1}(\cdot)$ is the inverse function of the output function, $\mathbf{y}^{\text{teach}}$ is the teacher signal vector, and $\mathbf{y}^{\text{out}}$ is the network output vector of $y_q^{\text{out}}(t)$ for all q .

3. Reservoir neural network architecture for stacked 3D IC structure

To accommodate the reservoir neural network with a recurrent structure in the TSV 3D stacked structure shown in Fig. 1, we propose a cyclic recurrent neural network hardware architecture as shown in Fig. 3. In the figure, a single chaotic neural network reservoir is constructed with two identical semiconductor substrates as a whole. That is, the neural network circuit in the upper semiconductor die (chip or substrate) is a copy of that in the lower die. In the following, we call the lower semiconductor die as **Layer 1**, and the upper one as **Layer 2**. These two semiconductor dies are sandwiched between the upper and lower memory chips (UM and LM) in which the synaptic connection weights are stored. The memory dies, UM and LM, are not shown in Fig. 3 for simplicity.

In Fig. 3, the hexagons with a dot show neuron circuits whose outputs are voltage. The circles on the crossbar grid represent variable synaptic conductance circuits, that is, their outputs are currents. The neuronal states on each semiconductor die are alternatively (that is, cyclically) updated as follows: Neurons on **Layer 1** are updated at discrete time bearing even numbers $t = 2n$ where n is an integer, that is, $t = \dots, -2, 0, 2, 4, \dots$. By contrast, those on **Layer 2** at discrete times bear odd numbers $t = 2n + 1$ such as $t = \dots, -1, 1, 3, \dots$. The outputs of neurons on **Layer 1**, $y_j(2n)$, are transferred to the synaptic circuits on **Layer 2** using TSVs at $t = 2n$ as shown in blue lines in Fig. 3. Similarly, the outputs of neurons on **Layer 2**, $y_i(2n + 1)$, are transferred to **Layer 1** at $t = 2n + 1$ as indicated by red lines in the figure.

The output voltage of each neuron on **Layer 1** at $t = 2n$, $y_j(2n)$, which is transferred to **Layer 2** through a sample-and-hold (S/H) circuit, propagates to all the synaptic circuits located on a same

Fig. 3. Simplified schematic diagram of 3D two-layer chaotic neural network architecture. A cyclic chaotic neural network circuit consisting of two semiconductor substrates (Layer 1 and Layer 2) as a whole is sandwiched between upper and lower memory dies (UM and LM; not shown) to complete a four-die vertically stacked 3D chaotic neural network reservoir system.

segment (a slanting line in the figure) of the crossbar grid on Layer 2. At each synaptic circuit, the synaptic weight, W_{ij} , is multiplied to $y_j(2n)$, and a corresponding synaptic current is generated. All the synaptic currents from the synaptic circuits on the same horizontal segment of the crossbar grid on Layer 2 are summed by Kirchhoff's current law (KCL). Finally, the weighted sum of the neuronal outputs (a total synaptic current) is fed into the corresponding neuron circuit on Layer 2. The green line in Fig. 3 depicts a situation in which the 4th neuron on Layer 1 is sending its output voltage, $y_4(2n)$, to the synaptic conductance circuit, W_{24} , on Layer 2 for example. The weighted current is summed with those from other synaptic circuits on the same horizontal segment of the crossbar grid according to KCL, and is input to the 2nd neuron on Layer 2. At the next time step $t = 2n + 1$, the updated output of the 2nd neuron in Layer 2, $y_2(2n + 1)$, will be sent back to the neurons in Layer 1 through synaptic conductance circuits on the crossbar grid on Layer 1. The above procedure is cyclically repeated to realize a fully connected recurrent neural network with two vertically stacked semiconductor substrates (Layer 1 and Layer 2) as a whole. Inter-layer signal communications are realized using TSV paths, which make compact hardware implementations possible.

The values of synaptic weights W_{ij} on each semiconductor die are determined by the weight value signals coming through TSVs from LM in the case of Layer 1 or UM for Layer 2 as shown in Fig. 3 with brown lines. Using these signals, we can change the synaptic connection weight matrix whenever it is necessary, because the weight value control through LM and UM is independent of the neuronal state updating operations in Layer 1 and Layer 2. For example, we can use this weight value control to change the network structure or parameter by reloading the values for W_{ij} depending on applications. More importantly, as detailed in Section 4, we have to change the synaptic conductance value several times in one neuronal state update cycle, because we share one synaptic conductance circuit among different input variables to the neuron. Furthermore, we can retain the weight value on a volatile local memory device in the synaptic circuit such as a capacitor by periodically updating the weight values. In this paper, we use a small capacitor ($C_1^{(1)}$ and $C_1^{(2)}$ in Fig. 4) as a local memory for the synaptic conductance circuit in the prototype chip described in Section 5, so that we periodically update the charge on each capacitor. However, we are planning to use a non-volatile analog memory device such

as a spintronics device [29,30] in the synaptic circuit in near future. In this case, the periodical update is not necessary drastically reducing the power consumption. In addition, we are planning to implement the whole reservoir network shown in Fig. 2 including an on-chip online learning circuitry. Therefore, we need to update weight values W_{qh}^{out} in Fig. 2 for learning in real-time. The independent controllability of the weight values mentioned above can be efficiently utilized for the on-chip online learning.

4. Chaotic neuron circuit for cyclic architecture

As mentioned in Section 1, a 3D cyclic neural network architecture cannot be directly applied to neural networks consisting of neurons with internal dynamics. The chaotic neuron in Eqs. (1) and (2) is a typical dynamic neuron model [22,28]. The internal state $x_i(t)$ exponentially decays with time with a decay factor of k as shown in Eq. (1). Hence, it is necessary to devise a way to map the chaotic neural network onto the stacked 3D cyclic neural network hardware architecture shown in Fig. 3 [15, 18, 21].

To accommodate the recurrent chaotic neural network in the two-die stacked 3D cyclic neural network IC architecture shown in Fig. 3, we propose a chaotic neuron circuit which is deployed in two semiconductor layers [15, 18, 21]. A simplified schematic diagram of a proposed circuit for a single chaotic neuron is presented in Fig. 4. In the figure, Layer 1 and Layer 2 correspond to Layer 1 and Layer 2 in Fig. 3, respectively. The circuits in Layer 1 and Layer 2 are exactly the same, but their states are updated alternatively by cyclic use of these circuits. That is, two circuits together implement one chaotic neuron.

In Fig. 4, superscripts with parentheses show the layer number, and subscripts x, y, u , and θ show variables corresponding to those in Eqs. (1) and (2). In addition, $\phi_j^{(i)}$ denotes the j -th clock in the i -th layer, whose waveforms are shown in Fig. 5. In Fig. 4, S/H denotes a sample-and-hold circuit, CDS is a correlated double sampling circuit, and $f^{(i)}(\cdot)$ is a sigmoidal output function circuit.

The state update equations for the chaotic neuron circuit in Layer 1 in Fig. 4 are described as

Fig. 4. Simplified schematic diagram of a single cyclic chaotic neuron circuit deployed in two semiconductor dies (Layer 1 and Layer 2).

Fig. 5. Clock waveforms for circuit in Fig. 4.

$$V_x^{(1)}(t) = \frac{T_{int}}{C_2^{(1)}} \left\{ k^{(1)} V_x^{(2)}(t-1) + W_{in}^{(1)} V_u^{(1)}(t) - \alpha^{(1)} V_y^{(2)}(t-1) + \theta^{(1)} V_\theta^{(1)} \right\}, \quad (6)$$

$$V_y^{(1)}(t) = f \left(V_x^{(1)}(t) \right), \quad (7)$$

$$k^{(1)} = g^{(1)} \left(V_k^{(1)} \right), \quad (8)$$

$$W_{in}^{(1)} = g^{(1)} \left(V_{w_{in}}^{(1)} \right), \quad (9)$$

$$\alpha^{(1)} = g^{(1)} \left(V_\alpha^{(1)} \right), \quad (10)$$

$$\theta^{(1)} = g^{(1)} \left(V_{w_\theta}^{(1)} \right), \quad (11)$$

where $V_x^{(1)}(t)$, $V_y^{(1)}(t)$, and $V_u^{(1)}(t)$ denote the internal state, output, and input voltages of the neuron at time t ; $V_\theta^{(1)}$ is an external bias voltage, T_{int} determines the current integration period of the I/V converter circuit which consists of $C_2^{(1)}$ and an op-amp; $C_1^{(1)}$ is a voltage-holding capacitor for $Z^{(1)}$; and $g^{(1)}(Z^{(1)})$ gives a voltage-controlled conductance with a control voltage of $Z^{(1)}$. The conductance $g^{(1)}(\cdot)$ is determined by the MOSFET characteristic of $M^{(1)}$ in Fig. 4. The control voltage signal $Z^{(1)}$ is appropriately switched to supply $V_k^{(1)}$, $V_{w_{in}}^{(1)}$, $V_\alpha^{(1)}$, and $V_{w_\theta}^{(1)}$, in a time-multiplex manner through TSVs to determine the corresponding values for $k^{(1)}$, $W_{in}^{(1)}$, $\alpha^{(1)}$, and $\theta^{(1)}$, respectively, as given by Eqs. (8) to (11). The terms in the braces in Eq. (6) represent currents that correspond to the terms in Eq. (1). That is, $k^{(1)} \rightarrow k$, $W_{in}^{(1)} \rightarrow W_{lm}^{in}$, $\alpha^{(1)} \rightarrow \alpha$, and $\theta^{(1)} \rightarrow \theta$. Note that the term which corresponds to W_{ij} in Eq. (1) is missing in Eq. (6) because Eq. (6) describes only one neuron.

A salient feature of the proposed circuit is to realize the exponential decay of the internal state $x_i(t)$ with a decay factor of k as given by the 1st term of the right-hand side of Eq. (1). In the circuit, as given by Eq. (6), $V_x^{(2)}(t-1)$ on Layer 2 multiplied by k is needed to update $V_x^{(1)}(t)$ on Layer 1. To accomplish this, copying the internal state voltage in another layer is required. This function is implemented in the proposed circuit by bypassing the output function circuit $f^{(2)}(\cdot)$ using the toggle switch $TS^{(2)}$. When $\phi_{2S}^{(2)}$ is high, the internal state voltage $V_x^{(2)}(t-1)$ is output to Layer 1. At the same time, $V_k^{(1)}$ is loaded to $Z^{(1)}$ to multiply k to $V_x^{(2)}(t-1)$. This time-multiplex scheme requires only one TSV saving the chip area and improving the reliability.

The circuit equations for Layer 2 are the same as those in Eqs. (6) to (11), but superscript (1) should be exchanged to (2).

5. Prototype chip design and fabrication

To verify the operation of the proposed circuit in Fig. 4, we designed and fabricated a prototype chip using the TSMC 180 nm CMOS semiconductor process. Figure 6 shows a microphotograph of the prototype chip. The prototype chip contains chaotic neuron circuits with which we can emulate a two-die stacked cyclic chaotic neuron circuit, as shown in Fig. 4. Auxiliary circuitry for testing purposes is also integrated on the chip. Table I lists the specifications of the prototype chip.

Fig. 6. A microphotograph of the prototype chip.

Table I. Specifications of prototype chip.

Process	TSMC 180 nm Mixed-signal
Supply voltage	Core : 1.8 V, I/O : 3.3 V
Number of pins	84
Chip size	2.5 mm × 2.5 mm

6. SPICE and MATLAB simulations

To compare the designed and measured characteristics, we conducted SPICE circuit simulations of the voltage-controlled conductance characteristic of the MOSFET $M^{(i)}$ in Fig. 4 using the post-layout circuit information. This gives the function $g^{(i)}(\cdot)$ in Eqs. (8) to (11). Conditions for simulations are summarized in Table II. The obtained characteristic is shown in Fig. 7. In the figure, the horizontal axis is the drain-source voltage V_{DS} of the MOSFET $M^{(i)}$ in Fig. 4, and the vertical axis is its drain current I_D . In addition, we obtained the input-output characteristic of the output function circuit $f^{(i)}(\cdot)$ in Fig. 4 as shown in Fig. 8. As shown in Table II, we used $V_{dd} = 2.4$ V instead of the nominal value of 1.8 V listed in Table I. This is because the embedded digital control circuitry needs to be driven by 2.4 V to guarantee proper operations. In addition, we set the analog common voltage $V_{com} = 0.8$ V instead of the nominal value of 0.9 V to use a relatively linear portion of the transconductance characteristics $g^{(i)}(\cdot)$ shown in Fig. 7. These circuit bugs have been fixed for the next prototype chip.

Using the circuit characteristics shown in Figs. 7 and 8, we obtain a bifurcation diagram of the internal state voltage $V_x(t)$ when we sweep the external bias voltage V_θ as a bifurcation parameter using a MATLAB simulation, as shown in Fig. 9(a). In addition, the return maps of $V_x(t)$ and $V_x(t+1)$ are obtained for $V_\theta = 0.741$ V and $V_\theta = 0.845$ V, as shown in Figs. 10(a) and 10(b), respectively. Figure 9(a) shows a typical bifurcation structure of the chaotic neuron model [22]. However, the shape is not symmetric because of the unavoidable nonlinear characteristics of the circuit elements.

Table II. Simulation conditions.

Power supply voltage : V_{dd}	2.4 V
Analog ground voltage : V_{com}	0.8 V
$V_k, V_\alpha, V_{w\theta}$	2.0 V
Operating frequency	100 kHz

Fig. 7. Voltage-controlled conductance characteristics of MOSFET $M^{(i)}$ in Fig. 4 when gate voltage of V_G is set at 2.0 V. Blue line shows characteristics obtained by SPICE simulation, and red line is obtained from a prototype circuit measurement.

Fig. 8. Input-output characteristics of output function circuit $f^{(i)}(\cdot)$ in Fig. 4. Blue line shows characteristics obtained by SPICE simulation, and red line shows measured results from prototype chip.

7. Circuit measurements

We measured the voltage-controlled conductance characteristic $g^{(i)}(\cdot)$ and the input-output characteristic of $f^{(i)}(\cdot)$ from the fabricated prototype chip. The results are shown by the red lines in Figs. 7 and 8. As shown in these figures, the measured results show in satisfactory good agreements with simulations. However, because of variations and nonlinearities in actual device characteristics in addition to the after fabrication voltage tuning for V_{com} and V_{dd} mentioned in Section 6, small deviations from SPICE simulations were observed in the measured results. In particular, the voltage transfer characteristic of $f^{(i)}(\cdot)$ is shifted to the left a little. In addition, the lower saturation voltage is smaller than that obtained from SPICE.

We then measured a bifurcation diagram of the internal state voltage $V_x(t)$ when we swept the

(a)

(b)

Fig. 9. Bifurcation diagrams of internal state voltage $V_x(t)$ when we change external bias voltage V_θ from 0.6 V to 1 V with a 0.001 V step as a bifurcation parameter. At each value of V_θ , 100 points after 900 iterations are plotted. (a) SPICE and MATLAB simulations, and (b) experimental results.

external bias voltage V_θ , as shown in Fig. 9(b). In addition, the return maps of the internal state voltage $V_x(t)$ and $V_x(t+1)$ were obtained from the measurements, as shown in Fig. 11. First, as shown in Fig. 9(b), a horizontal shrink of the bifurcation diagram was observed in comparison with that from SPICE simulation in Fig. 9(a). This is more vividly shown in the return maps. That is, the size of the return maps obtained from experiments taken at the same external bias voltage sets as simulations, i.e., $V_\theta = 0.741$ V and $V_\theta = 0.845$ V, shrunk in comparison with those from simulations. These shrinkages in return maps reflect the shrinkage in the bifurcation diagram. The main cause of these discrepancies must be the deviations in $f^{(i)}(\cdot)$ mentioned above, because the overall shapes of the bifurcation diagram and return maps are highly affected by the shape of $f^{(i)}(\cdot)$. In addition, the nonlinearity in $g^{(i)}(\cdot)$ would also affect the results. Second, the measured bifurcation diagram in Fig. 9(b) is smeared, and the points in measured return maps are fluctuated. The cause of these dynamical variations must be noise and clock jitters attributed to measurement setups.

Nevertheless, the measured results qualitatively confirm proper operations of the fabricated circuit as a chaotic neuron [22, 28, 31–33]. We rely on high-dimensional collective complex dynamics emerged in the chaotic neural network reservoir circuit [28, 31–33]. Furthermore, utilizing noise, deviations, and uncertainty is important in complex dynamical systems with robustness and rich variety [8–10, 28,

Fig. 10. Return maps of internal state voltage $V_x(t)$ and $V_x(t+1)$ obtained by simulations when external bias voltage V_θ is (a) $V_\theta = 0.741$ V (Dark brown one-dot chain line in Fig. 9(a)), and (b) $V_\theta = 0.845$ V (Dark green two-dot chain line in Fig. 9(a)). 300 points after 9,700 iterations are plotted.

Fig. 11. Return maps of internal state voltage $V_x(t)$ and $V_x(t+1)$ obtained by measurements when external bias voltage V_θ is (a) $V_\theta = 0.741$ V (Dark brown one-dot chain line in Fig. 9(b)), and (b) $V_\theta = 0.845$ V (Dark green two-dot chain line in Fig. 9(b)). 300 points after 9,700 iterations are plotted.

33–35]. In such complex systems, fine details of the circuit characteristics do not matter. Therefore, the deviations in measured characteristics mentioned above are acceptable.

8. Conclusions

We proposed a cyclic reservoir neural network architecture together with a two-semiconductor-layered chaotic neural network reservoir circuit suitable for a stacked TSV 3D structure. We designed and fabricated a prototype chip of the proposed circuit using the TSMC 180 nm CMOS semiconductor process. We confirmed the functionality of the prototype chip by comparing the bifurcation diagrams and return maps of the internal state voltage of the chaotic neuron circuit obtained from simulations and measurements.

We have designed and fabricated an improved chaotic neural network circuit chip for a large-scale reservoir neural network based on the results presented in this paper. In addition, we are currently designing a memory chip for the new chaotic neural network chip, with which we will construct a TSV 3D four-die stacked reservoir neural network system proposed in Section 3. We will quantitatively evaluate the performance of resulting TSV 3D stacked chaotic neural network reservoir IC system including size, speed, power consumption, and so on. Moreover, we will apply it to practical problems for edge computing hardware. The results for the full IC implementation will be reported elsewhere.

On the other hand, performance evaluation and analysis of the chaotic neural network reservoir are also important issues. We have already evaluated the performance of the chaotic neural network reservoir using word recognition tasks, nonlinear time-series classification tasks, and nonlinear time-series prediction tasks in addition to standard NARMA tests for memory capacity [13, 15–20]. As a consequence, we confirmed that the chaotic neural network reservoir has superior performance to a conventional neural network reservoir. Furthermore, we have analyzed complex dynamics emerged in the chaotic neural network reservoir through evaluation indices of information theory and nonlinear dynamics such as Lyapunov spectrum, permutation entropy, spatial mutual information, Kullback-Leibler divergence, Fisher information, and a complexity-entropy causality plane. The results will be submitted elsewhere soon [23].

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References

- [1] E. Ranjbar, R.G. Sedehi, M. Rashidi, and A.A. Suratgar, “Design of an IoT-based system for smart maintenance of medical equipment,” in *Proc. of International Conference on Internet of Things and Applications*, pp. 1–12, 2019. DOI: 10.1109/IICITA.2019.8808841
- [2] N. Arora and P.D. Kaur, “Augmenting banking and FinTech with intelligent Internet of things technology,” in *Proc. of International Conference on Reliability, Infocom Technologies and Optimization*, pp. 648–653, 2020. DOI: 10.1109/ICRITO48877.2020.9198018
- [3] I.B. Aris, R.K.Z. Sahbusdin, and A.F.M. Amin, “Impacts of IoT and big data to automotive industry,” in *Proc. of the Asian Control Conference*, pp. 1–5, 2015.
- [4] M. Dragojević, S. Stević, G. Stupar, and D. Živkov, “Utilizing IoT technologies for remote diagnostics of next generation vehicles,” in *Proc. IEEE 8th International Conference on Consumer Electronics*, pp. 1–4, 2018. DOI: 10.1109/ICCE-Berlin.2018.8576249
- [5] R. Dagar, S. Som, and S.K. Khatri, “Smart farming – IoT in agriculture,” in *Proc. of International Conference on Inventive Research in Computing Applications*, pp. 1052–1056, 2018. DOI: 10.1109/ICIRCA.2018.8597264
- [6] K.A. Patil and N.R. Kale, “A model for smart agriculture using IoT,” in *Proc. of International Conference on Global Trends in Signal Processing, Information Computing and Communication*, pp. 543–545, 2016. DOI: 10.1109/ICGTSPICC.2016.7955360
- [7] W. Yu, F. Liang, X. He, W.G. Hatcher, C. Lu, J. Lin, and X. Yang, “A survey on the edge computing for the Internet of things,” *IEEE Access*, vol. 6, pp. 6900–6919, 2018. DOI: 10.1109/ACCESS.2017.2778504
- [8] Y. Horio, “A brainmorphic computing hardware paradigm through complex nonlinear dynamics,” in *Understanding Complex Systems*, V. In, P. Longhini, and A. Palacios, eds., pp. 36–43, Springer, 2019. DOI: 10.1007/978-3-030-10892-2_5
- [9] Y. Horio, “Brainmorphic computing and expectations for physical devices,” *Oyo Butsuri*, vol. 88, no. 9, pp. 610–623, 2019. (in Japanese) DOI: 10.11470/oubutsu.88.9.619

- [10] Y. Horio, “Brainmorphic computing hardware and human-centric edge AI,” *The Brain and Neural Networks*, vol. 25, no. 4, pp. 140–147, 2018. (in Japanese) DOI: 10.3902/jnns.25.140
- [11] H. Jaeger, “The “echo state” approach to analysing and training recurrent neural networks,” Technical Report GMD, Report 148, German National Research Center for Information Technology, 2001.
- [12] M. Lukoševičius and H. Jaeger, “Reservoir computing approaches to recurrent neural network training,” *Computer Science Review*, vol. 3, no. 3, pp. 127–149, 2009. DOI: 10.1016/j.cosrev.2009.03.005
- [13] T. Tassy and Y. Horio, “Time series prediction through chaotic neural network reservoir,” in *Proc. of the IEICE General Conference*, N-1-2, 2018.
- [14] Y. Horio, “Chaotic neural network reservoir,” in *Proc. of International Joint Conference on Neural Networks*, pp. 1–5, 2019. DOI: 10.1109/IJCNN.2019.8852265
- [15] M. Inoue, K. Fukuda, and Y. Horio, “Switched-capacitor circuit implementation of the chaotic neural network reservoir,” *Journal of Signal Processing*, vol. 24, no. 4, pp. 133–136, 2020. DOI: 10.2299/jsp.24.133
- [16] M. Inoue, K. Fukuda, and Y. Horio, “Application of the chaotic neural network reservoir to speech recognition,” Technical Report, IEICE, NLP2019-103(2020-01), pp. 95–98, 2020. (in Japanese)
- [17] K. Fukuda, M. Inoue, and Y. Horio, “Quantitative evaluation of dynamics in chaotic neural network reservoir,” *IEICE Tech. Rep.*, vol. 119, no. 381, NLP2019-102, pp. 89–94, 2020. (in Japanese)
- [18] K. Fukuda, “Chaotic neural network reservoir –Analysis of dynamics and 3D circuit system integration–,” Master’s Thesis for Grad. School of Info. Sci., Tohoku Univ., 2021. (in Japanese)
- [19] K. Kudo, K. Fukuda, Y. Horio, and K. Kiyoyama, “Evaluation of 3D chaotic neural network reservoir IC characteristics through discrete word recognition,” in *Proc. of IEICE General Conference*, N-1-2, p. 209, 2021. (in Japanese)
- [20] K. Kudo, K. Fukuda, and Y. Horio, “On an online learning rule for reservoir neural network hardware,” *IEICE Tech. Rep.*, NC2020-66(202-03), pp. 133–138, 2021. (in Japanese)
- [21] K. Fukuda, Y. Horio, T. Orima, and K. Kiyoyama, “Cyclic reservoir neural network circuit for 3D IC implementation,” *Proc. NOLTA*, pp. 81–84, 2020.
- [22] K. Aihara, T. Tanabe, and M. Toyoda, “Chaotic neural network,” *Phy. Lett. A*, vol. 144, issues 6–7, pp. 333–340, 1990. DOI: 10.1016/0375-9601(90)90136-C
- [23] K. Fukuda and Y. Horio, “Analysis of dynamics in chaotic neural network reservoirs: Time-series prediction tasks,” submitted to Special Section on Nonlinear Dynamical Aspects of Edge Computing and Neuromorphic Hardware, *NOLTA*, 2021.
- [24] M. Koyanagi, “3D heterogeneous integration technology for AI system,” in *Proc. IEEE Int. Symp. on VLSI Design, Automation and Test*, J2-2, 2020. DOI: 10.1109/VLSI-DAT49148.2020.9196249
- [25] M. Koyanagi, H. Kurino, K.W. Lee, K. Sakuma, N. Miyakawa, and H. Itani, “Future system-on-silicon LSI chips,” *IEEE Micro*, vol. 18, no. 4, pp. 17–22, 1998. DOI: 10.1109/40.710867
- [26] M. Koyanagi, “Recent progress in 3D integration technology,” *IEICE Electronics Express*, vol. 12, no. 7, pp. 1–17, 2015. DOI: 10.1587/elex.12.20152001
- [27] T. Fukushima, H. Kikuchi, Y. Yamada, T. Konno, J. Liang, K. Sasaki, K. Inamura, T. Tanaka, and M. Koyanagi, “New three-dimensional integration technology based on reconfigured wafer-on-wafer bonding technique,” in *Proc. IEEE Int. Electron Devices Meet.*, pp. 985–988, 2007. DOI: 10.1109/IEDM.2007.4419119
- [28] K. Aihara, “Chaotic engineering and its application to parallel distributed processing with chaotic neural networks,” *Proc. IEEE*, vol. 90, no. 5, pp. 919–930, 2002. DOI: 10.1109/JPROC.2002.1015014
- [29] W.A. Borders, H. Akima, S. Fukami, S. Moriya, S. Kurihara, Y. Horio, S. Sato, and H. Ohno, “Analogue spin-orbit torque device for artificial-neural-network-based associative memory operation,” *Applied Physics Express*, vol. 10, 013007, DOI: 10.7567/APEX.10.013007, 2016.

- [30] A. Kurenkov, S. DuttaGupta, C. Zhang, S. Fukami, Y. Horio, and H. Ohno, “Artificial neuron and synapse realized in an antiferromagnet/ferromagnet heterostructure using dynamics of spin-orbit torque switching,” *Advanced Materials*, vol. 31, 1900636, DOI: 10.1002/adma.201900636, 2019.
- [31] Y. Horio, K. Aihara, and O. Yamamoto, “Neuron-synapse IC chip-set for large-scale chaotic neural networks,” *IEEE Trans. on Neural Networks*, vol. 14, no. 5, pp. 1393–1404, 2003.
- [32] Y. Horio, T. Ikeguchi, and K. Aihara, “A mixed analog/digital chaotic neuro-computer system for quadratic assignment problems,” *Neural Networks*, vol. 18, no. 5-6, pp. 505–513, 2005. DOI: 10.1016/j.neunet.2005.06.022
- [33] Y. Horio and K. Aihara, “Analog computation through high-dimensional physical chaotic neuro-dynamics,” *Physica-D*, vol. 237, no. 9, pp. 1215–1225, 2008. DOI: 10.1016/j.physd.2008.01.030
- [34] K. Aihara, J. Imura, Y. Horio, H. Suzuki, and S. Horai, “Mathematical theory for modelling complex systems and its transdisciplinary applications in science and technology,” *IEICE Fundamentals Review*, vol. 8, no. 4, pp. 218–228, 2015. DOI: 10.1587/essfr.8.218 (in Japanese)
- [35] Y. Horio, “A design technique for complex engineering systems,” *The Journal of IEICE*, vol. 98, no. 11, pp. 997–1001, 2015. (in Japanese)