A sub-0.3V highly efficient CMOS rectifier for energy harvesting applications

Dan Niu1a), Zhangcai Huang2, Minglu Jiang1, and Yasuaki Inoue1

1 Graduate school of Information, Production and Systems, Waseda University, Kitakyusyu-shi, Fukuoka 808-0135, Japan
2 Fukuoka Industry, Science and Technology Foundation, Fukuoka 814-0001, Japan

Received October 31, 2011; Revised March 9, 2012; Published July 1, 2012

Abstract: This paper presents a sub-0.3V CMOS full-wave rectifier for energy harvesting devices. By adopting a body-input comparator with simple bias circuit, combining with body bias technique, the lowest input voltage amplitude can be reduced to 0.28V when using a standard CMOS 0.18\(\mu\)m process. Moreover, the voltage drop of negative voltage converter can be reduced to enhance the output voltage efficiency by adopting the proposed body bias technique. In combination with minimum reverse current and simple bias circuit in the proposed comparator, the proposed active rectifier can achieve the peak voltage conversion efficiency of over 96% and the maximum power efficiency of approximately 94%.

Key Words: CMOS rectifier, energy harvester, body-input comparator, body bias technique

1. Introduction

Energy harvesting systems have recently attracted a great deal of interest within both the academic community and industry [1], as a potential inexhaustible source for low-power wireless devices. Comparing to conventional battery-powered systems, the systems powered by energy harvesting generators dominate little size, no unwanted maintenance burden of replacement, less toxic waste for the environment and reduce installation costs by eliminating wiring. Moreover, the output voltage of most energy harvesting devices is low, for example the thermo-electric generators (TEG) and silicon based micro-fuel cells can just produce voltages in the range of 0.2-0.6V [2]. Of the different sources like in [3–5], mechanical vibration energy is one of the main sources for harvesters and it is much appropriate for systems in a technical environment like engines. In order to become a useful system, energy harvesting devices generally require some interface circuits between harvester and load. Figure 1 shows the schematic of vibrational energy harvester. Firstly useful vibrations can be converted into electrical energy usually using transducer like piezoelectric, electromagnetic and electrostatic [6]. Then the output ac voltage of the transducer can be converted into a dc voltage by the ac/dc converter circuit (rectifier), while the regulator (for example, charge pump circuit) performs dc to dc conversion to provide stable supply voltage for the load system. For most vibration-powered energy harvesting
systems, the useful working frequency is between mHz and kHz [6], while the output voltage and power are low. Therefore, an ultra-low voltage rectifier with high efficiency is necessary. Moreover, the ultra-low output voltage of rectifier can be boosted to a needed voltage by the charge pump in [7], which can accept a minimum input voltage of around 150mV.

Researches on rectifiers have resulted in some remarkable advances. Conventional rectifiers are achieved by diodes and capacitors. A diode-bridged rectifier is a simple way to realize a full wave rectifier and it is mainly used in high voltage applications for inherent 2V\text{th} voltage drop. Schottky diodes can supply a voltage drop of about 0.3V each, but not being standard process and high reverse leakage are its disadvantages. In CMOS-only implementation circuit, the diodes can be replaced by diode-connected MOS transistors. In [9], two diodes of the diode bridge rectifier are replaced by two cross-coupled NMOS transistors. However the other two diodes are still implemented by diode-connected PMOS transistors to block the reverse current and therefore the efficiency is not optimized for the voltage drop on the diode. The CMOS rectifier with the active diode [8,10] is an innovative concept and it can achieve very high output voltage and power efficiency by using active diode to replace the diode-connected PMOS and NMOS transistors in the conventional rectifier. The active diode is composed of a MOSFET switch driven by a comparator, which controls the on and off states of the switch depending on the voltage difference over the switch. Such active diode aims for an ideal diode, with current flowing in only forward direction and nearly no voltage drop. Several rectifiers using active diode can be found in literatures. The active rectifier in [11] requires 4 comparators for a full wave rectifier and each comparator requires around 17\mu A. In [12–15], they use two active diodes to replace the diode-connected transistors. The two phase lead comparators in [12] require a small capacitor for start-up and the lowest input voltage frequency is 0.1MHz. However, large input voltage amplitude of the rectifier is its disadvantage. In [13], each comparator of the active full-wave rectifier requires an external power supply of 2.5 V, with the VDD and VSS of each comparator set at different voltage level [13]. These rectifiers have high voltage efficiency. However, they are not able to work below 1.2V input voltage and thus not sufficient for ultra-low voltage systems. Another drawback is that at least two power consuming comparators are needed. A reduction to only one comparator is necessary concerning power efficiency. In [16–20], the rectifiers with a negative voltage converter and only one active diode are proposed. The working frequency of rectifier in [16] is 125kHz and the minimum input voltage amplitude is 1.25V. The minimum input voltage amplitude is further decreased to around 0.7V [17, 19]. A concept using body-input techniques is presented in [18, 20]. The minimum operating voltage is 380mV [20].

In this paper, a sub-0.3V CMOS rectifier is proposed. A body-input comparator and body bias technique are used to allow the rectifier to work with just 0.28V input voltage with high voltage and power efficiency. In addition, comparing with the rectifier in [18,20], the proposed rectifier has some merits. Firstly, the input voltage amplitude can be further decreased to 0.28V with higher efficiency. Secondly, the bias circuit of proposed rectifier is very simple and does not need a resistor and an start-up circuit like in [18,20], which will decrease the chip area. At the same time, the bias circuit of the comparator in [18, 20] is large power consumption part, which takes up approximately 25% of the total power loss for the rectifier [18, 20]. Thirdly, the proposed rectifier can achieve nearly no reverse current, which exists in rectifier [18, 20].

This paper is organized as follows. Section 2 presents the principle of proposed sub-0.3V CMOS rectifier.
rectifier. The simulation results are shown in Section 3, followed by concluding remarks in Section 4.

2. Proposed low voltage rectifier

This active rectifier is mainly used in ultra-low voltage energy harvesters with ultra-low output voltage and low output energy (\(\mu\text{W}\) to mW). In addition, most energy harvesting systems work in low frequency and the rectifier with up to 3kHz working frequencies can satisfy the demand. Therefore, the main goals of this active rectifier are the reduction of the input voltage amplitude and the achievement of a high efficiency. Figure 2 shows the structure of the proposed rectifier. It consists of two stages: the negative voltage converter (NVC) stage and the active diode stage. The first stage NVC is used to convert the negative half wave into a positive one. However, the first stage itself cannot control the current direction and therefore it is not able to retain the charge on the storage capacitor. This is realized with the second stage: the diode stage. In this stage, a diode-connected PMOS transistor or an active diode is usually used. Compared to a diode-connected PMOS transistor, an active diode has a strongly reduced voltage drop, which is only some tens of millivolt [20]. However, an active diode has a permanent current consumption caused by the control circuit.

2.1 Negative voltage converter

This first stage is used to convert the negative half waves of the input sinusoidal waves into positive ones, which is achieved by two PMOS and two NMOS transistors. The proposed negative voltage converter circuit is shown in Fig. 3. During the positive half period of the input (\(V_{in1} > V_{in2}\)), MP1 and MN2 will be conductive when the input voltage increases and gets larger than \(|V_{thp}|\) and \(V_{thn}\). The terminal A is connected to \(V_{in1}\) and terminal B is connected to \(V_{in2}\). Similarly, for the negative half period of the input voltage, MP2 and MN1 are conducting and terminal A is connected to \(V_{in2}\). Therefore, the high potential of \(V_{in}\) is always at node A, while the low voltage potential is at node B. In contrast to MOS diodes, no threshold voltage drop \(V_{th}\) occurs between the input and the output of the first stage. The voltage drop of the NVC circuit is \(|V_{ds}| + V_{dsn}\), where \(V_{ds}\) and \(V_{dsn}\) are the dropout voltages of PMOS transistors MP1/MP2 and NMOS transistors MN1/MN2, respectively. For such an ultra-low voltage rectifier design, the ultra-low voltage drop is needed for achieving high output voltage efficiency. One method of achieving the ultra-low voltage drop is to increase transistor sizes, while it will result in large area consumption. In this work body bias technique is presented to lower the voltage drop and this technique can also reduce area consumption. For example, in order to achieve 11mV voltage drop, the widths of four transistors (MP1~MN2 in Fig. 3) should be 90000\(\mu\text{m}\), while the widths can be reduced to 60000\(\mu\text{m}\) by adopting the proposed body bias technique. The threshold voltage \(V_{th}\) is the function of the source-body voltage \(V_{BS}\) and it is explained as follows [21].

\[
V_{th} = V_{th0} + \gamma (\sqrt{2\phi_F} - V_{BS}) - \sqrt{2\phi_F}).
\]  

Herein \(\gamma\), \(\phi_F\) and \(V_{BS}\) are the body factor, the body surface potential and the source-body voltage. \(V_{th}\) can be reduced by increasing the source-body voltage \(V_{BS}\). At the same time, the low voltage drop means the low on-resistance, which can be achieved by adding proper bias voltages to the body terminals of the two PMOS transistors (MP1 and MP2). Additionally, the body terminals of the two NMOS transistors (MN1 and MN2) are connected to ground since the twin-well process is
not standard process and it is expensive. In this work the bias voltages can be obtained by using two diode-connected NMOS transistors (MN3 and MN4) to divide the output voltage of negative voltage converter ($V_{nvc}$) to two parts. The proper body bias voltage can avoid open pn-junctions and obtain negligible body leakage currents of two PMOS transistors (MP1 and MP2). In our case two ratios of $26\mu m/0.22\mu m$ and $23\mu m/0.22\mu m$ (MN3 and MN4) are used. Additionally, the body leakage currents will increase as temperature. In this paper, the average body leakage currents of MP1 and MP2 are labelled as $I_{leak}$. The current of load resistor $R_L$ (as shown in Fig. 2) is labelled as $I_{load}$. Then the ratios of $I_{leak}/I_{load}$ versus the temperature are shown in Fig. 4. From this figure, the body leakage current $I_{leak}$ is just around $25nA$ for the input voltage of $0.7V$ at $100^{\circ}C$ and it can be negligible compared to the output load current $I_{load}$ (around $17\mu A$). At the same time, proper transistor dimensions of the two diode-connected NMOS transistors (MN3 and MN4) are also important to lower the total current consumption, the average current of the two diode-connected NMOS transistors is only around $3pA$ at $0.7V$ input voltage. In this work, the voltage drop can be reduced by $33\%$ without increasing the transistor sizes by adopting the proposed body bias technique. However the negative voltage circuit cannot control the current direction and reverse current occurs. Therefore, a second stage is necessary to realize a useful rectifier.

2.2 Active diode

The main aim of this stage is to control the current direction and to make the active diode work nearly as an ideal diode with ultra-low voltage drop as well. Figure 5 shows the circuit of active diode, whose input is the output voltage of the converter ($V_{nvc}$). The proposed active diode includes a PMOS switch controlled by a novel comparator. Transistors M1-M12 work as a comparator to control the gate voltage of PMOS switch. No additional start-up circuit is necessary, since the output voltage of the comparator is low and the PMOS switch is on when the $V_{nvc}$ is higher compared to the $V_{out}$ during start-up. Vice versa, if the $V_{out}$ is higher, the output voltage of comparator is high and the PMOS switch is off to block the reverse current. At the same time, the appropriate size of the PMOS switch is important. A wide transistor can reduce the on-resistance, but the large area needed
and the increase of the gate capacitance must be considered. The active body biasing block consisting of M21 and M22 is necessary. This block is adopted to prevent the PMOS body-junction diode from turning on during start-up for better reliability [11]. The sizes of M21 and M22 can be small since only very low current flows during the start-up phase. In addition, the bypass PMOS diode in parallel with the active diode [18, 20] is added to promote start-up of the active diode over all process corners, while it can enhance the start-up speed and decrease the time for rectifier to reach steady dc output. The start-up time of active diode in combination with the bypass diode is approximately 10% faster compared to that of the rectifier without bypass diode. After the active diode starts working, the bypass diode will turn off and always in a high-ohmic state since the output dc voltage is nearly equal to the input ac amplitude.

2.3 Comparator design

The key part of the active diode is the comparator. The power consumption of the comparator should be very low due to the fact that the comparator is supplied via the $V_{\text{out}}$ from the storage capacitor $C_s$. Thus, a large current consumption would strongly reduce the overall efficiency. Moreover, since this rectifier is mainly for low voltage energy harvesting applications with low output power and voltage, therefore the comparator should work at around 0.3V input voltage amplitude which is lower than the threshold voltage (around 0.4V) of the used process. The minimum input voltage amplitude of conventional gate input comparator is $\max(|V_{\text{thp}}| + V_{\text{dsn}} + V_{\text{ov}}, |V_{\text{thn}}| + V_{\text{dsp}})$ [19], where $V_{\text{ov}}$ is the over-dropout voltage of PMOS transistor. The voltages $|V_{\text{thp}}|$ and $V_{\text{thn}}$ are the threshold voltages of PMOS transistor and NMOS transistor, respectively. The voltages $|V_{\text{dsp}}|$ and $V_{\text{dsn}}$ are the dropout voltages of PMOS transistor and NMOS transistor, respectively [19]. Therefore, such comparator cannot meet the demand. Due to this, a body-input comparator is proposed in this work. The transistors of the proposed comparator are working in the subthreshold region and the drain current $I_D$ is given as [20]

$$I_D = I_{D0} \frac{W}{L} \exp\left(\frac{V_{GS} - V_{th}}{n \cdot V_T}\right). \quad (2)$$

Where $I_{D0}$ is a constant, $L$ is the effective channel length and $W$ is width, $V_{GS}$ is the gate-source voltage, $n$ is the subthreshold-slope coefficient, $V_T = kT/q$ is the thermodynamic voltage. The dependence of threshold voltage $V_{th}$ on the source-body voltage $V_{SB}$ is known from Eq. (1). Equation (1) is valid for strong inversion of the channel, but presents the influence of $V_{SB}$ to $V_{th}$. For weak inversion an exponential dependency of $I_D$ to the source-body voltage $V_{SB}$ can be seen [22]

$$I_D \propto \exp\left(\frac{V_{SB}}{V_T}\right). \quad (3)$$

The body effect on the drain current is usually undesirable in analog circuit design. However, in this work the body terminal is used as the input. Figure 5 has given the circuit implementation

![Fig. 5. The circuit diagram of active diode and comparator.](image-url)
of the proposed ultra-low voltage comparator. This comparator consists of three parts: bias circuit part (M11 and M12), body-input circuit part (M1~M4) and inverter output circuit part (M5~M10). Firstly, the bias circuit is very simple. The bias voltage is supplied by using two diode-connected NMOS transistors to divide the output dc voltage ($V_{out}$). No large value resistor and start-up circuit like in [18, 20] is needed and therefore it can reduce the area consumption. Moreover the bias circuit part in [18, 20] is a large power consumption part, which will take up approximately 25% of the total power loss for the rectifier [18, 20]. Comparing to it, more simple bias circuit in this work consumes much lower current (only around 1.5 nA at 0.7V input), which is important for enhancing the voltage and power efficiencies. The body input circuit part adopts the body inputs of two PMOS transistors to compare the $V_{nvc}$ and $V_{out}$ potential. The output circuit part uses three inverters to generate a digital output signal for controlling PMOS switch on or off. At the same time, in order to lower the voltage drop, the width of PMOS switch is large and the gate capacitance load is large, therefore the W/L ratios of M9 and M10 should be large enough to drive the PMOS switch. In addition, the capacitance load of the body-input part (M1~M4) is important for the switch speed of the comparator. In this work, the high switch speed can be achieved by the small W/L ratios of M5 and M6. Hence the W/L ratios is gradually increased in the three inverters part. Furthermore, it is clear that current flow only occurs during the switching phase and there is no static power consumption in the inverter output circuit part. The power consumption of the comparator is very low for keeping high power efficiency. Comparing to the power consumption of comparator in [18] (0.2μW at 475mV input voltage), the current consumption of comparator in this work is only around 0.2μA at 600mV supply, which leads to a power consumption of less than 0.15μW. It is clear that the comparator of this work at higher input voltage, however, have lower power consumption.

In addition, the mismatch simulations for the proposed comparator are very important, which can highlight offset voltage. Moreover, they can further affect the output voltage of rectifier. From [23], threshold voltage differences and current factor differences are two dominant mismatch sources for a matched pair of MOS transistors. We can also obtain assuming that the W/L sizes and threshold voltages of two input transistors M1 and M2 mismatch by 3% is reasonable for the proposed comparator in the 0.18um process. In this comparator, for typical 0.3V supply voltage when the W/L size of input transistor M1 mismatches with the W/L size of input transistor M2 by 3%, the offset voltage of the proposed comparator will change around 5mV. However, the output voltage of the rectifier will nearly not decrease. Similarly, when the threshold voltage of input transistor M1 mismatches with that of input transistor M2 by 3%, the output voltage of the rectifier will also decrease slightly (around 3.5%).

Fig. 6. Simulated waveforms of the rectifier at 0.3V input voltage with $\Delta t$.  

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2.4 Reverse current consideration
There will be reverse current from $V_{\text{out}}$ to $V_{\text{nvc}}$ if the PMOS switch is still on when $V_{\text{out}} > V_{\text{nvc}}$ and reverse current can severely degrade the power efficiency of the rectifier. As shown in Fig. 6, for the ultra-low input voltage 0.3V, when $V_{\text{nvc}}$ decreases and gets smaller than $V_{\text{out}}$, the gate voltage of PMOS switch does not change to high potential until a delay time $\Delta t$. It means PMOS switch is still on in the time interval $\Delta t$ and there will be reverse current, for $V_{\text{out}} > V_{\text{con}}$. In order to enhance the power efficiency, the reverse current should be reduced. In [15, 17, 19], they use unbalanced-biasing scheme to reduce the time delay. In this work, without requiring this scheme, the proposed rectifier can achieve nearly no reverse current for the low input voltage 0.3V, which is shown in Fig. 7. By adjusting the W/L ratios of M11 and M12, we can obtain an appropriate bias voltage ($V_{gs}$ voltage) for M3 and M4, then the proposed comparator can cut off the PMOS switch at the appropriate time and nearly no reverse current flows through the active diode. Since the time delay $\Delta t$ and therefore the reverse current exists in rectifier [18, 20], combining with higher voltage efficiency of proposed rectifier, the power efficiency of this work can achieve approximately 5% higher than that of the rectifier in [18] at 0.3V input voltage.

3. Simulation results
The circuit has been simulated with HSPICE using a standard 0.18μm CMOS process. Table I shows the transistor dimensions in the proposed rectifier. The default input voltage frequency of rectifier is 100Hz. Additionally, a capacitor of 8μF and a load of 40kΩ are used.

![Fig. 7. Simulated waveforms of the rectifier at 0.3V input voltage without the reverse current.](image)

![Fig. 8. Simulated waveforms under 0.28V input voltage.](image)
### Table I. The transistor sizes of proposed rectifier.

<table>
<thead>
<tr>
<th></th>
<th>Unit Size</th>
<th>Multiply Factor</th>
<th>Unit Size</th>
<th>Multiply Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP1</td>
<td>100μm/0.2μm</td>
<td>500</td>
<td>M2</td>
<td>9.0μm/0.2μm</td>
</tr>
<tr>
<td>MP2</td>
<td>100μm/0.2μm</td>
<td>500</td>
<td>M3</td>
<td>2.3μm/0.2μm</td>
</tr>
<tr>
<td>MN1</td>
<td>100μm/0.2μm</td>
<td>500</td>
<td>M4</td>
<td>2.3μm/0.2μm</td>
</tr>
<tr>
<td>MN2</td>
<td>100μm/0.2μm</td>
<td>500</td>
<td>M5</td>
<td>3.0μm/0.18μm</td>
</tr>
<tr>
<td>PMOS Switch</td>
<td>100μm/0.2μm</td>
<td>600</td>
<td>M6</td>
<td>1.2μm/0.18μm</td>
</tr>
<tr>
<td>PMOS Diode</td>
<td>100μm/0.2μm</td>
<td>680</td>
<td>M7</td>
<td>9.0μm/0.18μm</td>
</tr>
<tr>
<td>M11</td>
<td>0.22μm/0.2μm</td>
<td>1</td>
<td>M8</td>
<td>3.6μm/0.18μm</td>
</tr>
<tr>
<td>M12</td>
<td>0.22μm/60.0μm</td>
<td>1</td>
<td>M9</td>
<td>27.0μm/0.18μm</td>
</tr>
<tr>
<td>M1</td>
<td>9.0μm/0.18μm</td>
<td>1</td>
<td>M10</td>
<td>10.8μm/0.18μm</td>
</tr>
</tbody>
</table>

### 3.1 Minimum input voltage and voltage conversion efficiency

The minimum operating voltage with acceptable voltage efficiency is very important for energy harvesting applications. Figure 8 shows the simulated output voltage, which indicates that the proposed rectifier can work at minimum input voltage of 0.28V and provides a voltage efficiency of approximately 78%. Note that the reverse current (the delay time $\Delta t$) exists for the ultra-low input voltage 0.28V, which results in not very smooth between 200mV and 140mV in the decreasing curve of $V_{nvc}$ (as shown in Fig. 8). When the input voltage is lower than this minimum operating voltage, the rectifier can also work. However, the efficiency will be lower and becomes unsatisfactory.

The voltage efficiency $\eta_v$ is defined as the fraction of the output dc voltage $\hat{V}_{out}$ and the input voltage amplitude $\hat{V}_{in}$, which is shown in Eq. (4).

$$\eta_v = \frac{\hat{V}_{out}}{\hat{V}_{in}} \cdot 100\%.$$  \hspace{1cm} \text{(4)}

![Fig. 9. Output voltage efficiency versus input voltage amplitude.](image_url)

![Fig. 10. Output power efficiency versus input voltage amplitude.](image_url)
Figure 9 further shows the voltage efficiency versus different input voltage amplitude using different ohmic loads. With larger load resistor the output voltage efficiency of the rectifier will be higher since a larger discharge time cycle is needed. The voltage efficiency can increase to a peak value of over 96% with the 40kΩ load.

### 3.2 Power efficiency

The power efficiency of the rectifier is defined using Eq. (5).

\[
\eta_p = \frac{1}{T} \int_{t}^{t+T} V_{out}(t) \cdot i_{out}(t) dt \cdot \frac{1}{T} \int_{t}^{t+T} V_{in}(t) \cdot i_{in}(t) dt \cdot 100\%.
\]

The power efficiency versus different input voltage amplitude using different load resistors is shown in Fig. 10. There is an inflexion voltage (around 0.38V) in the power efficiency curve. When input voltage is lower than this voltage, the larger the load is, the higher the power efficiency is. Since the larger load can achieve the higher output voltage in this region (as shown in Fig. 9). While in higher input voltage region, since the output voltages for different loads are at the same level (as shown in Fig. 9), the output current will lower with larger load and the proportion of current consumption of the active diode taking up the output load current will be larger with large load than that with light load. Therefore the lighter load can achieve higher power efficiency in this region. Moreover, the proposed active rectifier has a power efficiency of over 87% starting from 0.3V input voltage with the 40kΩ load. As the input voltage amplitude further increases over 1.0V, the body leakage current of the input transistor M1 of the proposed comparator will not be neglected and power efficiency will further decrease.

### 3.3 Maximum working frequency

Most vibration-powered energy harvesting generators work between 10Hz and 1000Hz \[16\]. Figure 11 shows the voltage efficiency versus input voltage amplitude for different input frequencies. The load capacitor is adapted for the applied frequency. The voltage efficiencies at the input voltage frequencies 10Hz and 100Hz are nearly the same, which are higher than that at the input voltage frequency 3kHz. Since higher frequency will result in more power loss in the large size transistors of negative voltage converter (MP1~MN2) and PMOS switch. The maximum input voltage working frequency of this rectifier with high efficiency is around 3kHz and it is sufficient for the most energy harvesting applications.

### 3.4 Performance in different process corners

The proposed rectifier has been simulated when the process corners are the typical (TT), fast (FF) and slow (SS) of 0.18μm CMOS technology, respectively. The minimum operating voltage in SS...
Table II. Performance comparisons between rectifiers.

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>Technology</td>
<td>0.18 μm CMOS</td>
<td>0.35 μm Low V_{th} CMOS</td>
<td>0.18 μm CMOS</td>
</tr>
<tr>
<td>$V_{in}$</td>
<td>0.7V-1.8V</td>
<td>0.45V-0.6V</td>
<td>0.3V-0.7V</td>
</tr>
<tr>
<td>$V_{out}/V_{in}$</td>
<td>$&gt;82%$ (RL=500Ω)</td>
<td>$&gt;90%$ (RL=50kΩ)</td>
<td>$&gt;88%$ (RL=40kΩ)</td>
</tr>
<tr>
<td>Power Efficiency</td>
<td>81.8%-87%</td>
<td>90% at 0.5V</td>
<td>$&gt;87%$</td>
</tr>
<tr>
<td>Frequency</td>
<td>20Hz-1.5MHz</td>
<td>~ around 5kHz</td>
<td>10Hz-3kHz</td>
</tr>
</tbody>
</table>

Process corner is around 0.35V for the approximately 0.07V higher threshold voltage in SS than that in TT process corner.

3.5 Performance comparisons

The performance comparisons of this work with other previously reported rectifiers are shown in Table II. Note that all the results of the [17–19] and the proposed work in the Table II are from simulation. From published papers and the Table, rectifiers in [15, 17–20] can work in the low frequency like 100Hz. However, the minimum input voltage amplitude is 1.2V in [15] and 0.7V in [17, 19] respectively, which are not suitable for the ultra-low voltage energy harvesting systems. Only the rectifier in [18, 20] and the proposed rectifier can work in the ultra-low voltage by using body input comparator. In Fig. 12 and Fig. 13, the detailed comparisons of the active rectifier in [18] and this work in terms of output voltage efficiency as well as power efficiency are given to demonstrate the good performances of the proposed circuit.

From Table II, the technology process in [18] is not same as that in this work. Therefore, for comparing with the rectifier in [18] fairly, we have simulated the two rectifiers in the same 0.18um CMOS technology process. In the comparisons, both the two rectifiers are simulated in the same capacitor of 8μF and resistor load of 40kΩ. Additionally, they also have the same sizes of PMOS.

![Fig. 12. Output voltage efficiency versus input voltage amplitude in this work and the rectifier in [18].](image1)

![Fig. 13. Output power efficiency versus input voltage amplitude in this work and the rectifier in [18].](image2)
transistors and NMOS transistors in the negative voltage converter part and PMOS switch part which are related to the voltage drop. The output voltage efficiency comparison versus different input voltage amplitude is shown in Fig. 12.

From Fig. 12, when the input voltage is between 0.3V and 0.75V, both the proposed rectifier and the rectifier in [18] have the high voltage efficiency of more than 80%. They can also achieve the peak voltage efficiency of around 97%. Moreover, it is clear that the voltage efficiency of the proposed rectifier is higher than that of the rectifier in [18] except for the input voltage around 0.4V. Therefore, we can divide our discussion into two parts. Firstly, when the input voltage is in the low input voltage region (between 0.28V and 0.4V), this work has a better performance. Since the proposed body bias technique can achieve the lower voltage drop, which is important for enhancing the voltage efficiency in the low input region. At the same time, the time delay (as shown in Fig. 6) exists in the low input voltage region. Comparing to the rectifier in [18, 20], this work can achieve much less time delay and much less reverse current, which further enhances the voltage efficiency. For the high input region (between 0.4V and 0.75V), more simple bias circuit in the proposed comparator and therefore less current consumption from the capacitor load can achieve higher voltage efficiency. As a matter of fact, the bias circuit of the comparator in [18, 20] is a large power consumption part, which will take up approximately 25% of the total power loss for the rectifier [18, 20]. The proposed rectifier achieves approximately 5% higher output voltage efficiency than the rectifier in [18] at 0.28V input voltage and 2% higher output voltage efficiency at 0.7V input voltage. The output power efficiency comparison versus different input voltage amplitude is given in Fig. 13.

For the power efficiency comparison, similar with the voltage efficiency comparison, both the two rectifiers can achieve over 80% high power efficiency for the input voltage between 0.3V and 0.7V and they can also achieve the peak power efficiency of 95% at the input voltage around 0.4V. The power efficiency will decrease in the low input voltage region (between 0.28V and 0.4V) for the low voltage efficiency (as shown in Fig. 12). Similarly, the power efficiency will also reduce in the high input voltage region (between 0.4V and 0.7V), which is due to the fact that the power consumption of comparator (including the body leakage current of the input transistor M1) will become more and more important comparing to the output power in the high input voltage region. Moreover, we can also divide the power efficiency comparisons of the two rectifiers into two parts and the detailed reasons are similar with that for voltage efficiency comparisons. The proposed rectifier achieves approximately 7% higher output power efficiency than the rectifier in [18] at 0.28V input voltage and 3% higher output power efficiency at 0.7V input voltage.

4. Conclusions
In this paper, a sub-0.3V CMOS active rectifier for energy harvesting applications is presented. The active rectifier is well suited for the input voltage amplitude as low as 0.28V by using a body-input comparator and body bias technique. Additionally, the proposed rectifier can achieve nearly no reverse current and has a simple bias circuit in the comparator part, which are important for enhancing the voltage and power efficiency. The proposed active rectifier can achieve the peak voltage efficiency of over 96% and the maximum power efficiency of approximately 94%.

References


