A CMOS circuit for PWM-mode nonlinear transformation robust to device mismatches to implement coupled map lattice models

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Abstract: In order to develop large-scale nonlinear dynamical systems using CMOS integrated circuits, we propose a core circuit for coupled map lattice (CML) models. The characteristics of the core circuits in the lattice on a chip are not generally equal, which is caused by CMOS device mismatches, including parasitic capacitance and wiring resistance. The proposed circuit solves this problem; it compensates for a DC offset voltage variation by holding it at a capacitor, and also for current variation by adjusting the bias voltage of a current source automatically so as to bring the current close to a target value. The proposed core circuit has been designed and fabricated using TSMC 0.25 μm CMOS technology. The measurement results using the fabricated circuit have shown that the bit precision is more than 8 bits, even if there is a DC offset voltage of 100 mV or a bias-voltage change of 100 mV in a switched current source.

Key Words: coupled map lattice, CMOS, device mismatch, spatiotemporal pattern, pulse width modulation

1. Introduction
Some coupled nonlinear dynamical models, known as coupled map lattice (CML) models, have been proposed [1–5]. The threshold coupled map [6] is a simple example of these models, but shows various spatiotemporal patterns. Although these models are generally evaluated by numerical simulation, there are few examples of CMOS circuit implementation. Therefore, our final goal is to design a CMOS circuit for CML.

We have already proposed a voltage- and a current-waveform-sampling-mode (VWSM and CWSM)
circuit that can achieve arbitrary analog nonlinear dynamics in the time domain using pulse width/phase modulation (PWM/PPM) signals [7, 8]. However, the characteristics of core circuits in the lattice on a chip are not generally equal, due to CMOS device mismatches, including parasitic capacitance and wiring resistance. The VWSM circuit is robust to such device mismatches, while the CWSM circuit easily achieves weighted summation. These advantages are important for developing a large-scale coupled array circuit.

In this paper, we propose a CMOS core circuit that can implement a threshold coupled map model, and experimentally show that the circuit achieves accurate analog nonlinear transformation even if a DC voltage offset and current variation exist.

This paper is organized as follows. In Section 2, we explain a threshold coupled map model, and in Section 3, the principle of the VWSM circuit and the SCS. Operation of the proposed circuit is explained in Section 4. We show measurement results of a fabricated circuit in Section 5, and conclude this paper in Section 6.

2. Nonlinear dynamical model with threshold coupled map

A threshold coupled map model with a one-dimensional unidirectional coupling is shown in Fig. 1(a) [6]. This model performs the following nonlinear transformation:

\[ x_i(n) = f(x_i(n - 1)), \]

where \( x_i(n) \) is the state variable on lattice site \( i \) at time step \( n \), and \( f(\cdot) \) is a nonlinear transformation function such as a logistic or circle map [9]. If \( x_i(n) > x_{th} \), the excess \( \delta_i(n) = x_i(n) - x_{th} \) is transported to the neighboring lattice sites as follows:

\[ x_i(n) \rightarrow x_{th}, \]
\[ x_{i+1}(n) \rightarrow x_{i+1}(n) + \delta_i(n). \]

It is noted that \( n \) increases only when \( x \) is mapped. This model has several updating schemes [10, 11], and for each of them, we can obtain various spatiotemporal patterns. We can extend the model to a two-dimensional (2-D) lattice with four-nearest-neighbor couplings as shown in Fig. 1(b). When the coupling is mutual, excess \( \delta \) are transported as follows:

\[ x_{i,j}(n) \rightarrow x_{th} + g\delta_{sum}(n) \quad \text{if} \quad x_{th} < x_{i,j}(n), \]
\[ x_{i,j}(n) \rightarrow x_{i,j}(n) + g\delta_{sum}(n) \quad \text{if} \quad x_{th} \geq x_{i,j}(n), \]

where \( (i, j) \) is the site index in the 2-D lattice, \( g \) is a coupling weight, and \( \delta_{sum} \) is the summation of \( \delta \) from the neighboring sites.

3. Circuit principles

3.1 Voltage waveform sampling for nonlinear transformation

Figure 2(a) shows the principle of VWSM nonlinear transformation using PWM signals. This sampling mode can achieve the dynamics shown in Eq. (1). State-variable voltage \( V_{in}(n) \) (\( \propto x(n) \)) at time step \( n \) is transformed into a PWM signal with a pulse width \( T_{in}(n) \) (\( \propto V_{in}(n) \)). This transformation can be achieved by comparing \( V_{in}(n) \) with ramped reference voltage \( V_{rmp}(t) \), as shown in Fig. 2(a). Nonlinear voltage waveform \( V_{non}(t) \) is sampled with this PWM signal, which is given by

\[ V_c = V_{non}(T_{in}(n)), \]

where \( V_c \) is the voltage that is sampled to capacitor \( C \). Arbitrary discrete-time analog nonlinear dynamics can be achieved by considering \( V_c \) as \( V_{in}(n + 1) \) at the next time step \( (n + 1) \).

3.2 Switched current source (SCS) for pulse-voltage conversion and integration/summation

Figure 2(b) illustrates the principle of pulse-to-voltage conversion. In order to convert the pulse-width of a PWM signal into a voltage, a current is integrated over time by capacitor \( C \). When
switched current sources (SCSs) are turned on by PWM signals $S_1, S_2, \ldots, S_h$ with a pulse width of $T_1, T_2, \ldots, T_h$, respectively, capacitor voltage $V_c$ is given by

$$V_c = \frac{1}{C} \sum_{r=1}^{h} T_r I_r(V_B) + V_0,$$

where $V_B$ is the gate voltage of p-type MOSFETs acting as current sources, $I_r(\cdot)$, is the voltage-current conversion function of the $r$th p-type MOSFET, and $V_0$ is the initial voltage of capacitor $C$. It is noted that each p-type MOSFET biased by $V_B$ operates at the saturation region in order to supply a constant current. As shown in Eq. (5), a simple configuration connecting SCSs to a capacitor achieves summation. Therefore, SCSs can be used to realize summation about $\delta$ shown in Eq. (3). Connection weight $g$ can be varied by changing $V_B$ or $C$.

### 3.3 Variation issues

A CMOS circuit for CML with the architecture shown in Fig. 1(b) can be constructed using a VWSM nonlinear transformation circuit and SCSs. VWSM circuits in all core circuits can share a single nonlinear voltage waveform $V_{non}$ as shown in Fig. 3. However, the characteristics of a core circuit are not generally equal to those of the other core circuits. In the VWSM, voltage difference $V_{os}$ between the base-voltage of $V_{rmp}(t)$ and that of $V_{non}(t)$ creates a DC voltage offset, and $V_{os}$ is converted into an offset pulse width when a state-variable voltage is converted into a PWM signal. The DC offset voltage $V_{os}$ is caused by the voltage shift variation of analog buffers, wiring resistance, etc., as shown in Fig. 3.

Regarding the SCSs shown in Eq. (5), function $I_r(\cdot)$ and capacitance $C$ are varied by threshold voltage variation of MOSFETs and parasitic capacitance, respectively. Therefore, $g$ shown in Eq. (3) also has variation.
4. Proposed circuit

Our proposed core circuit is shown in Fig. 4. This circuit includes source-follower analog buffers $S_{F_{\text{non}}}$, $S_{F_{\text{rmp}}}$, $S_{F_X}$, and $S_{F_{\text{iniA}}}$, a comparator CMP robust to $V_{os}$ variation, a capacitor $C_x$ that is used
in voltage sampling with PWM signals, an SCS, and a current/capacitance-variation compensation (CCC) circuit. The circuit achieves nonlinear transformation robust to $V_{os}$ variation generated from the analog buffers SF$_{non}$, SF$_{rmp}$, SF$_x$, and wiring resistance. The CCC circuit adjusts the gate voltage of M$_\delta$ in SCS, $V_{cc}$, so that CMP can output a PWM signal with target pulse width $T_{tgt}$ when S$_\delta$ is turned on during time span $T_\delta$. The PWM signal with pulse width $T_{tgt}$ is given as signal S$_{cc}$.

### 4.1 Operation of nonlinear transformation circuit robust to device variations

Figure 5 shows a timing diagram of control signals and voltages for nonlinear transformation in the proposed core circuit. In the nonlinear transformation operation, S$_{iniA}$ is kept at “ON” in order to fix the voltage at node P$_{st}$ to $V_{iniA}$. We define $V_{rmp,bt}$ and $V_{non,bt}$ as base voltages of $V_{rmp}$ and $V_{non}$ at the output stages of analog buffers SF$_{rmp}$ and SF$_x$. Here, in the initial condition, we define $V_{x0}$ as the output voltage of SF$_x$, which is an initial state-variable voltage.

1) When S$_{set}$ and S$_x$ are turned on, nodes P$_{st}$ and P$_{cmp}$ are set at $V_{x0}$ and the threshold voltage of the first-stage inverter in CMP, $V_{inv,th}$, respectively.

2) After S$_{set}$ is turned off, and S$_{non}$ is turned on, then node P$_{st}$ is varied from $V_{x0}$ to $V_{non,bt}$. At the same time, node P$_{cmp}$ is varied from $V_{inv,th}$ to ($V_{inv,th} - |V_{x0} - V_{non,bt}|$). Capacitor $C_{DC}$ holds the voltage difference ($V_{rmp,bt} - V_{non,bt}$) in this step.

3) S$_{non}$ and S$_x$ are turned off. The voltage difference ($V_{inv,th} - |V_{x0} - V_{non,bt}|$) at node P$_{cmp}$ is transformed into a PWM signal. This transformation can be achieved by comparing ($V_{inv,th} - |V_{x0} - V_{non,bt}|$) with ramped reference voltage $V_{rmp}(t)$. Nonlinear voltage waveform $V_{non}(t)$ is sampled and the resultant voltage is stored at $C_x$ by S$_{out}$, as shown in Fig. 5.

### 4.2 Operation of CCC

Figure 6 shows a timing diagram of control signals and node voltages for CCC operation. The gate voltage of M$_\delta$, $V_{cc}$, shown in Fig. 4 is adjusted in order to minimize the difference of the pulse width between the target pulse width $T_{tgt}$ and $T_{inv,\delta}$, which is defined as the time width of the PWM signal output from node S$_{inv}$ corresponding to voltage $V_{\delta}$. Here, $V_{\delta}$ is the voltage difference at node P$_{\delta}$ shifted by charging up $C_{\delta}$ during $T_{\delta}$, which is the pulse width of the PWM signal S$_\delta$. Waveform $V_{non}(t)$ is fixed at base voltage $V_{non,bt}$ during the current compensation operation, and the initial voltage of $V_{cc}$ is set at $V_{iniB}$. Voltage $V_{cc}$ is adjusted by transistor M$_{cc}$ acting as a current source, and its current value is determined by $V_{cmp}$. The current compensation operation is as follows:

1) S$_{set}$, S$_{non}$, S$_x$, and S$_{iniA}$ are turned on in order to initialize nodes P$_{cmp}$, P$_x$, P$_{st}$, and P$_{\delta}$, respectively.

2) After S$_{iniA}$ and S$_{non}$ are turned off, S$_{\delta}$ is turned on during pulse width $T_{\delta}$. Nodes P$_{\delta}$, P$_x$, and P$_{st}$ are shifted up by $V_{\delta}$.

3) After S$_{set}$ is again turned off, S$_{non}$ is turned on. Node P$_{cmp}$ is shifted down by $V_{\delta}$.

4) After S$_x$ is turned off, S$_{iniA}$ is again turned on. Then, $V_{rmp}(t)$ is increased linearly. Comparator CMP generates an inverted PWM signal during time width $T_{inv,\delta}$ corresponding to $V_{\delta}$. Capacitor $C_{cc}$ is charged up by feed back PWM signal S$_{fb}$, with pulse width ($T_{inv,\delta} - T_{tgt}$).

5) Steps 1) to 4) are repeated until ($T_{inv,\delta} - T_{tgt}$) is minimized.

Here, since the circuit shown in Fig. 4 only has a current source for charging up $V_{cc}$, the initial voltage of $V_{cc}$, $V_{iniB}$, must be set sufficiently low.

### 4.3 LSI circuit design

We designed and fabricated a CMOS circuit using TSMC 0.25 μm (1-Poly, 5-Metal) CMOS technology. The layout result and a microphotograph are shown in Figs. 7 (a) and (b), respectively; the specifications of the fabricated core circuit are shown in Table I. The capacitance values were designed
as follows: $C_{DC} = C_{inv} = 0.225 \, \text{pF}$, $C_x = 0.1 \, \text{pF}$, $C_\delta = 2.0 \, \text{pF}$, and $C_{cc} = 0.5 \, \text{pF}$. The core circuit has four SCSs for coupling with four-nearest-neighbor cores, and includes four capacitors $C_{cc}$ in order to compensate the SCSs as shown in Figs. 7 (a). All bias voltages are supplied externally.

5. Measurement and evaluation results

5.1 Definition of bit precision

We define the following bit precision for input-output characteristics of the comparator and nonlinear transformation characteristics:
Fig. 6. Timing diagram of control signals and node voltages for CCC.

Fig. 7. Circuit design result: (a) layout, and (b) microphotograph. Squares surrounded by white lines in panel (a) implement capacitors.

\[
\text{(Bit precision)} = \log_2 \frac{T_{\text{max}}}{\sigma_{\text{fit}}} \quad \text{[bits]},
\]

where \(T_{\text{max}}\) is the maximum value of \(T_{\text{out}}\), and \(\sigma_{\text{fit}}\) is the standard deviation obtained from a fitting function. The fitting function is obtained from a return-map made from time-series data using a least squares method.

The bit precision of the CCC circuit was defined using standard deviation \(\sigma_{cc}\) of time average \(\langle T_{\text{out}} \rangle\)
5.2 Input-output characteristics of proposed comparator

We measured the input-output characteristics of the proposed comparator. We define $V_{non,bt0}$ and $V_{rmp,bt0}$ as the base voltages of $V_{non}$ and $V_{rmp}$ before $SF_{non}$ and $SF_{rmp}$, respectively. We set $V_{rmp}(t) = 0.414 \times 10^6 t + V_{rmp,bt0}$ [V], $V_{rmp,bt0} = 1.6$ [V], and $V_{invA} = 1.0$ [V]. In order to show the robustness to DC offset voltage variation, $V_{non,bt0}$ was varied as follows: $V_{non,bt0} = 1.6, 1.65, 1.7$ [V]; corresponding to $V_{os} = 0.0, 0.05, 0.1$ [V], respectively, and $V_{non}$ was set to a rectangular wave. We changed the amplitude of $V_{non}$ in the range of $[0.05, 0.85]$ V in steps of $0.05$ V, and measured ten sequential PWM signals of $S_{out}$ in each amplitude.

Figure 8 shows the input-output characteristics of the comparator when $V_{os}$ was varied. They were almost the same in all cases, and were fitted by a linear equation: $T_{out} = kV_{non} + a$. The fitting results are shown in Table II. The difference between $a$ when $V_{os} = 0.0$ V and $a$ when $V_{os} = 0.1$ V was $2.7$ ns, which corresponds to $V_{os}$ variation of $1.0$ mV, if we assume that $T_{out} = 2,630$ ns when the amplitude of $V_{non}$ is $1$ V. The bit precisions shown in Table II are more than $9$ bits in all cases.

\[
\text{(Bit precision)} = \log_2 \left( \frac{T_{\text{max}}}{|\sigma_{cc}| + |\Delta_{tgt}|} \right) [\text{bits}]. \tag{7}
\]

Table II. Fitting results of Fig. 8.

<table>
<thead>
<tr>
<th>$V_{os}$ [V]</th>
<th>0.0</th>
<th>0.05</th>
<th>0.1</th>
</tr>
</thead>
<tbody>
<tr>
<td>$k$ [ns/V]</td>
<td>2651.3</td>
<td>2656.4</td>
<td>2649.1</td>
</tr>
<tr>
<td>$a$ [ns]</td>
<td>9.7</td>
<td>8.7</td>
<td>12.4</td>
</tr>
</tbody>
</table>

Table III. Fitting results for obtained return maps.

<table>
<thead>
<tr>
<th>$V_{os}$ [V]</th>
<th>0.0</th>
<th>0.05</th>
<th>0.1</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\langle q_c \rangle$ [1/μs]</td>
<td>$-1.466 \pm 0.001$</td>
<td>$-1.467 \pm 0.001$</td>
<td>$-1.466 \pm 0.001$</td>
</tr>
<tr>
<td>$\langle k_c \rangle$ [1/s]</td>
<td>$3.944 \pm 0.004$</td>
<td>$3.945 \pm 0.003$</td>
<td>$3.942 \pm 0.002$</td>
</tr>
<tr>
<td>$\langle a_c \rangle$ [ns]</td>
<td>$-22.0 \pm 3.0$</td>
<td>$-21.8 \pm 2.0$</td>
<td>$-20.0 \pm 2.0$</td>
</tr>
<tr>
<td>(Bit precision) [bits]</td>
<td>$8.85 \pm 0.14$</td>
<td>$8.89 \pm 0.17$</td>
<td>$8.93 \pm 0.12$</td>
</tr>
</tbody>
</table>

and the difference $\Delta_{tgt}$ between $T_{tgt}$ and $\langle T_{out} \rangle$ as follows:

\[
\text{(Bit precision)} = \log_2 \left( \frac{T_{\text{max}}}{|\sigma_{cc}| + |\Delta_{tgt}|} \right) [\text{bits}]. \tag{7}
\]

In this paper, we set $T_{\text{max}}$ to 2,630 ns.
5.3 Nonlinear transformation

We used the same waveform of $V_{rmp}(t)$ as in the previous subsection, where $V_{rmp,0}$ was fixed to 0.6 V, and $V_{non}(t) = 1.385 \times 10^6(1 - 0.38 \times 10^6t) + V_{non,0}$ [V]. We measured time-series data of $T_{out}$ when $V_{non,0}$ was 1.6, 1.65, and 1.7 V, which meant that $V_{os} = 0.0, 0.05, 0.1$ V, respectively. Figure 9 shows the voltage waveforms of $V_{rmp}, V_{non}, V_x,$ and $S_{out}$ during nonlinear transformation.

Figure 10 shows return-maps when $V_{os}$ was changed; they are almost identical in all cases. We fitted 10 return maps to $T_{out}(n+1) = q_c T_{out}(n)^2 + k_c T_{out}(n) + a_c$, and calculated the bit precision. Table III shows the averages of $q_c, k_c, a_c$, and bit precision; coefficients $q_c, k_c, a_c$ were almost the same in all cases. The maximum change in $a_c$ was 2 ns, and the bit precision was more than 8.8 bits in all cases.
Table IV. Pulse width $T_{\text{out}}$ of $S_{\text{out}}$ for different $V_{\text{iniB}}$.

<table>
<thead>
<tr>
<th>$V_{\text{iniB}}$ [V]</th>
<th>1.35</th>
<th>1.4</th>
<th>1.45</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\langle T_{\text{out}} \rangle$ [ns]</td>
<td>596.9 ± 2.6</td>
<td>596.6 ± 2.2</td>
<td>595.4 ± 2.6</td>
</tr>
<tr>
<td>$\Delta_{\text{tgt}}$ [ns]</td>
<td>-3.1</td>
<td>-3.4</td>
<td>-4.6</td>
</tr>
<tr>
<td>Bit precision [bits]</td>
<td>8.85</td>
<td>8.88</td>
<td>8.51</td>
</tr>
</tbody>
</table>

Table V. Pulse width $T_{\text{out}}$ of $S_{\text{out}}$ for different $V_{\text{cmp}}$.

<table>
<thead>
<tr>
<th>$V_{\text{cmp}}$ [V]</th>
<th>1.95</th>
<th>2.0</th>
<th>2.05</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\langle T_{\text{out}} \rangle$ [ns]</td>
<td>595.1 ± 3.3</td>
<td>595.4 ± 2.6</td>
<td>596.3 ± 3.8</td>
</tr>
<tr>
<td>$\Delta_{\text{tgt}}$ [ns]</td>
<td>-4.9</td>
<td>-4.6</td>
<td>-3.7</td>
</tr>
<tr>
<td>Bit precision [bits]</td>
<td>8.33</td>
<td>8.51</td>
<td>8.45</td>
</tr>
</tbody>
</table>

Table VI. Pulse width $T_{\text{out}}$ of $S_{\text{out}}$ for different $T_{\text{tgt}}$.

<table>
<thead>
<tr>
<th>$T_{\text{tgt}}$ [ns]</th>
<th>520</th>
<th>560</th>
<th>600</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\langle T_{\text{out}} \rangle$ [ns]</td>
<td>516.2 ± 2.6</td>
<td>556.4 ± 2.2</td>
<td>595.4 ± 2.6</td>
</tr>
<tr>
<td>$\Delta_{\text{tgt}}$ [ns]</td>
<td>-3.8</td>
<td>-3.6</td>
<td>-4.6</td>
</tr>
<tr>
<td>Bit precision [bits]</td>
<td>8.68</td>
<td>8.82</td>
<td>8.51</td>
</tr>
</tbody>
</table>

Fig. 11. Voltage waveforms $V_x$, $S_{cc}$, and $S_{out}$ for CCC operation, where $V_{\text{iniB}}=1.4$ V, $V_{\text{cmp}}=1.95$ V, $T_{\delta}=600$ ns, and $T_{\text{tgt}}=600$ ns. Voltages charged up during $T_{\delta}$ are represented by $V_{\delta,1}$, $V_{\delta,2}$, and $V_{\delta,3}$.

5.4 CCC circuit

We used the same waveform of $V_{\text{rmp}}(t)$ and the same values of $V_{\text{rmp},0}$ and $V_{\text{iniA}}$, as in the previous subsection, and $V_{\text{non}}=V_{\text{non},0}=1.6$ [V]. We measured $T_{\text{out}}$ at each updating $V_{cc}$. Initial voltage $V_{\text{iniB}}$, gate voltage $V_{\text{cmp}}$ of transistor $M_{cc}$, and $T_{\text{tgt}}$ were varied as follows: $V_{\text{iniB}}=1.35$, 1.4, 1.45 V; $V_{\text{cmp}}=1.95$, 2.0, 2.05 V; $T_{\text{tgt}}=520$, 560, 600 ns. We defined $m$ as the update time step on $V_{cc}$. Figure 11 shows voltage waveforms of $V_x$ at node $P_x$, $S_{cc}$, and $S_{out}$ during the compensation operation. Charged up voltage value $V_{\delta,m}$ at time step $m$ is represented by $V_{\delta}$, and it decreased as $V_{\delta,1}$, $V_{\delta,2}$, and $V_{\delta,3}$.

Time series of $T_{\text{out}}$ are shown in Fig. 12. Figures 12 (a), (b), and (c) show the changes in $T_{\text{out}}$ when $V_{\text{iniB}}$, $V_{\text{cmp}}$, and $T_{\text{tgt}}$ were changed, respectively. Output pulse width $T_{\text{out}}$ converged on $T_{\text{tgt}}$ in all cases. These results show that the CCC circuit compensates the V-I conversion characteristic variation of $M_{\delta}$, and that we can set connection weight $g$ arbitrarily using the CCC circuit. Here, it
Fig. 12. Time series data $T_{\text{out}}$ obtained from fabricated LSI chip for CCC operation: (a) $V_{\text{cmp}} = 2.0\,\text{V}$ and $T_{\text{tgt}} = 600\,\text{ns}$; (b) $V_{\text{ini}B} = 1.4\,\text{V}$ and $T_{\text{tgt}} = 600\,\text{ns}$; and (c) $V_{\text{ini}B} = 1.4\,\text{V}$ and $V_{\text{cmp}} = 2.0\,\text{V}$.

should be noted that $T_{\text{tgt}}$ is smaller than $T_\delta$.

We calculated the average of $T_{\text{out}}$, $\langle T_{\text{out}} \rangle$, its bit precision, and the difference $\Delta_{\text{tgt}}$ between $\langle T_{\text{out}} \rangle$ and $T_{\text{tgt}}$. The averages $\langle T_{\text{out}} \rangle$ are calculated within the range $40 \leq m \leq 59$. The calculation results
are shown in Tables IV, V, and VI. The bit precisions were more than 8 bits in all cases.

6. Conclusions

We proposed a core circuit to implement a coupled map lattice (CML) circuit using CMOS technology. The core circuit includes a new comparator robust to DC offset voltage variation and a circuit for current and capacitance variation compensation. The bit precision evaluated using the fabricated circuit was more than 8 bits, even with a DC offset voltage of 100 mV and a change of 100 mV in the bias voltage of the current source for weight summation. The circuit for current and capacitance variation compensation achieves variation-compensation and connection-weight-setting operations simultaneously. A large-scale hardware CML system robust to device mismatches in a CMOS LSI can be constructed by arranging the proposed core circuit.

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