Possible Origins and Some Methods to Minimize LER

Munirathna Padmanaban, David Rentkiewicz, Chisun Hong,
Dongkwan Lee, Dalil Rahman, Raj Sakamuri and Ralph R. Dammel

AZ Electronic Materials USA Corp.
70 Meister Avenue, Somerville, NJ 08876, USA

Munirathna.padamanban@az-em.com

Line-edge roughness (LER) & line-width roughness (LWR) poses serious problems for the device performance and CD error budget for sub 100nm design rules. Illumination conditions, pitch, resist formulations, resist process conditions, substrates have shown to be the possible origins of LER. With in the resist formulations, polymer composition, dissolution characteristics of polymer during the development process, acid diffusion influence the roughness of the resulting patterns. ITRS (2003) roadmap requires LWR of 2nm (3 sigma) for 65nm DRAM half-pitch for 2007 year of production. Resist formulation optimization can minimize LER but this can not be achievable simply by the resist formulation modifications as the radius of gyration of polymers itself is in the order of 2-5 nm. It is therefore important to study (1) device performance compromises if the required 2nm is not achieved (2) methods to improve the LER after patterning (litho). As for methods to improve the LER after patterning viability of use of rinse solutions, hard bake, RELACS process and some etch process are reported. Possible origins of LER and some attempts to minimize the LER after patterning such as hard bake and RELACS™ process are discussed.

Keywords: LER, origins, 193nm formulations, hard bake, RELACS™ process.

1. Introduction

Line edge roughness (LER) is defined as the non-uniform deviation of the edge width (CD) along the length (either side) of the resist lines. Fluctuation of the CD width along the length of the resist line is called line width roughness (LWR) (Fig 1). LER and LWR are critical issues because they ultimately affect the device performance.¹⁻⁴ Device characteristics such as leakage current, threshold voltage and on-off current variation are reported to be affected due to LWR¹. Yamaguchi et al.² explain the transistor performance and threshold voltage variation due to long-period LER driven transistor width fluctuations. In MOSFET devices with a gate length of 50nm, the off-state leakage (I_{off}) increased with an LER of 9 nm.³ Diaz et al.⁴ report that a reduction of LER from 9.3 nm to 6.5 nm translated in to 1.5 times improvement in leakage current for a 0.13μm CMOS technology.

Fig. 1 Schematic representation of LER and LWR

Due for these reasons and also considering the CD error budget, International Technology Roadmap for Semiconductors (ITRS 2003 edition) requires LER to

be 2 nm for a 65 nm half-pitch scheduled to go production in year 2007 and beyond. It warrants LER of 1 nm for 32nm node technology. When translated in to molecular size, a 1 nm LER corresponds to roughly

Table 1. 2003 ITRS LER roadmap requirements converted to molecular size

Year of production	2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
Node	130 nm	115 nm	100 nm	90 nm	80 nm	70 nm	65 nm	45 nm	32 nm	22 nm
LER (nm, 3 sigma)	7	6	5	4	4	3	3	2	1	1
Monomer units	8	7	6	4	4	3	2	2	1	1

2. Origins of LER and LWR

Many theories have been proposed to explain the origins of LER/LWR. It is generally accepted that the LER/LWR is complex and many factors contribute. Studies in recent years have explored various parameters that contribute directly or indirectly to resist LER/LWR and methods to reduce the same.⁵⁻²¹ They can be broadly classified as non-resist related and resist component (formulation) related. Non-resist related parameters include intrinsic edge roughness found on the mask that can be transferred to resist image⁵, aerial image contrast⁶⁻⁷, pitch, and substrates. Higher aerial image contrast and also higher pitch for a given CD leads to lower LER. We have found that substrates also have an influence in the LER/LWR. For example figure 2 shows differences in LER/LWR for a given resist between organic bottom anti reflective coated silicon wafer and SiON.

Fig. 2 Influence of substrates on LER/LWR for a given resist.

The resist was exposed on a Nikon 306C exposure tool with 6% att. PSM, 0.85 NA, 2/3 annular illumination. Baked at soft bake temperature of 100C/60sec, PEB of 110C/60 sec and developed for 30 seconds using aq. TMAH

the size of one adamantane methacrylate a monomer($r=8.93 \text{ \AA}$) most commonly used in 193nm resist designs(Table 1).

solution. The substrate effects may be attributable to the differences in reflectivity as well as the microscopic differences in the distribution of photoacid generator and quenchers (concentration gradient) at the substrate – resist interface.

Resist material related effects include nature of monomers in the polymers and polymer composition⁸, polymer molecular weight and distribution⁹, amount of photoacid generator, type and acid diffusion¹⁰⁻¹², base quencher type and it's amount¹³⁻¹⁴, statistical effects during exposure and dissolution¹⁵⁻¹⁷, polymer aggregate formation¹⁸, phase incompatibility of protected and deprotected resin moieties at the boundary region between exposed and unexposed areas¹⁹, and interaction of exposed resist with developer²⁰⁻²¹.

In our studies we observed that molecular weight distribution did not play a significant role in controlling the LER/LWR. Figure 3 shows the LER values of resists (80 nm equal L/S) whose only difference is polydispersity of the resin used.

Fig. 3 Effect of polydispersity on LER

Attempts to reduce the LER/LWR by optimizing the resist formulation have its own limitation and trade-off. For instance, increasing base loading reduces LER but low sensitivity as well as resolution becomes an issue. Acid diffusion also helps but at the cost of losing resolution.²⁵ Gallatin²⁶ reports a model based on the relationship between resist blur (statistical

deprotection differences that occur in the vicinity of generated acid upon post-exposure bake process) and LER that predicts the limitations in simultaneously achieving low roughness and high resolution.

3. Some methods to improve LER

Resist formulation optimization is by far the best preferred method to improve LER/LWR. In addition to the limitations provided in section 2, if one takes in to account of the size of the monomeric units (close to 1nm) commonly used to make 193nm polymers and the radius of gyration of polymer molecules as shown in figure 4 whose size itself accounts to 2 to 5nm, it is unclear if the ITRS target of 2nm LER will be achieved only by resist optimization.

Fig. 4 Radius of gyration of polystyrene vs. molecular weight (Mw) in THF.

It is therefore important to investigate post-processing methods that could reduce LER/LWR. Some of the reported techniques include addition of organic salts to the developer solution, use of rinse solutions containing surfactants²⁷ organic salt additives²², application of overcoat layer to the resist²³, and chemical treatment in the etch chamber before the etch process²⁸. We studied the use of RELACSTM and hard bake (HB) processes to check their viability.

3.1 Effect of RELACSTM process on LER

RELACSTM process is known as a contact hole shrink process. Details of the process are published else where.²⁹⁻³¹ In this experiment, patterned wafer was coated with AZ[®] R-600 RELACSTM material. Since the purpose of the experiment is to provide a smooth coating to minimize LER, a milder mix bake condition of 100° C for 60 seconds was used. Figure 5 shows the top down SEM pictures of patterned reference wafer (80 nm, 1:1 L/S) and wafer treated with R-

600 and baked for 100° C for 60 seconds. Shrink was less than 10 nm. RELACS treatment leads to a noticeable improvement (from 5.1 nm to 3.7 nm) in LER. For dense L/S, this means that the original imaging may have to be carried out with a small offset from the isofocal line but it is a viable process to reduce LER.

Fig. 5 Minimizing the LER by application of RELACSTM process (80 nm equal L/S).

3.2 Application of hard bake process

Another process we studied is a simple hard bake process. Two 193nm resists denoted as resist A and B were employed for hard bake studies. Resist A is a methacrylate/acrylate hybrid polymer based (polymer Tg = 166 °C) where as resist B contains 100 % methacrylate polymer (polymer Tg = 182 °C). Both resists consists of adamantane and lactone groups similar to the polymers reported elsewhere.²⁴ Except for the polymers there was no other difference between resist A and B and was processed in a similar way details of which are provided elsewhere³². Hard bake of the patterned wafers were carried out on the coating track hot plates at a predetermined temperature and time described below. CD and LER measurements were carried out on a KLA[®] 8100 CD SEM, 150K magnification, 50 % threshold, 800V acc. voltage. LER analysis is performed on an image obtained by 256 frame to average using 32 scan lines for a 1.5 μm box. The measurement was repeated 10 uncorrelated measurement points. LER is reported as the 3sigma of the edge variation.

Figures 6 and 7 show the top down CD SEMs and X-SEMs of resist A and B. Both resist A and B showed nice improvement in LER values as well as visually observable smooth top down profiles. Resist A showed marked improvement (4.6 nm to 3.1 nm) at 160° C and for resist B (5 nm to 3.5 nm) it was at 180 ° C. There was no change in the CD (Figure 8) due to the hard bake and also the LER improvement was observed

through focus. There was no film thickness loss also for both resist A and B during the hard bake process

Fig. 6 Effect of hard bake (HB) process on LER for resist A (85 nm dense CD @ 36 mJ/cm²)

Fig. 7 Effect of hard bake on LER for resist B (85 nm dense CD @ 28 mJ/cm²)

Fig. 8 Influence of hard bake process on CD and LER for resist A.

Hard bake process was found to have a one major draw back. The wall angle of the edge lines (bulk) becomes less than 80° and is unacceptable for use. The resist bulk started to flow at about the same temperature where the LER improvement was seen. Resist A (figure 9) starts to show substantial degradation of the wall angle at 152 °C and at 170 °C for resist B and correlates well with the polymer Tg. Since the hard bake process is very simple to implement but for the bulk wall angle issue, we attempted to check the effect of flash hard bake - kind of thermal shock to the patterned resist. Thus the patterned wafers were heated at a given temperature for a short duration of time, typically 10 seconds or less and the process is referred as flash hard bake (FHB). Top

down CDs and X-SEMs are shown in figure 10 for resist A. A FHB temperature of 200 °C is needed for resist A and 220 °C for resist B to achieve good LER improvement. This temperature is about 40 °C higher compared to the standard hard bake process.

Fig. 9 Resist A edge line (bulk) wall angle after hard bake process

Fig. 10 Top down CD and X-SEMs of resist A after flash hard bake process for 10 seconds

Similar to the effects seen during the hard bake process, the flash hard bake also did not help in maintaining the edge bulk resist line angle. The wall angle for resist A as well B changed to 62° and 64°, respectively at temperatures (200 °C for resist A and 220 °C for resist B) where LER improvement could be obtained (figure 11). The bulk flow could not be avoided in the flash hard bake process as well.

4. Conclusions

Origins of LER and LWR were reviewed based on experimental and published literature data. LER as seen after patterning is influenced by aerial image contrast, pitch, substrate effects, hydrophilic/hydrophobic nature of the polymer, cleaving group type and content, PAG and

Fig. 11 Effect of flash hard bake process on the side wall angle of edge lines for Resist A

quencher amount, type and diffusion effects.

While resist formulation optimizations will continue to minimize LER, modeling and molecular size limitations predict that target LER of 2 nm will be difficult to achieve. RELACSTM and hard bake process were tried as post litho treatments. Both processes improve LER. However, thermal hard bake process also leads to decrease in the wall angle of the edge lines.

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