Au Nano-Wiring on Si Wafer with NaAuCl_4 -Ethanol Solution

Mikinori Suzuki and Shinzo Morita

*Department of Electronic Information System, Nagoya University
Nagoya, 464-8603, Japan
morita@nuee.nagoya-u.ac.jp*

Fabrication processes of Au nanometer wiring circuit was proposed, which is plated on doped Si wafer through resist windows or nano-insulation beds. The resist windows are fabricated with using negative resist by an electron-beam lithography process. After the Au plating, Au wired circuits is realized by oxidizing the resist and the Si substrate. The nano-insulation beds are fabricated by the special processes on the semi-conductive Si wafer, which have flat surface with conductive and insulating area. The Au plating is performed on the conductive area and the plated Au wire is insulated from base substrate by oxidizing Si surface area. Au plating is performed on the negatively biased Si wafer at 9V with using NaAuCl_4 dissolved in ethanol at 0.5 mol%. The Au plated area on the Si wafer through resist window showed dotted line. However continuous Au wire with 500 nm wide was successfully plated on the Si wafer, which was under coated with 1 nm thick semi-conductive carbon-sulfur-gold (C-S-Au) film.

Keyword : Au nanometer-wire, Nano-insulation-bed, NaAuCl_4 dissolved in ethanol, Electrical plating, Semi-conductive carbon-sulfur-gold film.

1. Introduction

Au plating technology on Si wafer will be applied for nano-wired electrical circuits and hybrid beds of biological and electrical devices.

In the nanometer device processes, the most interesting targets for the lithography works after Likharev [1] is the conductive wired circuit fabrication because the etching process is almost impossible to realized the metal wire with a few 10 nm wide. As the metal wire at a few 100 nm wide, Cu is presently using after the Al wired circuit. However, Au is supposed to be more profitable material at nano-wire circuit because Au is more chemically stable even if the Au volume resistivity of $2.3 \mu\Omega\text{cm}$ is larger than the Cu volume resistivity of $1.724 \mu\Omega\text{cm}$ at 20°C [2]

For the wired circuit fabrication, two kind methods were proposed in this works. One is plating in the resist window on the conductive Si wafer. The other is plating on the conductive area of Si wafer with

nano-insulating beds.

The resist window is prepared as followings. Spin coated negative resist on doped Si wafer were served to the electron beam patterning process. After the pattern development, Au plate is performed.

The plating through the nano-insulating bed on doped Si wafer is performed as followings. The doped n-type Si wafer is processed to pillars or walls with using a conventional lithography process. After that, the wafer with pillars or walls is oxidized in the oven with oxygen gas flow. Therefore oxidized Si wafer have oxidized pillars and walls, but the oxidized depth profile is not uniform under the Si wafer surface because of the pillars or the walls. Then the oxidized Si wafer is exposed to halogen gas plasma in order to etching off the oxidized pillars or walls and flatten the surface until the conductive heads are revealed in the oxidized Si wafer. The Au plating will be performed on

the conductive area. After the plating, the Si wafer will be oxidized again with plated Au layer. Finally Au plates insulated from the conductive Si substrate.

The Au plate is widely using for the biological bed to hold organic materials by the chemical bond between Au and S atom [3]. Therefore the Au plated layer on Si wafer will be used as hybrid beds of biological and electrical devices, if the Au layer is successfully plated on the Si wafer,

The C-S-Au film is an interesting material from the standpoint of fundamental material science as well as industrial applications. The C-S-Au films were fabricated using plasma CVD reactor with a parallel plate electrode system, using CH_4 , SF_6 and Ar gas mixture and the gold plate discharge electrode target [4]. By using the refractive index analysis [5], we found that such films with Au content at about 10 atomic% contains C-S-Au conductive grain with a size of 0.8~1.0 nm. This speculation was conformed by AFM/STM measurement [6].

2. Experiments

As a source material of Au, NaAuCl_4 was used, which is commercially available. NaAuCl_4 -ethanol solution at 0.5 mol% was prepared for the electrical plating.

Fig. 1. Au plating apparatus

In order to confirm the Au plating on to the Si wafer, three plates of n-type Si wafer, a glass cap and an electrical circuit with 9V battery were prepared as shown in Fig. 1. The three plates were immersed in the plating liquid in the glass cup and two plates were connected through 9V battery with using the Cu wire. The surface of three plates was served for the ESCA

analysis. The ESCA analysis were performed by using ESCA Lab 210 (V.G Scientific limited).

The plated wiring was fabricated with using resist window, which was fabricated on the spin coated negative resist film. The resist used was commercially available electron-beam resist (Shiplay SAL601). The patterning was performed by the electron-beam patterning machine (JEOL JBX-6000SG) at 50kV, 100pA and $100 \mu\text{C}/\text{cm}^2$.

The fabricated Au plated pattern was observed by using SEM.

3. Results and Discussions

1) Confirmation of Au plating

After 5 min plating, three plates were dried in the air. Their surfaces were analyzed by using ESCA apparatus. The ESCA spectrum was measured on the Si wafer as shown in Fig 2. Only on the plate connected to the negative electrode showed the Au deposition. The plate on the positive electrode and the plate without the voltage application did not show Au deposition. From the experiments, Au plating onto the Si wafer was confirmed

Fig. 2. ESCA spectrum of Au on Si wafer

2) Nano-wire formation through resist windows

In order to realize the nano-wire formation on the Si wafer, a resist was spin coated and patterns of 100, 200, and 400 nm L&S was delineated by using the electron beam patterning machine and the pattern were developed. The Si wafer with the resist window was immersed in the NaAuCl_4 -ethanol solution and connected to the negative polarity of battery at 9V. After a few min plating, the Si wafer was dried and exposed oxygen plasma to strip the resist. The Au plated Si wafer was observed by the SEM. The Au

wired pattern was not observed, but the Au deposition was observed only on the area around the place that the negative resist patterns were existed. The Au plated wire was not observed in the area of the resist window.

Next, the flat area of Si wafer without the negative pattern was covered by thick organic layer and only the area with negative resist window pattern were exposed to the Au plating in NaAuCl_4 -ethanol solution. After the oxygen plasma treatment, SEM picture of 100 and 400 nm L&S area was observed as shown in Fig. 3. It was confirmed that the Au plated was filled along the resist trench. However the Au plated lines were broken lines. The reason why the broken lines were formed is not known at this moment.

100 nm L&S

400nm L&S

Fig. 3. SEM picture of Au plated on Si wafer

In order to enhance the adhesion between the Au plated film and Si wafer, the C-S-Au thin film was under-coated by co-operation process of plasma CVD of methane, SF_6 and Ar mixture gas and sputtering of Au plate fixed on the upper electrode in the plasma CVD reactor. The C-S-Au film was selected as the interface layer, because the C-S-Au film can adhered the Au film to the Si wafer.

The Au plating was repeated again through the resist window after the semi-conductive 1 nm thick C-S-Au layer coating on the Si wafer. After the oxygen plasma etching of the resist on the Si wafer, SEM picture of 400 nm width Au plated wire was observed on the Si wafer as shown in Fig. 4. The Au plated wire was continuous film.

Fig. 4. SEM picture of 400 nm Au plated pattern.

The Au solid line at 400 nm width was formed by the Au plating through the resist window in NaAuCl_4 -ethanol solution. However the continuous plating was not performed through the window with 100 and 200 nm width. This phenomenon will be named as the micro-loading effect, which is known in the micro pattern fabrication by the plasma etching processes [7].

The reason of the micro-loading effect in the electro plating is not clarified yet. To overcome the problems, several experiments are necessary to realize the continuous solid lines with narrower lines than 400 nm.

3) Au plating through nano-insulation beds

The Au plating will be also performed by the other method, which uses narrow conductive lines surrounded by the nano-insulation beds. The nano-insulation bed will be fabricated by the processes as shown in Fig. 5. The firstly; nanometer size polls or walls are formed on n-type Si wafer by lithography processes. Next, the polls, and walls and flat surface of Si wafer are oxidized. Then the polls and walls are etched off to reveal the flat surface and the uniform plasma etching is continued to reveal the conductive heads in the insulating surface.

Fig. 5. The processes for the Nano-insulation bed fabrication.

The Au plating will be performed using the conducting lines as shown in Fig. 6.

Fig. 6. Au plating through the conductive lines

4. Conclusion

The Au nanowire was fabricated on the Si wafer through the resist window using the 1 nm thick semi-conductive C-S-Au film as interface layer between the Au film and the Si wafer. However the continuous Au plating was not realized for the 100

and 200 nm wide resist window, because of the micro-loading effect. The mechanism of micro-loading effect is not known at this moment. For the future process, Au plating through nano-insulation beds was proposed.

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