Double Patterning Materials for Sub-40nm Application

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Double patterning is one of the most promising candidates for sub-40nm half-pitch devices. Several variation of double patterning processes have been reported by research groups, including a dual-trench process (litho-etch-litho-etch) and a dual-line process (litho-litho-etch). Between these, the dual-line process is attracting the most attention because it is a simple process that achieves high throughput. However, there is concern that the second lithographic process damages the first litho patterns in the dual-line process. Therefore, new technology must be developed to keep the configuration of first litho patterns during the second lithographic step for this patterning process to be practical. Recently, we have succeeded in forming sub-40nm half-pitch litho patterns by the introduction of a new “freezing” step to this process. This step involves covering the first litho pattern with chemical freezing materials to prevent damage by the second litho pattern creating a dual-line process composed of litho-“freezing”-litho-etch processes. In this study, the performance of dual-line process including a “freezing” step are explained and sub-40nm half-pitch litho patterns including depth of focus, exposure latitude, CD uniformity and etching results by this process are shown.

Keyword: lithography, sub-40nm half-pitch, double patterning, freezing

1. Introduction

Recently ArF water immersion lithography began enabling the manufacturing of 45nm half-pitch devices. Water immersion lithography has the effect of increasing the NA parameter from 0.85 of dry lithography to 1.3, which gives higher resolution capability. Further improvement of resolution capability, should be necessary for sub-32nm half-pitch patterns, however, it is impossible to achieve such a higher resolution with existing water immersion lithography systems. According to the ITRS-roadmap, three candidates seem viable for patterning sub-32nm half-pitch patterns; extreme ultraviolet (EUV) lithography, high index liquid (HIL) immersion lithography and double patterning lithography. EUV lithography is expected to realize 22nm half-pitch patterning by adopting a short-wavelength of 13.5nm, but it would still take several years to fully

commercialize this technology. Similarly, development of new lens with a high refractive index ($n > 1.6$) will be required for HIL immersion lithography. On the other hand, existing ArF dry or water immersion lithography systems can be used for double patterning lithography, and would require only development of new patterning techniques and reticles. Therefore, double patterning lithography seems to be the most probable process for upcoming fabrication of sub-40nm half-pitch devices.

Several process flows of double patterning, including dual-trench process (litho-etch-litho-etch), have been previously reported¹⁻⁵. A dual-trench process requires dual lithography and etching after transcription of the first litho pattern on an inorganic stack by etching, which inherently decreases throughput. Therefore a double litho patterning system that is completed

before etching is desired to reduce the number of process steps. Meanwhile, dual-line process (litho-litho-etch)⁶ means that the entire lithographic patterns are completed before pattern transcription, so that only a single etching step is needed and higher throughput can be expected. However, there is concern that the second lithographic process damages the first litho pattern in a dual-line process. Therefore new techniques that protect the configuration of the first litho pattern without causing any damage during the second lithographic process will be required for a double patterning process to be practical.

In order to solve these problems, we have developed a new “freezing” technique for use in a dual-line process. This new dual-line process consists of (i) patterning first litho by normal ArF lithography process, (ii) “freezing” the first litho pattern, and (iii) patterning the second litho on the first litho patterns. Here, the freezing step works by covering the first litho pattern with a chemical freezing materials to prevent damage from the second litho process, this process is very important in the dual-line process of litho-“freezing”-litho-etch. For the patterning of sub-40nm half-pitch litho, it is important that the first litho pattern not only remains intact but also maintains (or improves) its lithographic performance after the second lithographic process. In this paper, the details of a dual-line process including a “freezing” step are explained and sub-40nm half-pitch litho and etched patterns created by this process are shown. Furthermore, the advantages of adding a “freezing” step are shown through the lithographic performance of 32nm half-pitch litho patterns.

2. Experimental

2.1. Materials

JSR FZX F103 was used for the freezing agent. JSR standard ArF resist, a methacrylate base 193nm photoresist, was used throughout this study. ARC91 was spin-coated on bare silicon substrates as a bottom anti-reflective coating (BARC) and aqueous, tetramethylammonium hydroxide (TMAH, 2.38 wt %) was used for developing the photoresist. Deionized water (DIW) was used for the immersion exposures.

2.2. Evaluation tools

CLEAN TRACK LITHIUS i (TEL) was used for the BARC/photoresist/freezing-agent coating, bake and development processes. Exposure was carried out with an ASML XT1700i (NA=1.00). CD measurement and observation of top-down profile for each wafer was performed using the CD-SEM: S-9380 (Hitachi High-Tech.).

2.3. Process flow of double patterning with resist “freezing”

Our resist freezing process is defined as covering the first litho pattern with chemical freezing materials, called a “freezing agent”, to prevent damage by the second litho process. The freezing agent is composed of resin and cross-linker, along with the appropriate casting solvent. Figure 1 shows each process step of double patterning with the inclusion of a resist freezing step. After patterning first litho on Si wafer coated with BARC (a), freezing agent is coated on first litho pattern and baked (b). During the bake, cross-linkage between not only a resin of the first litho pattern and cross-linker, but also resin of freezing agent and cross-linker, is accomplished by both the acid remaining at the surface of the first litho pattern along with thermal deprotection from the bake step. Then, unreacted freezing materials are developed (c) and the first litho pattern is completely frozen. After the resist freezing step, the second litho is patterned by the same lithographic process as the first lithography (d-g). During the second litho process, the cross-linked freezing material prevents the first litho pattern from dissolving by second exposure so double patterning is achieved.

Figure 1. Process schemes of double patterning with resist freezing process.

3. Results and Discussion

3.1 Patterning 32nmL/64nmP litho throughout each process step

To demonstrate the effectiveness of a double patterning process with resist freezing, formation of sub-40nm pattern was conducted. Figure 2 shows top-down SEM images measured at each double patterning step for patterning 32nmL/64nmP pattern. For 32nmL/64nmP double patterning, the 32nmL/128P first litho pattern was formed by a standard positive-tone lithographic process (left). After the resist freezing step, the first litho pattern remained without any surface damage (center). Subsequently, the second litho pattern, which also had 32nmL/128P, was formed at an offset from the first litho pattern by 64nm (right). As a result, a 32nmL/64nmP litho pattern was formed, while maintaining configuration of the first litho pattern. Top-down configuration of the 32nmL/64nmP litho pattern was good in double patterning step. Therefore, we have demonstrated a definite advantage of adding a freezing step for the formation of 32nmL/64P litho patterns.

Figure 2. Top-down SEM images measured in each double patterning step of 32nmL/64nmP pattern.

3.2 DOF and process window of 32nmL/64nmP double patterning

Depth of Focus (DOF) was measured for both first and second litho patterns of 32nmL/64nmP double patterning. Figure 3 shows top-down SEM images of 32nmL/64nmP litho patterns by positive and negative defocus for both first and second exposure. Though DOF of the second litho pattern is slightly smaller than that of the first litho pattern after second exposure, good 0.24 μ m common DOF in both first and second litho patterns of 32nmL/64nmP was obtained.

Additionally, the process window of

32nmL/64nmP litho patterns after double patterning is shown in Figure 4. This window indicates that 17% Exposure Latitude (EL) was obtained against 0.22 μ m DOF for the first litho pattern after second exposure, and 30% EL was obtained against 0.17 μ m DOF for the second litho pattern. These DOF and process windows are within practical levels for adoption of a freezing step in the commercial manufacture of 32nm half-pitch litho patterns.

Figure 3. Top-down SEM images of 32nmL/64nmP litho patterns after double patterning processes at 0.03 μ m intervals of positive and negative defocus with a center on best focus (BF).

Figure 4. Process window of 32nmL/64nmP litho patterns after double patterning processes. This window is drawn by ProData.

3.3 CD variation of first litho pattern throughout each freezing process

Our double patterning process includes a cross-linkage of the first litho pattern with the resist “freezing” agent, which essentially causes the increase of the first pattern CD. However, CD variation of the first pattern through each step should be minimized as

much as possible for the patterning of 32nm half-pitch. CD variation of the first litho pattern after the freezing step and the second litho for 32nm line/various pitch patterns were evaluated (Figure 5). For 32nmL/64nmP pattern, CD size of the first litho pattern was decreased by less than 1nm through the introduction of a freezing step, which is due to thermal shrinkage of the resist pattern by the high temperature freezing bake (usually, the bake temperature of the freezing process is higher than that of the litho process). Also, the CD of the first litho pattern was increased by around 4nm after the second litho, which is caused by a reaction between cross-linking units of the second resist and the first litho pattern. As a result, total CD variation through each double patterning step was less than 4nm.

Figure 5. Top-down SEM images measured in each step of double patterning of 32nm line and various pitch patterns.

Furthermore, pitch size dependency of first pattern CD variation for 32nm line, from 64nm pitch (line:space=1:1) to 352nm pitch (line:space=1:10), was also investigated (Figure 6). The CD variation of the first pattern, through the freezing step, was almost 0nm for all pitches, and the total range of CD

variation was kept within 3.6nm, where the maximum increase was less than 4nm for 32nmL/64nmP litho patterning. These results indicate that the CD variation through the freezing step is not dependent on pitch size, and dispersion of total CD variation through each double patterning step is also controlled to less than 4nm. Based on these results, our freezing step could be applicable to various pitch sizes of litho patterning. Though it would be desirable to decrease the total CD variation throughout the double patterning process to almost 0nm, decreasing of CD variation may be achieved by optimization of freezing materials and process conditions, for example, temperature and time of freezing bake.

Figure 6. CD variation of first litho pattern through each process step of double patterning.

3.4 Evaluation of CD uniformity throughout double patterning process of 32nmL/64nmP litho

Minimizing CD variations is very important for the manufacturing of devices. To understand the effects of the freezing step on uniformity of a 32nm half-pitch litho pattern, the variation of CD uniformity through each process step of double patterning was measured. Figure 7 shows the CD uniformity data of the first litho pattern in each process step of patterning 32nmL/64nmP on a 300nm wafer. The 3σ of the first litho pattern was initially 1.36nm, 1.96nm after the freezing step and 1.86nm after the second litho. Though CD uniformity became slightly worse during the freezing step, the CD uniformity of the litho pattern was kept within 2nm through each double patterning process step. It indicates the freezing process step is adequate for actual device fabrication.

Figure 7. CD uniformity data of the first litho pattern after first litho, after freezing step, and after second litho on 300mm wafer. Center of color bar corresponds to the average CD in each process step of double patterning.

3.5 First etching results of double patterning by freezing process

The lithographic pattern with 64nm Pitch was formed on BARC/SiOC/APF/Poly-Silicon/Oxide stack by double patterning with freezing agent and poly silicone etching experiment was conducted. Figure 8 showed top-down SEM image of 32nm line and space pattern after etching. There was no significant patterning image quality difference between 1st and 2nd pattern. This result suggests that double patterning with the freezing process enables ArF lithography to be used for sub-40nm half-pitch device application.

Figure 8. Top-down SEM images of poly silicone etching 32nmL/64nmP pattern formed by double patterning with freezing agent.

3.6 Formation of contact holes with resist “freezing” process

Our double patterning process is applicable to not only line and space (LS) patterns but also other kind of patterns, such as contact holes. Hole patterns are formed by the following steps; (i) forming first LS patterns, (ii) freezing first patterns, and (iii) forming second LS patterns perpendicular to the first patterns (Figure 9(a))⁴. Figure 9(b) shows top-down SEM images of hole patterns formed by double patterning with resist freezing.

Figure 9.(a) Process schemes of double patterning for hole patterns formation. (b) Top-down SEM images of hole patterns formed by double patterning with resist freezing. Hole/pitch sizes are 74nmHole/200P(left), 51nmHole/120nmP (center) and 46nmHole/104nmP (right).

We succeed in creating 51nm hole patterns with full circularity by patterning 70nm-lines perpendicularly. Similarly, 46nm hole patterns were formed by patterning 60nm-lines perpendicularly, but degradation of circularity was observed. We are currently studying the improvement of circularity for smaller hole patterns by considering the optimization of various lithographic conditions.

4. Conclusions

In this study, the details of a dual-line process including a “freezing” step were explained and the formation of sub-40nm half-pitch litho and etched patterns using this process was examined. A “freezing” step requires covering the first litho pattern with chemical freezing materials, known as “freezing agents”, to prevent damage by the second litho process.

Our double patterning process with resist freezing appears to have many advantages. Primarily, formation of double lithographic patterns is completed before pattern transfer on an inorganic stack, which enables the shortening of process flow and improvement of throughput. 32nmL/64nmP litho patterns were formed by freezing process. These patterns kept good configurations through each double patterning step. 32nmL/64nmP double patterning showed good 0.24 μ m common DOF in both the first and second litho patterns. Total CD variation of the first 32nm line pattern through each double patterning process step was less than 4nm and hardly depended on the pitch size, which showed that our freezing process could be applicable to various pitch sizes of litho patterning. CD uniformity of the first litho pattern was kept within 2nm through each double patterning process step for 32nmL/64nmP patterns. Furthermore, the first etching result of 32nmL/64nmP formed by double patterning with freezing agent was obtained. It suggests this freezing process is usable for sub-40nm half-pitch device manufacturing process. Additionally, our double patterning process is also applicable to patterning of contact holes. Circular 51nm hole patterns were formed by patterning the first and second line patterns perpendicularly, where a freezing step was incorporated after the first line pattern and before the second.

These results are the first evaluating report of lithographic performance (DOF, process window and CD uniformity) and etching for 32nmL/64nmP pattern formed by water immersion lithography.

We hope that our double patterning process will help the upcoming practical application of 32nm half-pitch devices.

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References

1. S. -M. Kim, S. -Y. Koo, J. -S. Choi, Y. -S. Hwang, J. -W. Park, E. -K. Kang, C. -M. Lim, S. -C. Moon, J. -W. Kim, “Issue and Challenges of Double Patterning Lithography in DRAM”, *Proc. of SPIE*, 6520, 65200H-1 (2007)
2. M. O. Beeck, J. Versluijs, V. Wiaux, T. Vandeweyer, I. Ciofi, H. Struyf, D. Hendrickx, J. V. Olmen, “Manufacturability Issues with Double Patterning for 50nm Half Pitch Single Damascene Applications, Using RELACS Shrink and Corresponding OPC” , *Proc. of SPIE*, 6520, 65200I-1 (2007)
3. W. -Y. Jung, S. -M. Kim, C. -D. Kim, G. -H. Sim, S. -M. Jeon, S. -W. Park, B. -S. Lee, S. -K. Park, J. -S. Kim, L. -S. Heon, “Patterning with Amorphous Carbon Spacer for Expanding the Resolution Limit of Current Lithography Tool” , *Proc. of SPIE*, 6520, 65201C-1 (2007)
4. H. Nakamura, M. Omura, S. Yamashita, Y. Taniguchi, J. Abe, S. Tanaka, S. Inoue, “Ultra-low k1 Oxide Contact Hole Formation and Metal Filling Using Resist Contact Hole Pattern by Double L&S Formation Method” , *Proc. of SPIE*, 6520, 65201E-1 (2007)
5. H. J. Liu, W. H. Hsieh, C. H. Yeh, J. S. Wu, H. W. Chan, W. B. Wu, F. Y. Chen, T. Y. Huang, C. L. Shin, J. P. Lin, “Double Patterning with Multilayer Hard Mask Shrinkage for sub-0.25k1 Lithography” , *Proc. of SPIE*, 6520, 65202J-1 (2007)
6. A. Vanleenhove, D. V. Steenwinckel, “A Litho-Only Approach to Double Patterning”, *Proc. of SPIE*, 6520, 65202F-1 (2007)