EUV Lithography Development and Research Challenges for the 22 nm Half-pitch

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Extreme ultraviolet lithography (EUVL) is the main contender for high volume semiconductor lithography patterning at the 22 nm half-pitch node. The most aggressive semiconductor manufacturers target pilot line introduction of this technology in 2011/12 and high volume manufacturing insertion in 2013/14. This requires the infrastructure of the supply chain supporting the technology—light sources, masks, and resists—to be ready once pilot line exposure tools are delivered to customers. Although improvements are still needed, the current status of infrastructure technology readiness suggests that it will support the targeted pilot line insertion date. However, to support high volume manufacturing introduction, more significant developments are still required to address technical and business challenges. These include demonstrating reliable high power EUV sources and enabling a commercial mask tool infrastructure that can support sub-20 nm defect inspection and review requirements.

Keywords: Lithography, EUV

1. Introduction

More than 25 years have past since the first image was recorded using light in the extreme ultraviolet (EUV) wavelength spectrum [1]. More than 10 years ago, EUV lithography (EUVL) was targeted for manufacturing introduction at 100 nm feature sizes [2]. Since then, EUVL has missed its introduction for high volume manufacturing (HVM) at three subsequent technology nodes: 65 nm, 45 nm, and 32 nm half-pitch (hp) [3]. For the 65 nm and the 45 nm hp nodes, the industry turned to more affordable extensions of tried and tested optical transmission lithography. 193 nm lithography was eventually extended down to imaging ~50 nm features, making use, for example, of polarization techniques and focus drilling to allow for robust manufacturing process windows. Then, as 193 nm dry lithography ran out of steam, 193 nm immersion lithography was quickly ramped up and introduced at the 45 nm hp node.

Although EUVL infrastructure and technology were clearly not ready to be introduced into HVM at the ≥ 45 nm hp nodes, they likely would not have been introduced even if they had been ready. Extensions of existing lithography technologies have always been the preferred path to enable the printing of smaller integrated circuit (IC) features because this approach minimizes risk, is more cost-efficient, and builds on existing know-how. However, this is no longer true for the 193 immersion double patterning lithography (DPL) that now must be used for ramping up 32 nm hp manufacturing because EUVL is not ready. Most cost-of-ownership calculations show EUVL to be significantly more affordable than 193 immersion DPL at the 32 nm and 22 nm hp nodes [4]. If EUVL cannot be made ready to support introducing 22 nm hp HVM, the industry could find itself without a cost-efficient lithography to support manufacturing needs. Therefore, the industry must address the remaining infrastructural issues hindering the introduction of EUVL.

2. Status of EUVL

EUVL has seen more than 25 years of development taking it all the way from first principles demonstrations to full-field EUVL alpha-type exposure tools being used to evaluate its manufacturing readiness [1,5,6,7,8,9]. EUVL now must succeed at pilot line introduction in 2011/12 and then HVM introduction in 2013/14.

To introduce a new lithography technology into pilot line and later into manufacturing, the infrastructure of the supply chain supporting the technology needs to be in place. Fig. 1 illustrates
the so-called lithography development food chain. Clearly, success in lithography tool development depends on access to all lithography-enabling infrastructure. And lithography exposure tool suppliers will be able to sell their tools to IC manufacturers only if the supporting infrastructure is successfully in place.

![Lithography Development Food Chain Diagram](image)

**Fig. 1. The lithography development food chain.**

This interdependence of suppliers and customers is even more evident for EUVL for which most of the infrastructure and technology could not build on previous technologies. Frequently, such a mutual interdependence can become a chicken and egg problem—everybody waits for everybody else to make sufficient progress before they believe that the technology is for real. For EUVL, this phase is long gone and a very different spirit of cooperation has taken root. However, for EUVL to be successfully introduced, an even higher level of cooperation will be required among all stakeholders to address the remaining technology and infrastructure challenges in time for a 2011/12 pilot line introduction.

Every year, the EUVL critical issues/focus areas are reviewed and ranked after a three-day symposium by industry experts. At the 2008 EUVL Symposium [10], EUV sources remained the main concern for the third consecutive year. However, EUV masks and resists swapped rankings since EUV mask technology is now seen as more critical than resist, largely due to the excellent progress in EUV resist development over the past two years. Specifically, EUVL technology and business development must demonstrate the following:

- Long-term source operation with 100 W at the intermediate focus (IF) and 5 megajoules delivered per day
- Defect-free masks throughout the lifecycle and inspection/review infrastructure
- Resist resolution, sensitivity, and line edge roughness (LER) targets met simultaneously

EUV source readiness is still seen as the most significant risk to introducing EUVL. Clearly, without reliable EUV sources meeting power and performance specifications for pilot line operation very soon, EUVL will never be introduced into manufacturing.

Assuming that EUV sources will support the EUVL pilot line schedule of 2011/12, significant infrastructure gaps in the EUV mask area still must be resolved. While in some instances this can be accomplished by individual organizations, addressing the most important mask tool gaps will require a concerted industry effort. The various industry stakeholders—consortia, IC companies, and suppliers—must closely work together to enable defect-free mask blanks and the respective supporting infrastructure.

Excellent progress has been made in improving EUV resist performance. It is generally agreed that EUV resists are almost ready to support EUVL pilot line introduction. The remaining most challenging aspect is simultaneously meeting the requirements for resolution, line width roughness (LWR), and resist sensitivity. As the development of new resist platforms take a long time, understanding and addressing the fundamental physics limitations of improving LWR to extend EUV beyond the 22 nm hp node will be important.

### 2.1 EUV Source

The EUV power requirement that exposure tool suppliers have agreed upon is 180 W at the IF based on a resist sensitivity of 10 mJ/cm², which must be delivered at the IF within a 2% bandwidth window centered about the 13.5 nm wavelength. This power specification has remained constant for several years. Radiation produced by the plasma source outside the 2% bandwidth, so-called out-of-band (OOB) radiation, needs to be suppressed because OOB radiation reaching the resist could diminish image contrast as resists tend to be sensitive to such radiation.
To support pilot line introduction, integrated medium power level source collector modules (SoCoMos) must reliably support ~50 W at the IF over extended operating periods. Over the past decade, the industry has developed two EUV source technology choices: discharge produced plasma (DPP) and laser produced plasma (LPP). Initially, LPP sources were seen as the better option and they supported the first exposure stations, including the first full-field prototype scanner [2,5]. However, after 2003, LPP development significantly diminished while DPP sources continued to progress. Because of that, DPP became the source technology of choice to support standalone microexposure tools (METs) and the first full-field alpha tools.

Source power requirements from exposure tool suppliers kept rising until by 2006 they eventually settled on 180 W at the IF for the first generation of EUVL HVM tools. Because of that, the scalability of integrated SoCoMos with power requirements became an increasing concern and led to a renewed interest in LPP technology, which was becoming perceived as the intrinsically more scaleable technology. Hence, the pendulum has swung back and LPP sources have become the prime candidate for use in the first EUVL exposure tools to support EUVL pilot line introduction. However, regardless of the technology currently in favor, LPP or DPP, SoCoMo integration and reliable operation at a power level supporting EUVL pilot line operation are the main challenges with EUV sources.

As DPP sources have been used in alpha tools, much more data on their integrated performance is available. The power level currently being used in alpha tool operation is only a few watts of EUV power at the IF. As this is significantly lower than the ~200 W at the IF that will be needed in manufacturing tools, it is difficult to predict whether DPP sources can be scaled to this higher power level while meeting the high reliability and uptime requirements of pilot line operation. Generating higher EUV power levels at the source point seems possible; however, extracting the generated EUV power with collectors and debris mitigation devices engineered to withstand the much higher thermal loading is proving to be more difficult.

For LPP sources, there is no field data for integrated SoCoMos. While scaling technology to higher power requirements is likely less of an issue for LPP than for DPP technology, a fully integrated SoCoMo as it will be used in beta-type exposure tools has not yet been demonstrated. Achieving the required power at the IF, efficiently collecting EUV photons, and solving the debris mitigation problem are also seen as key challenges for LPP. Increasing the power of the pump lasers and cost of ownership are other critical issues that must be addressed. Clearly, cost of ownership is seen as a more immediate concern for LPP sources because they have been selected to be used in beta-type exposure tools and will likely be used in the first EUVL production tools.

Fig. 2 shows the progress reported by source suppliers of useable EUV power output delivered at the IF [11]. The values are still much lower than the 50–100 W at the IF that will be required for EUVL pilot line operation. However, since early 2008 the rate of progress has increased and suppliers are addressing the challenges of building integrated sources that include efficient EUV light collection, effective debris mitigation, and possibly spectral filtering, all of which tend to reduce the achievable power output at the IF.
The best usable power value reported for DPP sources is \( \sim 8.0 \) W at the IF extracted from 170 W of EUV power generated at the source point. This source has been demonstrated for runtimes of many days with full debris mitigation and a six-shell collector. While both DPP and LPP technologies face scaling issues as power is being ramped up, those associated with DPP sources are likely greater than those restricting LPP source output. In addition, the ultimate power level at the IF achievable with LPP sources will likely be higher than for DPP sources. This becomes important if one looks beyond the first generation of EUVL HVM tools for which power requirements could scale to 500 W and higher at the IF. As can be seen in Fig. 2, the best LPP sources now produce useable EUV output of \( \sim 20 \) W at the IF. This level of power, which is only a factor of 2–3 away from power levels that can support EUVL pilot line introduction, was demonstrated over an 18-hour run in an integrated test bed source using a 1.6 sr collection mirror and debris mitigation system [13].

Fig. 3. Projected electricity needs for a fab with 10 EUV scanners assuming a CO\(_2\)-based laser source with 50% duty cycle and $0.07/\text{kWh}$ [12].

The electrical input power projections for EUV HVM sources are currently in the 300–500 kW range. With ten EUV exposure tools in a chip manufacturing plant, the power requirements will be in the 3–5 MW range. This is not only a cost concern but also an environmental concern and will likely drive the need for more efficient EUV sources. Developing sources with greater efficiency will be more difficult for DPP than for LPP. LPP source efficiency can dramatically increase if diode-pumped laser modules can be used, but improving the efficiency of an electrical discharge source is more difficult. Fig. 3 shows the projected electricity needs for ten EUV exposure tools assuming a CO\(_2\)-based laser source with 50% duty cycle and $0.07/\text{kWh}$; it compares these numbers with the projected power requirements and costs if fiber laser-based sources can be used instead. Although fiber laser-based sources are currently not close to delivering the required power to support HVM LPP sources, laboratory demonstrations clearly indicate their potential as highly efficient pump lasers for second or third generation LPP sources that may be targeting 500 W at the IF. At a source power of 180 W, annual savings for a fab using fiber laser-based sources with ten EUVL scanners can amount to \( \sim 2.0 \text{M} \) [12].

As Fig. 2 illustrates, suppliers of DPP and LPP sources will need to increase usable output power at the IF by a factor of 3–4X by the end of 2009 to stay on the roadmap for supporting EUVL pilot line introduction. Because of that and the lack of reliability data at higher power levels, EUV source readiness is still seen as the major risk to the introduction of EUVL. However, once sufficiently mature sources enable pilot line introduction, mask yield is expected to quickly become the most important issue for EUVL.

Not surprisingly, EUV sources are also critical to enabling several EUV mask metrology applications, among them actinic inspection and review tools. While for several EUV metrology applications low power DPP sources are now being used, the development of coherent EUV sources has progressed [14]. If higher power coherent EUV sources become available in the next several years, they certainly will be attractive light sources in helping to achieve the challenging EUV mask inspection requirements.
2.2 EUV Masks

As EUVL moves closer to pilot line introduction, the industry’s major concern is shifting from the availability of high power EUV sources to the availability of high yielding EUV masks. Mask defects have always been a major concern as the ability to manufacture defect-free EUVL masks and to keep them defect-free during handling, shipping, and use raised serious doubts when EUVL was initially proposed as a potential manufacturing technology. Progress has been made in reducing mask blank defects to a level that is only a factor of ~25X away from pilot line requirements; however, commercial EUV mask blanks must also meet other metrics (e.g., for the optical performance of the EUVL Bragg reflector and for mask flatness as outlined in SEMI P37 and P38) [15,16]. Meeting all mask blank specification requirements simultaneously is more difficult than meeting only a subset of the metrics.

EUV Mask Substrate

While the thermal performance metrics of the low thermal expansion materials (LTEMs) that must be used for EUV substrates have routinely been met, simultaneously meeting the requirements for defectivity, flatness, and roughness remains difficult for doped glass materials. Specifically the trade-off between flatness and defectivity is challenging as the substrates undergo several cycles of fine polishing and local flatness correction such as ion beam finishing. During polishing, defects can be generated either by removing material and creating pit defects or by embedding material and creating bump defects; if the embedded material is removed in a subsequent polishing or cleans step, it will convert the bump defect into a pit defect.

Because bump defects can convert into pit defects more easily than the other way around, the majority of substrate defects in a clean manufacturing process are expected to be pit defects. A detailed analysis of the defect types on a typical substrate shows that the dominating defect species are indeed pit defects [17]. Reducing pit defects will require improved polishing processes. To develop those, a much more detailed understanding of the interactions among the substrate surface, the polishing slurry, and the polishing pad will be necessary.

As has been pointed out, the boundaries between cleans and repair processes are becoming increasing murky with EUV masks [18]. If only a few defects must be addressed, a repair process may be preferable; if many defects must be addressed, cleans processes are likely more efficient. Although repairing defects has been considered for EUV substrates, filling or removing individual pits and bumps is a slow process and not cost-efficient; a global repair process—a cleans process—that can render all substrate pit defects non-critical is required. Recently, such cleans processes have been successfully used to reduce the total number of pit defects and to shift the center of the pit defect size distribution to smaller pits [19].

Parallel to developing improved polishing processes and cleans processes to prevent and mitigate substrate pit defects, the stringent mask flatness requirement is being re-evaluated by the industry. The flatness requirement for reflective EUV masks is driven by the pattern placement accuracy needed on the wafer. Initially, the industry addressed this by requiring a perfectly flat mask [15]. However, more recently it has been recognized that a certain amount of well characterized mask non-flatness can be tolerated if it can be compensated for by adjusting the pattern written on the mask such that the end result imaged onto the wafer is the same as for a perfectly flat mask with no flatness compensation during pattern write. First results show that this is feasible, at least to correct for low order non-flatness terms such as a simple bow. It now seems likely that greater non-flatness for EUV substrates can be tolerated [20]. Relaxing the flatness specification will make it easier to meet the defectivity specifications for EUV substrates.

Making progress in reducing substrate defects will require better substrate defect metrology. Current substrate defect inspection tools may enable finding defects down to the 30 nm polystyrene latex (PSL) equivalent, but finding smaller defects will be challenging. Defect inspection tools are expensive, and for EUV substrates they likely will be required only to introduce EUVL into manufacturing, but not when EUVL is in the HVM phase. Therefore, non-optical defect inspection techniques may have to
be used to complete substrate development to support HVM introduction.

**EUV Mask Blank**

The EUV mask blank is an EUV Bragg reflector that must be defect-free and perfectly flat with the highest possible EUV reflectivity [16]. While the best such EUV blanks today routinely meet optical specifications, meeting defectivity metrics remains challenging. Achieving a mask yield that can support EUVL pilot line introduction will require not only significant progress in reducing substrate defects and defects added in the multilayer deposition process but also extensive use of defect mitigation, compensation, and repair techniques.

![Graph showing mask blank yield with zero defects vs defect density](image)

**Fig. 4.** Zero-defect mask blank yield as a function of defects that can be successfully mitigated. The yield function assumes a simple Poisson model and the upper curves (b) show yields for a smaller area than the full mask blank quality area as shown for the lower set of curves (a). The number next to a curve indicates how many defects were assumed to be “repairable” for this specific yield curve, and the grayed areas indicate today’s defect level (scaled to 18 nm and 25 nm defect sensitivity) and the pilot line and HVM defect target areas.

Clearly, even if only a few mask blank defects can be successfully rendered non-printable, mask yields acceptable for pilot line EUVL introduction should be feasible if the current mask blank defect level can be improved by a factor of ~50 or even less if initially the full mask blank area is not used. The graph also shows that achieving nearly defect-free mask blanks > 0.003 defects/cm² corresponds to about a half defect in the full mask blank quality area—will be difficult if no defect repair or mitigation techniques are available to make blanks with a few defects acceptable.

Fig. 4 shows the zero-defect mask yield calculated by a simple Poisson-type model as a function of defects that can be successfully mitigated. Two series of curves are shown: the lower set assumes the full mask blank quality area of 142 cm x 142 cm is used; the upper set assumes that only an area of 100 cm x 100 cm is being used. For each calculated curve, it was assumed that a specific number of defects would be “repairable”; that is, they could be made non-printable by direct repair, smart pattern placement (defect covered with absorber), or defect optical proximity correction. Also indicated are today’s mask blank defect levels, the desired yield range for pilot line operation in 2011/12, and the HVM target (0.003 defects/cm²).

The curves in Fig. 4 consider all defects detected by inspection tools—printable and non-printable. However, it is not known how many of the defects found on today’s blanks actually result in printable defects. The best currently available data does indicate that only a fraction of the defects on today’s masks result in printable defects. Those results initially came from printing evaluations using larger design features (45 nm node designs) and older mask blanks that had many more defects than current blanks [21]. Recently similar results have been found for printing smaller feature sizes (22 nm node design) [22]. Hence, what Fig. 4 shows as today’s best mask blank defect level may actually be too pessimistic since not all of the defects found today will print. Determining exactly what types of defects are printable/non-printable is critical to enabling the introduction of EUVL.

The industry uses different kinds of defect inspection technologies to detect mask blank defects. The workhorses among them have been optical inspection tools using inspection wavelengths of 488 and 266 nm. In parallel, the industry has developed so-called actinic inspection
tools capable of inspecting and/or imaging EUV blanks at the EUV wavelength. The continued reduction of mask blank defects critically depends on ever more sensitive defect inspection tools becoming available. Already today, we know that the best available optical inspection tools do not see all the defects that an actinic tool can. Fig. 5 compares an image recorded with SEMATECH’s aerial imaging tool (AIT) [23] and the same defect image acquired by SEMATECH’s Lasertec M7360 [24] optical inspection system. As can be seen, optical defect inspection systems are reaching their resolution/sensitivity limits.

Fig. 5. Mask blank defect image as recorded with SEMATECH’s AIT and the best optical defect inspection tool [25].

An analysis of the aerial images of the defects shown in Fig. 5 using an intensity drop in the aerial image below a 40% threshold as the printability measure predicts that none of the defects would print in an open area. However, they still could print if they were located in a densely patterned area; additional experiments and data will be necessary to verify this. Building a defect printability database that can help predict which mask blank defects will be printable under what conditions (dark-field or bright field mask, densely patterned area, close to an isolated feature, or open area, illumination conditions etc.) is one of the key tasks that needs to be addressed. Once the key critical defect types are better known, mask blank defect reduction can focus specifically on eliminating those defect types in the mask blank manufacturing process.

In addition to improved defect inspection capability, a new generation of multilayer deposition tools will be required. With some modification and process learning, the current generation of multilayer ion beam deposition tools should be able to achieve pilot line quality for mask blanks. However, a new deposition tool design is needed that includes all past learning from current tools and has more flexibility for hardware modifications to determine the final tool configuration that can support HVM mask blank deposition. Defect-free deposition process development on those tools must be supported not only by adequate inspection sensitivity but also by significantly improved capabilities for compositional analysis of nanosize particles and defects. Only when such smaller defects can be located (inspection tools) and defects can be analyzed (compositional analysis) will it be possible to identify the defect sources and eliminate them step by step.

**EUV Mask Patterning and Use**

Mask blank suppliers and mask shops have developed mask stack materials and patterning processes that are expected to provide the high fidelity and high resolution mask templates required for the 22 nm hp node [26]. However, to manufacture masks at yield, mask shops will need improved metrology capabilities to fine-tune their processes. Foremost among those capabilities are aerial imaging and patterned mask inspection, which are required to disposition defects. The industry currently has only one synchrotron-based aerial imaging tool that can support the EUVL development effort. Initially, if those tools were not available for pilot line introduction, the industry could resort to printing-based defect inspection; however, once EUVL is ramped up to HVM levels, mask shops will need a standalone aerial imaging and patterned mask inspection capability.

The first real defect data from integrated devices that had layers exposed with EUVL became available only recently [21,22]. Surprisingly, only a small fraction of mask blank defects resulted in printable defects. Fig. 6 shows images of two mask areas recorded with the SEMATECH actinic AIT at Lawrence Berkeley National Laboratory and the same mask areas imaged with a scanning electron microscope (SEM). In both areas, the SEM images clearly show two different types of defects. The AIT images recorded at EUV wavelength, however, show that the printability of those defects is likely
less severe than would be suggested by the SEM images.

![Fig. 6. Comparison of mask defect images recorded with an AIT and with an SEM. Reprinted from ref. 22 by permission of SPIE.](image)

Fig. 6. Comparison of mask defect images recorded with an AIT and with an SEM. Reprinted from ref. 22 by permission of SPIE.

Fig. 7 compares a mask SEM image and the respective printed wafer image also recorded with an SEM. Clearly, understanding defect printability is critical in judging the scope of the defectivity challenge for EUVL. The conservative assumption for specifying mask defect requirements is to assume that all defects print. However, with EUVL, this may be too pessimistic.

![Mask SEM and Wafer SEM](image)

Fig. 7. Comparison of defect images recorded with a mask SEM (left) and the printed wafer SEM image (right). Reprinted from ref. 22 by permission of SPIE.

From the best defect printability today, we can extrapolate that only about 10–20% of all mask defects result in a printed wafer defect. If one combines this result with an initial mask yield pilot line requirement for zero-defect masks of 20–50%, the pilot line mask defect levels required to introduce EUVL can be predicted. The curves in Fig. 8 show mask defect yield as a function of the percentage of printable defects for a set of mask defect levels ranging from the production requirement of around a half defect (0.003 defects/cm²) to masks with roughly 200 defects in the mask blank quality area.

The vertical gray bar area in Fig. 8 represents the percentage range (10–20%) of defects that have been found printable. The horizontal gray bar outlines the initial mask yield range that is likely needed to support EUVL pilot line introduction. The intersection of the vertical and horizontal gray bars defines the target zone for pilot line defect requirements that must be met for EUVL introduction. As can be seen, that zone ranges from ~0.02 to 0.06 defects/cm². No defect size specifications are required to draw the graph in Fig. 8, but if one were to introduce EUVL for 22 nm hp patterning, the size would be around 18 nm; if one were to introduce EUVL earlier for a mid-cycle insertion between the 32 and 22 nm hp nodes, then the specification would be around 25 nm.

![Fig. 8. Mask yield as a function of the percentage of printable defects for different mask defectivity levels. The numbers next to the curves give the defectivity level in defects/cm². The vertical gray bar indicates the currently found defect printability (10–20%), and the horizontal gray areas indicate an initial mask yield that can support EUVL pilot line introduction and later HVM.](image)

Fig. 8. Mask yield as a function of the percentage of printable defects for different mask defectivity levels. The numbers next to the curves give the defectivity level in defects/cm². The vertical gray bar indicates the currently found defect printability (10–20%), and the horizontal gray areas indicate an initial mask yield that can support EUVL pilot line introduction and later HVM.

Using the best available defect data today and rescaling it from the best current defect inspection sensitivity to 18 nm and 25 nm, respectively, the current defect levels correspond to defect densities of ~1.0 defects/cm² at an 18 nm size equivalent and of ~0.4 defects/cm² at a 25 nm size equivalent.
Therefore, for a mid-cycle insertion, the industry must improve defectivity by a factor of ~10X; for a 22 nm insertion target, mask defect levels must improve by a factor of ~ 25X. As pilot line insertion is targeted in 2011/12, defectivity improvements between 10–25X certainly should be achievable.

Fig. 8 can also be used to predict the required defect level to support HVM mask yield requirements. Mask shops do not disclose mask yield data, but it is not likely in the > 90% yield area. A reasonable assumption is that the 70–85% area represents a good estimate, which would indicate that levels around 0.01 0.02 defects/cm² should be able to support HVM EUVL introduction.

Achieving a high mask making yield is not sufficient. EUV masks also need to be protected from particle and molecular contamination during handling and use. Zero particle adder handling, shipping, and storage concepts have already been demonstrated down to a 40 nm equivalent PSL size [27]. However, this was taken using EUV substrates and not patterned EUV masks for testing. Therefore, the next steps must be to demonstrate defect-free handling, storage, and use with patterned EUV masks while extending the inspection sensitivity to sub-30 nm. Because molecular contamination is usually related to mask exposure, data is limited since few exposure tools are available and they have comparatively low EUV flux. However, even under low flux conditions, carbon growth is being observed and its impact on critical dimension changes is being evaluated. For more realistic testing, EUV power levels at the mask must be increased to what is expected for pilot line and HVM use. Cleans processes to remove particles and contamination are being successfully developed. While the results are encouraging, a better fundamental understanding of the relevant physics and chemistry is clearly needed; e.g., results show that the cleaning efficiency for removing very small particles (e.g., < 50 nm) is very much reduced [17]. This is not a specific challenge for EUV masks and may be more severe for optical masks because of their higher susceptibility to pattern damage.

While EUVL masks are not yet ready to support EUVL pilot line introduction, there is good reason to expect that they will in 2011/12. However, to achieve this, the remaining mask infrastructure challenges must be aggressively addressed. Key among those challenges is the availability of higher sensitivity mask inspection and review tools, specifically actinic mask blank inspection tools to stay on the defect reduction roadmap and standalone aerial imaging tools as well as actinic patterned mask inspection tools. And finally, EUVL masks must remain cost-competitive as compared to high end optical masks.

2.3 EUV Resists

The development of chemically amplified resist (CAR) platforms for EUVL has made impressive progress over the past two years. The resolution potential of current resist platforms has been consistently underestimated; only a few years ago, there was significant concern that the resolution of CAR platforms could hit a brick wall at ~35 nm hp. Now, as shown in [28], CAR platforms have recently broken the 22 nm hp imaging barrier and demonstrated image modulation down to 20 nm hp [28]. In addition to sub-22 nm hp imaging of dense lines and space patterns, EUV CAR platforms have also demonstrated excellent contact hole imaging. Fig. 9 shows an SEM cross section of a high resolution contact hole; all the images were recorded with SEMATECH’s EUV MET at the Berkeley Advanced Light Source Lab.

![Fig. 9. Cross-section SEM images of high resolution resist exposures recorded with SEMATECH’s MET at Berkeley [28].](image-url)

The MET has a 0.3 numerical aperture (NA); to record the images in Fig. 9, rotated dipole illumination was used. For EUV full-field alpha demo tools (ADTs), which have a 0.25 NA, use conventional illumination, and have about twice the amount of flare as the MET, 26 nm hp pattern and 27 nm isolated line resolution and sub-30 nm contact hole resolution with good isolated/dense contact hole bias have been demonstrated [29, 30].
SEMATECH has been working with all major resist suppliers to evaluate and accelerate progress towards meeting 22 nm hp performance requirements. Tab. 1 summarizes the performance status at the end of 2008 for meeting resolution, LER, and LWR; sensitivity; and pattern collapse specifications. For resolution and LWR, performance is measured against the International Technology Roadmap for Semiconductors (ITRS) specifications. The ITRS specifies LWR as 8% of a microprocessor unit (MPU) gate critical dimension in resist, but for dynamic random access memory (DRAM), LWR requirements do not have to be as stringent. Tab. 1 also compares the data against a looser LWR specification for DRAM, 8% of DRAM hp, that likely will be sufficient to introduce EUVL for this device technology.

Sensitivity is not specified in the ITRS but is driven by productivity requirements. As indicated above, the source power specification for a 100 wafer per hour tool throughput is 10 mJ/cm². The ITRS does not have a specification for resist pattern collapse; however, this is one of the critical issues for manufacturability. Typically a patterned resist aspect ratio (AR) of 2.5 needs to be targeted for manufacturing, which implies a resist thickness of 55 nm for the 22 nm hp node. The benchmark data in Tab. 1 was recorded using 50 nm thick resist films.

Tab. 1. EUV resist benchmark performance as measured against 22 nm hp requirements. All data was acquired using the SEMATECH 0.3 NA MET with dipole illumination.

<table>
<thead>
<tr>
<th>Metric</th>
<th>Resolution [nm]</th>
<th>LER / LWR [nm]</th>
<th>Dose [mJ/cm²]</th>
<th>Resist Collapse [nm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>ITRS / HMV Specification</td>
<td>22</td>
<td>NA / 12 (1.39)</td>
<td>10.0</td>
<td>2.5</td>
</tr>
<tr>
<td>A</td>
<td>22</td>
<td>3.8 / 5.6</td>
<td>14.5</td>
<td>28 (1.92)</td>
</tr>
<tr>
<td>B</td>
<td>24</td>
<td>3.2 / 4.6</td>
<td>12.0</td>
<td>28 (1.78)</td>
</tr>
<tr>
<td>C</td>
<td>30</td>
<td>5.3 / 8.0</td>
<td>12.2</td>
<td>30 (1.67)</td>
</tr>
<tr>
<td>D</td>
<td>28</td>
<td>5.2 / 7.9</td>
<td>13.3</td>
<td>30 (1.67)</td>
</tr>
<tr>
<td>E</td>
<td>28</td>
<td>3.5 / 5.1</td>
<td>15.0</td>
<td>30 (1.67)</td>
</tr>
<tr>
<td>F</td>
<td>30</td>
<td>4.8 / 6.8</td>
<td>7.8</td>
<td>34 (1.47)</td>
</tr>
<tr>
<td>G</td>
<td>32</td>
<td>4.5 / 7.1</td>
<td>8.8</td>
<td>36 (1.39)</td>
</tr>
</tbody>
</table>

1) MET 0.3 NA, rotated dipole
2) Average of 30 nm, 22 nm, 36 nm, and 40 nm HP 1:1 dense line features
3) 50 nm resist thickness
4) The number in brackets gives LWR for DRAM HP with an 8% 3σ specification

Tab. 1 shows that LWR for the benchmarked resist materials is ~4-6X greater than the ITRS specification. With respect to the relaxed DRAM LWR requirement, the gap is reduced to a 2.5-4.5X difference. Clearly, going forward, improving LWR while maintaining all other performance specifications is the greatest challenge for resist development. Sensitivity is 1.5X greater than the specification and needs a ~30% improvement from current best values. Pattern collapse is seen for ARs >1.9, which limits resist thickness to ~40 nm for 22 nm hp patterning. If single layer resist patterning with a 2.5 AR is required for etch, then pattern collapse needs to be improved by 1.3X.

To support the early mid-cycle introduction of EUVL between the 32 and 22 nm hp nodes, resist suppliers must focus on engineering resists to meet specific requirements. These must include a fast resist with high resolution and moderate LWR (~3-4 nm) that can support DRAM and Flash device applications for the near future, but allow the moderate LWR to be improved through post-processing of the resist or through LWR-reducing etch processes. At the same time, MPU gate-level processing will require a slower resist with higher resolution and better LWR to meet the more stringent LWR specification required by MPU gate-level processing.

![Fig. 10. LWR performance vs. requirements.](image-url)

Developing application-specific resists for microprocessor and memory device manufacturing is a realistic target and should be achievable to support EUVL pilot line introduction in 2011/12. Fig. 10 shows a more extensive data set of LWR vs.
resist resolution performance and illustrates the gap that needs to be closed between current LWR values and the ITRS specification or a more relaxed DRAM LWR specification; LWR would have to be reduced by about 2 nm through post-processing starting from what seems to be a very achievable 3-4 nm LWR target for today's fast and high resolution resists.

Although EUV CAR platforms have demonstrated that they are much more extendable, it remains to be seen how far they can ultimately go. As of today, these platforms appear capable of supporting 22 nm hp manufacturing, but will they be extendable to the 16 nm hp and beyond? Some of the challenges EUV resist development is facing for patterning at features sizes ≤ 22 nm hp are EUV-specific while some are generic and will have to be addressed by potential extensions of 193 nm immersion lithography as well. The EUV-specific challenges mostly relate to the EUV-specific exposure mechanism [31,32,33]. Thin film resist effects such as the scaling of LWR with resist film thickness is a challenge that EUVL shares with extensions of 193 nm immersion lithography. Simultaneously meeting resolution, LWR, and sensitivity metrics (the so-called RLS challenge) will become increasingly difficult with shrinking feature sizes. When preparing resist materials, component uniformity needs to be controlled on the relevant pixel level to improve the targeted resolution. This will have to include molecular level engineering so that during EUV exposure, excitations can be kept localized and decay channels can be controlled. To achieve this, a more fundamental understanding of the relevant energy transfer processes in EUV resists is indispensable.

As is well understood, diffusion driven by post-exposure bake is the main contributor to resist blur below 50 nm feature sizes [34]. Clearly, there will be an intrinsic resolution limit for chemical amplification driven by kinetic processes. Educated guesses as to what this diffusion limit could be are in the 10-15 nm range. To limit the diffusion-related resist blur, the amount of base loading is usually increased. This, however, leads to slower resists requiring more photons. While a high base loading is beneficial in unexposed areas and helps narrow the diffusion zone, it also reduces the number of available acids in exposed areas. An approach to address this problem is to develop resists with photo-decomposable bases [35,36,37]. This approach decreases base loading during the latent image formation in exposed areas. While there will still be competition between acid formation and base trapping of protons, the exposed areas will contain less base after the latent image formation. This process should allow the use of resists with higher base loading so that in the latent image there will be a base and acid gradient when crossing from the exposed to the unexposed area. This gradient should help limit diffusion-related resist blur during post-exposure bake.

Approaches such as the photo-decomposable base could help push the resolution limit of CARs to smaller feature sizes and reduce LWR. However, it is not clear yet how much more LWR in current resist platforms can be reduced as feature sizes keep shrinking. While in the near term, post-exposure LWR reduction looks promising, new platforms or chemistries must be pursued to meet LWR requirements for future patterning nodes in case CAR platforms will not support them any more.

3. Summary

The most aggressive semiconductor manufacturers target 2011/12 for EUVL pilot line introduction. While EUVL source readiness is still perceived as the greatest challenge, EUV masks will quickly move to the fore as semiconductor manufacturers will require EUV mask yields that can support critical layer exposures in pilot lines. EUV source power is close to meeting pilot line readiness but long-term reliability and stability of integrated high power EUV sources still need to be demonstrated. On the mask side, the industry is actually closer to meeting pilot line yield requirements than would have been expected only a few years ago. This is mostly because, contrary to expectations, only a small fraction of mask blank defects seem to result in printable defects. Resist readiness was perceived as the greatest challenge only three years ago. Due to excellent progress since then, EUV resists are clearly perceived to be on track to support 22 nm hp manufacturing and to present a lower risk to EUVL introduction than either EUV source or mask readiness. The industry can be optimistic about EUVL infrastructure being ready to support EUVL
pilot line introduction. However, several critical gaps in the commercial mask tool infrastructure still must be addressed to support EUVL HVM introduction in 2013/14. In addition, EUVL sources must demonstrate high power operation (> 150 W at the IF) over extended periods of time and scaling of optics contamination/mitigation, mask temperature control, and overall thermal stability must be demonstrated for HVM EUV power levels.

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