The Design of Photosensitive Polyimide Materials for Buffer Coating Processes

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The reasons for the use of photosensitive polyimides (PSPIs) in semiconductor buffer coating processes and the technical problems associated with such materials have been widely described. The requirements for the further improvement of the pre-established processes and the considerations affecting the design of future PSPI materials are discussed. The next generation of PSPI buffer coating processes is briefly described.

Keyword: buffer coating process, photosensitive polyimide, PSPI

1. Introduction

Photosensitive polyimides (PSPIs) have been widely used as semiconductor passivation materials in buffer coating processes because of their excellent physical properties and photo-definable characteristics [1,2]. There are four major roles for PSPI materials: stress buffers, heat resistance, promoters of adhesion between Epoxy Molding Compound (EMC) and the passivation layer, and the patterning of the fuse and pad area in semiconductor fabrication processes. Traditional two-mask polyimide (PI) buffer coating processes for semiconductor fabrication have been replaced by one-mask PSPI processes because of the need for process simplicity and the reduction in the costs of the formation of the buffer coating layer.

There were many technical issues that arose during the initial stages of the use of PSPI materials in semiconductor fabrication processes. The main issues resulted from poor communication between material producers and device manufacturers. Device manufacturers attempted to substitute PSPI layers for PI layers without altering their established PI buffer coating processes because they hoped to reduce process costs by adopting PSPI processes without investing in new facilities or upgrading process control. From the viewpoint of the device manufacturers, the change from PIs to PSPIs resulted only in the addition of photo-definability, yet many modifications to pre-established PI buffer coating processes were required. In addition, this change in material affected the characteristics of the interfaces between buffer coating layers and packaging materials as well as the packaging processes themselves.

2. Technical affecting the introduction of PSPIs

The important technical issues mostly involve the front end fabrication (FAB) process in which the PSPI buffer coating layer is formed. Unlike PIs, PSPIs are photo-definable materials, and so should be managed similarly to the photosresists used in lithography processes. In patterning processes, the resolution and dissolution rate contrast of PSPI materials are poorer than those of photosresists. The enhancement of the resolution of PSPI materials was a high priority in the development of PSPI buffer coating processes. Apart from the inherent contribution of the material to improved resolution in PSPI lithography, many process variables such as the soft bake temperature, the post-exposure delay time, the appropriate developing recipe, the exhaust rate, and the mask bias should be

Received May 5, 2009
Accepted June 5, 2009
optimized to obtain high resolution. To obtain patterning uniformity, the variations of the temperature of the bake unit and of the thickness of the coated material should be controlled. The out-gassing of small molecules makes it difficult to use scanning electron microscopy (SEM) to monitor patterning during the buffer coating process and the reaction of PI and PSPI in the drain line to give solid products made it necessary to use separate pipe lines to drain each material.

After the FAB process, the wafers covered with PSPI are transferred to the packaging process. All packaging facilities and processes that were initially adopted and optimized for PI layers need to be checked for compatibility with the new PSPI layers. The relatively poor transparency of PSPI layers with respect to aligning lasers in packaging facilities has resulted in failures in consecutive manufacturing due to the poor recognition of wafers. PSPI material also should endure abrupt heat and mechanical stress during packaging. After the packaging process, interface layers form between the PSPI and the packaging material such as EMC or a PI adhesive. Most problems at these interfaces arise due to mismatches between the different materials. Any damage occurring during these back end processes usually results in reliability failures during electrical tests under various heat and pressure conditions. However, the confirmation of the results of such reliability evaluations normally requires more than two months and it is sometimes very difficult to determine the origin of the problem, so careful design of the experiments and evaluations of any modifications must be carried out.

3. Further considerations

As the range of applications of PSPI materials increases and semiconductor fabrication processes change, many new issues related to the use of PSPI materials are becoming apparent. Long, inconvenient preconditioning procedures and a short shelf life at room temperature brought about a lot of human errors related with handling of PSPI materials. The high viscosities of PSPI materials mean that it is difficult to attain coating uniformity and to reduce the dispensed volume. The trend towards the minimization of fuse and pad size has also driven the need to increase patterning accuracy. Open area uniformity should also be improved to reduce the number of failures related to wire bonding processes. Cosmetic problems and process-driven defects must also be minimized, especially for wafer level business applications. The random particles generated by previous processes and the bubble defects formed during the curing process also necessitate additional removal steps. Without an in-depth understanding of material properties, it is very difficult to determine the origins of such defects and to remove the process-driven defects. Thus, appropriate countermeasures for each PSPI material need to be taken into consideration.

The productivity of the steppers used in exposure processes needs to be improved, particularly for highly sensitive PSPI materials. The total processing time for a wafer in a stepper has recently been significantly reduced by decreasing the time allotted to each shot. In order to increase the sensitivity of PSPIs, attempts have been made at formulation optimization through the optimization of resins, PACs (photoacid compounds), and solubility enhancers. The trend towards the minimization of devices has also driven a reduction in the thickness of the final wafer down to ~ 30 um for specialized applications. This trend in final wafer thickness necessitates the development of tough PSPI materials with low warpage.

4. Next generation PSPI processes

Technical trends in semiconductor devices require new PSPI designs. The introduction of temperature-sensitive devices into the market means that low temperature curable materials with low power and enhanced connection requirements are required, particularly in novel packages such as wafer level and chip scale packages. If the demand for these kinds of new packages increases, the range of applications and the importance of PSPI passivation layers will also increase. In addition, multi-chip packages (MCPs) and systems in packages (SIPs) have resulted in the emergence of new kinds of interfaces between materials, so the adhesion properties and characteristics of the PSPIs need to be controlled and optimized.

Competition between device manufacturers is another factor driving the modification of PSPI formulations for material makers to include cheaper raw materials. The insistence on environment-friendly materials and processes is also of increasing importance to the buffer coating applications of PSPI materials.

Acknowledgements

I am grateful to lots of material engineers and researchers in Japanese PSPI makers such as Toray,
HDMS, Sumitomo Bakelite for their continuous material improvement for my requests and cordial discussion with various problems.

References