Three Litho-Process-Litho Approaches for 2D Double Patterning at the 32nm Half Pitch Node

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Various material approaches for more cost-effective double patterning have been proposed during the past few years. Resolution capabilities of these approaches using dipole illumination are documented in literature. In this paper it is investigated whether these novel materials may also be applied for printing of more random structures at the 32nm half pitch using annular illumination. As expected process windows with more relaxed illumination conditions are observed to decrease. The CD bias of Litho1 features throughout the double patterning process is observed to vary more under annular illumination compared to dipole. This has important implications for the process window of the Litho1 target. Nevertheless, excellent CDU results are obtained for all three processes. LWR is shown to be high, which can be mainly attributed to the illumination setting and is not inherent to the materials. Finally a demonstration of the printing feasibility of turns and stitching in selected logic and DRAM structures is given. The poly-Si etch capabilities of the alternative processes is also shown.

Keywords: double patterning, line width roughness, resolution

1. Introduction

In 2007, water immersion lithography at the 193nm imaging wavelength has reached its maximum practical numerical aperture (NA) at 1.35 [1]. Systems with this NA allow imaging down to 36.5nm half pitch under extreme off-axis illumination conditions at $k_1=0.255$. With the path to high index immersion lithography being abandoned [2, 3], further resolution improvements with ArF lithography thus require breaking through the limit of 0.25, which is not possible in a single patterning step.

For double (or multiple) patterning, alignment and overlay are the main technological challenges in order to perfectly match the two photos. However, an additional practical drawback is that the total litho costs are almost doubled for litho-etch-litho-etch (LELE) double patterning (DP) schemes (Figure 1). More clever DP process schemes may help to alleviate this burden in part, but do require new patterning material developments. Several approaches for such litho-process-litho-etch (LPLE) schemes have been

proposed. The general theme in most schemes is to avoid the first etch step of the LELE process and ‘freeze’ the first photo. The second resist layer may then directly be coated over the patterns of Litho1. The cost reduction mainly comes from avoiding the first etch step, but is partially offset by higher resist consumption that is required for Litho2. The currently used LPLE approaches do not allow for using a solvent pre-wet during Litho2 resist coat. For these alternative DP processes resolution capabilities to 32nm half pitch and below have been demonstrated using extreme dipole illumination conditions [4-8]. Such conditions are good for demonstrating material resolution capabilities, but will not be very suited for more random patterning that is typically required for Logic or DRAM type applications.

In this paper, three material approaches for LPLE will be discussed at 32nm half pitch using annular illumination to allow for more random feature patterning. These are: 1) Coat-freeze (CF) approach from JSR [5,7]. In this process a freezing material is coated over the 1st resist patterns that is

subsequently baked and developed to remove excess freezing material. After this the 2nd resist may be applied. 2) Thermal freeze (TF) from JSR [5,7]. Here the freezing property is built into the resist of Litho1. The freezing is activated by a bake step after development of Litho1. 3) Posi-posi (PP) approach from TOK [6,8]. The 2nd resist solvent is chosen such that it does not dissolve the patterns of Litho1. A bake is required after the development of Litho1 to remove excess solvent. Approaches 2 and 3 have a cost benefit over approach 1, since no additional freeze material and fewer in-track process steps are used (Figure 1). On the other hand, the CF process is the most mature.

Figure 1. Comparing process costs of patterning steps of virtual single patterning (VSP) with LELE, and LPLE processes. The alternative processes bring ~10% cost benefit compared to LELE.

2. Experimental

All experiments have been done in the imec 300mm cleanroom facility. Exposures are done on the ASML TWINSCAN XT:1900iTM scanner. All wafers are aligned for both Litho1 and Litho 2 patterns to zero-markers etched in the silicon substrate. No overlay optimization has been done. The dipole illumination setting used is NA=1.0 with $\sigma_{out}/\sigma_{in}=0.85/0.65$ dipole40X and Y polarization. For annular exposures NA=1.35 with $\sigma_{out}/\sigma_{in}=0.85/0.65$ annular illumination and XY polarization is used.

Wafer processing is fully done on a Sokudo RF^{3S}TM track interfaced with the XT:1900iTM scanner. Either 80 or 90nm resist thickness is used depending on the LPL approach investigated.

It is important to note that the process conditions used for all three alternative processes are not optimized for the low aerial image contrast that comes with the annular illumination setting. The same process conditions are used as recommended for dipole illumination.

In the standard test pattern, three different areas are patterned side by side during the DP process. The left and middle areas get exposed with gratings of 1:3 duty cycle during the first exposure. The middle and right areas get exposed with gratings of 1:3 duty cycle during the second exposure. Thus the left area contains single patterned (SP) lines printed during the first exposure with the first resist and pitch 1:3. The right area similarly only contains lines printed during the second exposure with the second resist and pitch 1:3. Only in the middle area are both lines printed together, resulting in a final 1:1 pitch at the pitch of interest. It is important to note that both the SP and DP areas undergo the full DP process.

All measurements are done on a Hitachi CG4000 CD-SEM. CD and line width roughness (LWR) are measured for Litho1 pattern and/or Litho2 pattern as applicable. Data is checked on top-down SEM images, re-measured off line where needed and subsequently analyzed with Klarity ProdataTM software from KLA-Tencor for process window analysis or with MATLAB from The MathWorksTM for CD uniformity (CDU) analysis. For LWR measurements rectangular scans at 300x49kX magnification are taken and analyzed with LERDEMO software from Demokritos in order to capture low frequency LWR contributions [9].

3. Results and Discussion

3.1 Litho1 process bias

For comparison of results from this study with previous work [10,11] the impact of annular and dipole illumination on Litho1 has been studied (Figure 2). The resulting Exposure Latitude (EL) versus Depth of Focus (DoF) curves for the CF approach are shown. Annular illumination results in an EL decrease of approximately 50% and a DoF reduction of around 60% when compared to dipole. This relative reduction in EL and DoF matches with ProlithTM simulations using a non-calibrated resist model. Similar results are obtained

Table 1. Process bias (in nm) on Litho1 lines compared to CD after Litho1 only. Results are given after freezing step only and after the full process in the single patterned (1:3 duty cycle) and double patterned (1:1 duty cycle) areas.

	Annular			Dipole		
	CF	TF	PP	CF	TF	PP
Freezing only	2.7	0.9	-0.9	3.4	1.0	-0.1
SP full process	2.9	-3.3	-5.2	4.5	-3.8	-3.6
DP full process	7.7	-3.3	-3.7	5.2	-4.0	-2.5

for the PP approach. Although the exact EL and DoF numbers will differ, the relative EL and DoF reduction is the same.

For good control of the DP process in the LPLE approach it is important to understand how processing for Litho2 impacts the patterns of Litho1. In order to study this, the impact on CD after three steps in the process is considered for Litho1: the freezing step by itself, after the full process in the Litho1 SP area, and after the full process in the DP area. Typically a bias is found when the full double patterning CD is compared to the patterns after Litho1 only. This process bias is determined for the three LPLE approaches (Table 1). Here a negative bias indicates CD shrink of Litho1 compared to the CD after Litho1 only, while a positive bias indicates CD growth.

Figure 2. EL versus DoF for dipole and annular illumination for the CF process.

Minor CD changes occur upon the freezing step. In the PP process the freezing bake causes a minor CD loss, which may be attributed to solvent or water evaporation. In the TF process there is a small CD growth which is probably due to minor reflow of the resist. For CF the CD growth is somewhat more substantial, which can be rationalized by additional material that is put on the original pattern in the freezing step (coat and bake).

The most important effects are seen after the full DP process. Most notably, the CF approach gives a substantial CD growth of Litho1 after the full DP process, whereas PP and TF give more moderate

CD reduction. The further CD growth with CF upon full DP could be attributed to reaction of the Litho2 resist with the freeze material on the Litho1 lines. In the case of PP and TF the additional bake and development steps during Litho2 on the Litho1 lines may cause additional deprotection and dissolution, leading to a net CD shrink.

For the annular illumination settings the magnitudes of the biases for PP and CF appear to be larger when compared to the dipole settings. The most likely reason for this increased process bias lies in the shallower aerial image for annular illumination. This means that there is a broader zone of partially deprotected material at the edge of the resist profile. In the PP and TF cases this material may or may not be removed in the second development step depending on the position of the development threshold. In the CF case it means more material can play a role in the freezing reaction which results in more CD increase. Other effects such as profile reflow during the freezing process could also play a role in the observed process biases. Finally, there is also a clear proximity impact of the Litho2 pattern on the Litho1 bias, especially for CF. The CD growth of the Litho1 patterns in the double patterned area is significantly larger than in the Litho1-only area.

The observed process biases on Litho1 have important consequences for the Litho1 process windows. In order for both Litho1 and Litho2 patterns to print to target after full DP, Litho1 initially needs to be overexposed to ~24nm for CF, and underexposed to ~36nm for TF and PP. Especially overexposing the CF process is on the limit of the process. In order to have a robust process, it was therefore decided to use a target Litho1 of 26nm and allow for a slightly higher CD after final DP for the CF approach. In Figure 3 the impact of the required biases on the process windows of Litho1 in resist before the freezing process are given for the three approaches. For both PP and TF underexposing the lines to 36 and 35.5nm respectively results in a minor decrease of EL and an increase in DoF. Also the absolute numbers of the process windows between these

Figure 3. EL versus DoF windows for the three LPLE processes after Litho1 in resist compared for the 32nm target and for the required target to meet 32nm after the full DP process.

Figure 4. EL versus DoF windows for the three LPLE processes after full DP for the Litho1 lines in the double patterned area.

Figure 5. Full wafer CDU for the three LPLE processes after full DP. Mean CD and 3σ CDU values (in nm) are given for Litho1 (L1) and Litho2 (L2) separately.

two processes are quite similar. The drop in EL for PP and TF is expected due to lower NILS upon underexposing. This may be recovered (at least in part) by using appropriate biasing on the mask. For this study this has however not been attempted. On the other hand, for the CF approach the

overexposing to 26nm results in a significant decrease of both EL and DoF.

Finally, the impact of the full DP process on the Litho1 process windows have been determined (Figure 4). In all cases the full DP process causes a further reduction of the Litho1 process windows. For CF both EL and DoF are further reduced. For PP and TF there is not much impact on EL, but DoF is reduced after full DP, when compared to just Litho1. The reduction in DoF is somewhat more moderate for the TF case.

3.2 32nm hp CDU and LWR with annular

To further determine the process robustness of the three DP approaches, full wafer CDU and LWR have been determined after the full DP process. The results for the CDU analysis are given in Figure 5.

In spite of the significant drop in process window when using annular illumination, all three processes are still capable of meeting 3σ CDU numbers below the 10% target at the 32nm half pitch. The CF and TF processes even are capable of achieving CDU less than 2nm, which is an excellent result. It should be noted however, that the Litho1 CD for the CF process cannot be printed to target, since Litho1 cannot be sufficiently overexposed (*vide infra*).

Figure 6. PSD plots for the three LPLE processes demonstrate the LWR response through frequency of the Litho1 and Litho2 prints, separately.

Table 2. 3σ LWR and correlation length for the three LPLE processes after full DP.

	3σ LWR (nm)	Corr. Length (nm)
CF-Litho1	7.1	31
CF-Litho2	6.9	23
TF-Litho1	5.4	28
TF-Litho2	4.6	23
PP-Litho1	4.9	26
PP-Litho2	6.7	27

For the LWR analysis, the lines of Litho1 and Litho2 after the full DP process (in the DP area) have been analyzed separately. A PSD analysis has been applied on the lines in order to understand the contribution of different frequencies to the total LWR. The results are summarized in Table 2 and Figure 6.

Figure 7. Top-down SEM image in rectangular scan mode (300x49kX) for the CF process as used for LWR measurements. In the circles a small pattern deformation is observed. Within the field of view of a typical square scan image (as indicated by the horizontal lines), this would typically not be noted

The LWR performance of the three processes is quite comparable when expressed in absolute 3σ numbers. The roughness is relatively high at $\sim 6\text{--}7\text{ nm } 3\sigma$, which is typical for the low NILS annular illumination condition that is used. For all three processes the roughness from Litho1 and Litho2 is not the same. In the case of CF and TF the roughness of Litho1 is higher than that of Litho

2, whereas in the case of PP the trend is opposite. Also the correlation length of the roughness is higher for Litho1 which may be caused by the nature of the freezing process. The PSD analysis shows that the higher roughness in the case of PP is consistent over the entire frequency range. For CF and TF the difference in roughness mainly stems from the low frequencies. In the mid and high frequency region the roughness between Litho 1 and Litho 2 is similar. The low frequency LWR of Litho1 could (in part) be caused by very low frequency pattern deformation as highlighted by the ovals in Figure 7. These pattern deformations are only visible when a careful analysis using rectangular scan is made. The frequency is too low to be picked up within the field of view of a regular square scan image. The dimensions of such a field of view are highlighted by the horizontal bars in Figure 7. The origin of the pattern deformation is not further investigated but may be caused by the freezing process. Potentially, optimization of the freezing conditions could remove these deformations, but this has not been attempted.

3.3 Turn and stitching patterning and 1D etch feasibility

Some suitable designs have been selected [12,13] to illustrate the ability to pattern line turns, and line stitching at the 32nm half pitch (Figure 8). In the logic case the cutting and stitching is done in the turn, in the DRAM case there is no cut in the turn but cutting and stitching is done in an island structure. It should be noted that a non-calibrated aerial image based OPC was used to design the mask. As a result not all lines could be printed on target.

The result obtained with CF and PP for the logic test pattern is shown in Figure 9. The pattern is well defined for both CF and PP alternatives with smooth printing of the turns and no stitching issues are observed. Similarly Figure 10 shows the results

for the DRAM pattern for the CF and PP processes. For the DRAM test pattern 64nm and 72nm pitch are printed. In all cases the patterns are well defined with smooth turns and again no stitching issues are observed. The 2D printing and stitching exercise on the TF process is still ongoing.

Figure 8. 32nm half pitch logic (left) and DRAM (right) test patterns used for 2D printing and stitching tests

Figure 9. Top-down SEM images of 32nm half pitch 2D logic patterns after full DP demonstrate excellent stitching capabilities.

Figure 10. Top-down SEM images of 32nm and 36nm half pitch 2D DRAM patterns after full DP.

Finally, an etch feasibility study at the 32nm half pitch is done. Patterns were etched into 50nm poly-

Si on gate oxide. 25nm SiOC on 70nm APF was used as hard mask for this patterning. Here results from dipole illumination are shown. However, no difference in etch performance is expected when annular illumination would be applied. It should be noted that a standard etch recipe has been used and was not optimized for the current application. Further improvements in targeting and CDU should thus still be possible. Figure 11 gives etch results for the three LPLE processes. The line wiggling that is observed for the TF process originates from pattern collapse due to the non-optimized reflection control. The results demonstrate that these LPLE processes all give sufficient etch resistance to pattern features in a relevant stack with excellent profiles down to the required dimensions.

Figure 11. Top-down and x-section SEM images after pattern transfer of LPLE DP line/space patterns into poly-Si by standard dry etch process.

4. Conclusion

This study has demonstrated that the currently available approaches for more cost-efficient double patterning are well capable of printing random 2D logic and DRAM structures with annular illumination. Special attention is needed to correctly target Litho1 in order that it reaches the desired CD after the full double patterning process. This so-called process bias is shown to depend on the illumination condition as well as on the type of LPLE process that is used. The bias may be either positive or negative. For each process there is a bias range over which a workable process can be achieved.

CDU for the three studied processes has been demonstrated to be well within target. LWR is on the high side for all processes, but this is largely due to the annular illumination condition. There may be differences in LWR performance between Litho1 and Litho2. Moreover, these differences may vary over the LWR frequency range.

Finally 2D printing (including turns and stitching) and etch feasibility has been demonstrated. No specific issues for either stitching or etching have been identified for any of the processes under study.

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