Non Topcoat Self-freezing Photoresist for Double Patterning Process

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Double patterning is one of the most promising techniques for sub-30nm half pitch device manufacturing. Several techniques such as dual-trench (litho-etch-litho-etch: LELE) and dual-line (litho-litho-etch : LLE) have been reported. Between them, the dual-line process attracts a great deal of attention due to its higher throughput. The key issue in the dual-line process is preventing damage of the first resist pattern during the second lithography process. As a solution, we have developed a process to alleviate this issue using a chemical material called “freezing agent.” More recently, we have further simplified the process by developing a simple freezing technique called “self-freezing”. The “self-freezing resist” material can accomplish the freezing process by applying only one bake to the resulting first pattern. In addition, our self-freezing resist also has added water shedding properties to meet non-topcoat (non-TC) immersion resist requirements, which further simplifies the process and materials.

In this study, imaging results of Non-TC self-freezing resist including critical dimension uniformity (CDU), defectivity and processing properties of the resulting patterns is shown.

Key words: lithography, double patterning, self-freezing, non-topcoat

1. Introduction

ArF water immersion lithography systems enabled manufacturing of 45 nm half-pitch devices. However, single exposure alone cannot achieve sub-32 nm half pitch resolution due to optical image limitations. For next generation lithography, two viable candidates are; extreme ultraviolet (EUV) lithography and double patterning lithography. EUV lithography is expected to realize 22 nm half-pitch patterning by adopting a short- wavelength of 13.5 nm, but it might not be applied for full commercialization for a few years. However, double patterning lithography would be considered the most promising technique, since it can be applied with existing ArF water immersion lithography tools.

For double patterning lithography, several extensive process flows, including both dual-trench (litho-etch-litho-etch) and dual-line (litho-litho-etch) (LELE) processes, have been reported. The simpler dual-line process (litho-litho-etch (LLE)) means that all lithographic double patterning is completed before pattern transfer to the underlying substrate, so only a single etching step is needed. The LLE process obviates the low throughput disadvantage of the dual-trench
LELE process, which requires two lithography processes and two etching processes. For the dual-line process, the first pattern needs to have chemical resistance to second lithography process. We have already developed so-called litho-freezing-litho-etch (LFLE) process to freeze the first pattern through the use of a chemical freezing agent, and the process successfully demonstrated the formation of sub-32 nm printing.\(^7\)\(^-\)\(^8\)

In this paper, a further simplified LFLE process is reported. Printing using a novel self-freezing photoresist without topcoat is the most important feature of this process, which does not require the freezing agent to immobilize the first pattern. Designs, properties, and lithographic performances of the non-TC, self-freezing resist are discussed. CDU and defect inspection data were collected to discuss the practical use of the process. In addition, pattern transfer to silicon oxide substrates were carried out to demonstrate the overall feasibility of the LFLE improved process with non-TC, self-freezing resist.

2. Experimental

2.1. Materials

JSR non-TC self-freezing resist and JSR non-TC ArF resist were used for double patterning as first and second litho, respectively. All these resists used in this experiment were designed to work without a topcoat. Nissan Chemicals ARC66 or ARC29A coated on 300 mm bare silicon wafers were the substrates for general lithographic data collection. Pattern transfer testing was carried out on JSR multilayer materials with a SiO\(_2\) substrate. Tetra-methyl-ammonium hydroxide aq. (TMAH, 2.38 weight %) was used to develop the resist.

2.2. Evaluation tools

Tokyo Electron Clean Track LITHIUS Pro-i, Tokyo Electron Clean Track ACT12, or SOKUDO RF\(^3F\) was used for resist coat, bake, and development. Exposure was carried out with Nikon NSR S610C (NA = 1.30) or ASML XT1900i (NA = 1.35). Observation of top down photoresist profiles was carried out with Hitachi High-Technologies CG-4000, or S-9380. Observation of cross-sectional profile was carried out with Hitachi High-Technologies S-4800 or S-5200. Defect measurements were done with KLA Tencor KLA2800.

2.3 Process flow of double patterning with non topcoat self-freezing resist

Process flows of the chemical-freezing and self-freezing processes are shown in Fig. 1. The chemical freezing process requires extra steps, i.e., freezing material coat, freezing bake and TMAH development to remove the unreacted freezing agent. In contrast, the self-freezing process requires only one bake to immobilize the first patterns. Additionally, non-TC functionality was also introduced into our self-freezing resist system for more materials and processing reduction. Basic properties of the non-TC self-freezing resist are discussed in the next section.

![Chemical Freezing Process Flow](image)

![Self-Freezing Process Flow](image)

Fig. 1 Schematic illustration of Process flows of Chemical-Freezing and Self-Freezing process.

3. Results and Discussion

3.1 Property of Non-TC Self-Freezing resist

At first, to confirm resist immobilization after the self-freezing process, bulk pattern profiles after second lithography process were checked. For a conventional ArF resist, the pattern almost disappeared after the second patterning due to the solubility with the casting solvent of the second resist. On the other hand, the non-TC self-freezing resist showed much better resistance to the second lithography process. This result suggests that self-freezing system works properly for double patterning lithography.

![Comparison of Bulk Pattern Damage](image)
For ArF immersion lithography, water shedding property such as advancing contact angle (ACA), receding contact angle (RCA) are important in terms of exposure scan speed and defects such as the bubble and water mark defects. Reducing the level of PAG anion leaching is also critical, because such contamination can cause damage to the immersion lithography tool. The measured leaching level of PAG anion was 0.18 ng cm$^{-2}$ s$^{-1}$, which meets the specifications of both Nikon and ASML. Thus, our non-TC, self-frozen resist satisfied these requirements, and can be used in ArF immersion lithography.

<table>
<thead>
<tr>
<th>CA / degree</th>
<th>ACA / degree</th>
<th>RCA / degree</th>
<th>Leaching / ng cm$^{-2}$ s$^{-1}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>90.1</td>
<td>94.2</td>
<td>76.0</td>
<td>0.18</td>
</tr>
</tbody>
</table>

Table 1 Water shedding and leaching property of Non-TC self-freezing resist. The specs on leaching are 2.5 ng cm$^{-2}$ s$^{-1}$ and 1.6E-12 mol cm$^{-2}$ s$^{-1}$ for Nikon and ASML respectively.

3.2 Patterning and CDU of 26nmL/52nmP line and space (LS)

Formation of 26 nm L/52 nm P LS was carried out with ASML XT1900i (NA = 1.35, dipole). For double patterning a 26 nm L/52 nm P LS pattern, a 26 nm L/104 nm P LS pattern was first formed by a standard positive lithographic process. After the freezing bake step, the first litho pattern remained without any surface damage or CD variation. Subsequently, the second litho pattern of 26 nm L/104 nm P LS was formed at an offset from the first litho pattern by 52 nm. Figure 3 shows top down and cross-sectional SEM images of 26 nm L/52 nm P LS pattern.

Minimizing CD variation is very important for device manufacturing. To understand the effects of the self-frozen step on CDU of 26 nm half-pitch litho pattern, the variation of CDU through each process step of double patterning was measured. Figure 4 shows the CDU data of the first and second litho patterns throughout the double patterning process. The 3σ of the first litho pattern after the second layer patterning was 1.62 nm, and that of the second litho pattern itself was 1.35 nm. These values are less than the required 2.5 nm CDU target for the XT1900i, and therefore the self-frozen process exceeds requirements for actual device fabrication.

3.3 Patterning and CDU of 40 nm H/80 nm P contact holes (CH)

Formation of 40 nm H/80 nm P contact hole was carried out with Nikon NSR S610C (NA = 1.30, dipole) according to the procedure described below:

i) The 40 nm S/80 nm P LS first litho pattern was formed by a standard positive lithographic process.

ii) Freezing bake was applied to the first pattern.

iii) The 40 nm S/80 nm P LS second litho-pattern was formed on perpendicular to the first patterns. Formation of 40 nm H/80 nm P CH was successfully achieved. Resulting 40 nm H/80 nm P CH pattern was shown in Fig.5.

![Fig. 3 Top-down and X-Sectional images of 26nmL/52nmP pattern](image)

![Fig. 4 CDU data of the first line (left) and second line (right) after second litho in 26nmL/52nmP LS pattern.](image)

![Fig. 5 Resulting 40 nm H/80 nm P CH pattern.](image)
Figure 5 Top-down and X-sectional images of 40nmH/80nmP CH pattern

Figure 6 CDU data of the first space (left) and second space (right) after second litho in 40nmH/80nmP CH pattern.

Figure 6 shows the CDU data of the first Y space and second X space in each process step of patterning the respective 40 nm H/80 nm P CH. The 3σ of the Y space after second litho was 2.90 nm, and that of the X space after second litho was 2.96 nm. The CD uniformity of the litho pattern was kept within 4.0 nm through each double patterning process step. The lithographic performance of non-TC self-freezing resist on 40 nm contact holes is also adequate for actual device fabrication.

3.4 Defect results of 35nm L/70nm P pattern by double patterning

Figure 7 shows the first defect inspection result of the non-TC self-freezing process conducted on 35 nm H/96 nm P CH, which showed 0.61/cm² as defect density (D.D.). Further optimization of exposure and coating settings is needed, but this result indicates that the double patterning process with non-TC self-freezing resist is expected to be usable at the manufacturing level.

3.5 Defect results of 48nm H/96nm P CH pattern by double patterning

Figure 8 shows the first defect inspection result of the non-TC self-freezing process conducted on 48 nm H/96 nm P CH, which showed 1.30/cm² as defect density (D.D.). This result also indicates the non-TC self-freezing resist is expected to be available at the manufacturing.

3.6 Processing properties on multilayer including JSR spin-on glass (SOG) and spin-on organic hard mask (SOH)

Pattern transfer on to SiO₂ was done to better understand the processing properties as they would apply to actual device manufacturing. Considering that the resist thickness decreases as the target pattern size shrinks, a multilayer
process is one of the promising items in terms of enhancing precise pattern transfer. The demonstration was carried out on SOH as such a process which is most attractive from the view point of cost of ownership.

First, SOH was coated on a SiO₂ substrate. Subsequently, SOG was coated on the SOH film. Formation of the 48 nm H/96 nm P CH and 32 nm L/64 nm P LS pattern were carried out on the SOG film substrate, as mentioned above. Etching results of these patterns were shown in Figure 9. These both patterns were accurately transferred on to the underlying SiO₂ substrate. These results showed the feasibility of the system, and how it can apply to actual device manufacturing.

![Figure 9 Pattern transferring results of 48 nm H/96 nm P CH pattern and 32 nm L/64 nm P LS pattern on to SiO₂ with JSR multilayer system.](image)

4. Conclusions

In this study, simplified double patterning process with non-TC self-freezing resist was demonstrated. For non-TC self-freezing resists, the solubility resistance toward the second lithography process was accomplished via one bake. Formation of the 26 nm L/52 nm P LS and 40 nm H/80 nm P CH were successful. The resulting CDU was first/second = 1.62 nm/1.35 nm for LS and first/second = 2.90 nm/2.96 nm for CH which meet or exceed requirements for high volume device manufacturing. Defect inspection was also carried out on 35 nm L/70 nm P and 48 nm H/96 nm P CH, and these D.D. were 0.61 and 1.30, respectively. Additionally, pattern transfer on to SiO₂ using a multilayer system was demonstrated, succeeding in transferring 48 nm CH and 32 nm LS on to the underlying SiO₂ substrate accurately. These results showed the feasibility of this double patterning system can be applied to actual device manufacturing.

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References


