EUVL Challenges towards 1x nm Generation

Suigen Kyoh, Yumi Nakajima, Shinya Watanabe, Tsubasa Imamura, Toshiyuki Sasaki, Mitsuhiro Omura, Kazuo Tawarayama* and Kentaro Matsunaga*

Device Process Development Center, Toshiba Corporation
8 Shinsugita-Cho, Isogo-Ku, Yokohama 235-8522, Japan
* Advanced Memory Development Center, Toshiba Semiconductor Company
800 Yamanoissiki-Cho, Yokkaichi, Mie 512-8550, Japan

EUVL applicability to mass production in 2x nm generations has been proved by recent developments. For 1x nm generations, three major lithography candidates to be applied for mass productions are discussed, quadruple patterning, EUVL single patterning and EUVL double patterning. Three candidates are compared from following viewpoints, lithography performance, process cost and turn around time. Through the comparison, EUVL is the most promising way to 1x nm generations. EUVL single patterning has an advantage of cost and TAT and EUVL double patterning has a potential to extend resolution limit to 0x nm hp.

Keywords: EUV, quadruple patterning, double patterning, cost, TAT

1. Introduction

Semiconductor industry has won continuous revenue growths by spreading semiconductor device applications. It is always the goal in the past, now and future that realizing higher performance with reduced costs. Scaling had always been one of main drivers to accelerate toward the goal. Nevertheless, scaling requirement seemed to stand at the corner in this several years. Especially in memory device, there are some options to aim at the goal, 3D-devices, for an example. If 3D-devices becomes main stream of memory devices, will scaling requirement be relaxed? The answer may be no, because scaling will certainly bring fruitful business successes even in 3D-devices.

Referring ITRS roadmap, scaling will be proceeded in all devices, DRAM, MPU and Flash memory shown in Fig.1. In each half pitch generation, proper lithography technology will be applied from the performance and cost viewpoints. In 2011, it is the transition timing from immersion to double patterning. Double patterning will reach its physical limitation after several years. We think EUVL is the most promising technology for 1x nm generation beyond the limit of double patterning.

2. Status review of EUVL for 2x nm hp

Before discussion of 1x nm hp, status of EUVL for 2x nm hp is reviewed. Good critical dimension (CD) uniformity of 28 nm lines and spaces (L/S) pattern was achieved in both intra shot and inter shots, 3.7 nm and 1.8 nm at 3σ, respectively. These are results of alpha version exposure tool, Nikon EUV1, so we think there are rooms for more improvements. Resolution results, chemically

![Fig.1. Device scaling roadmap and applied lithography technology](image1)

![Fig.2. CA resist resolution chart](image2)
amplified (CA) resist of 50 nm thickness, are shown in Fig.2. The wafer was exposed with 0.3 numeric aperture (NA) and off axis illumination. In 24 nm L/S, good resist profile was obtained and in 20 nm L/S resist modulation was observed. The exposed dosage was 14.6 mJ/cm² and this value would be practical for manufacturing usage.

Yield vs. half pitch (Length: 0.7 mm)

Fig.3. Yield improvements of electrical test site

To grasp the maturity of EUVL as a total lithography system, electrical test site have been evaluated applying the alpha version exposure tool². The history of yield improvements is shown in Fig.3. Successful enhancements of yield and scaling down were achieved. In latest results, yield of 26 nm L/S was obtained. As shown, exposure tool exhibited good performance and resist had an ability to resolve 2x nm pattern. Manufacturing of 2x nm generation device applying EUVL will be in the scope of semiconductor industry.

3. Three Candidates for 1x nm hp lithography

For challenge toward 1x nm half pitch, we have three major technology candidates. First one is Quadruple patterning with ArF immersion. Second one is EUVL single patterning. And third one is EUVL double patterning. Simplified process flows of quadruple patterning and EUVL single patterning are shown in Fig.4. EUVL double patterning is easily supposed so omitted. Though obtained patterns are same between these two technologies indexed as “Processed”, mask and resist pattern are relaxed in quadruple patterning. In EUV lithography, the process flow is very simple, the processed wafer can be obtained by one lithography and one etching.

4. Comparison among the candidates

To make a comparison among those three candidates, basic viewpoints are selected. First viewpoint is lithographic performance. When some technology is applied for production, the technology should be satisfied technical requirements. Second viewpoint is process cost. Process cost is so important that reduction of process cost will brew profits from semiconductor business. Third viewpoints is turn around time of process flow. Turn around time of process flow has been focused not so often, but turn around time is also important in stock operations.

4.1. Lithographic performance

In lithographic performance, comparison is made upon resolution and CD uniformity.

4.1.1 Resolution Limit

A simple chart, Fig.5, shows feature size corresponding of each technology. If resolution limit of ArF immersion lithography is set as 40 nm, quadruple patterning can cover the size from 20 nm to 10 nm. It also can be applicable to larger feature size than 20 nm, but double patterning can cover that area. Resolution limit is defined by that of ArF immersion, so 10 nm hp is the resolution limit on quadruple patterning. In EUVL single patterning, there is no clear resolution limit. Of course, it has optical resolution limit. Nevertheless, real limitation is defined mainly by resist blur. In EUVL double patterning, it can double the pattern frequency. If the...
resolution limit of single exposure is 16 nm half pitch, we can obtain 8 nm half pitch by EUVL double patterning.

Hereafter, the challenged results to enhance the resolution limits are reviewed. The outstanding results of quadruple patterning were reported by Yaegashi-san. Good pattern profile of 11 nm half pitch was obtained by quadruple patterning.

EUVL single patterning results for ultimate resolution are shown in Fig. 6. Pattern of 15 nm half pitch is modulated applying dipole illumination.

Fig. 6. EUVL single exposure results

Current image quality of EUVL single patterning in 1x generation is not enough for manufacturing. Resolution limit will be extended by improvement of image contrast and resist materials. We think resist blur improvement is most effective for enhancing resolution limit. Figure 7 shows how much we should improve resist blur for 1x generation in EUVL single patterning. Horizontal axis is pattern half pitch and vertical axis is normalized intensity log slope (NILS), target of NILS is set to 1.0 for 10% exposure latitude. Background color indicates resolution limit of each NA. Each solid line shows resist blur from 5 nm to 10 nm. A right cloud spot is current status, 0.25 NA and resolution limit is 20 or 22 nm half pitch. So, nm, reduction of resist blur to 5 or less is required, this seem to be a big challenge for resist improvements. Moreover, higher NA more than 0.32 is also required.

Figure 8 shows an example of EUVL double patterning. Top of the figure is a resist image of 32 nm pattern by EUVL exposure. And we obtained 16 nm half pitch by combining EUVL and double patterning technology. Recently we obtained very good image of 20 nm half pitch applying a beta-version exposure tool. We are now trying to form 10 nm half pitch.

4.1.2 Estimated CD uniformity

Uniformity of CD is estimated under some error assumptions. Assumed errors are as following. 7% error of half pitch is assumed to both lithography and reactive ion etching process. Also, 5% error of half pitch is assumed to slimming and spacer film deposition process. The CD variation results are presented in 18 nm half pitch and 12 nm half pitch. Comparison between quadruple and EUVL single are made in 18 nm half pitch. And

Fig. 9. Estimated CD uniformity

comparison between quadruple and EUVL double are compared in 12 nm half pitch. In quadruple and double patterning, CD errors will be different from each other because pattern edge is formed by different process. So, we plotted the most critical
CD variation in this figure. When we set uniformity target as 15% of half pitch, EUVL can fulfill the uniformity target both in single and double patterning. Nevertheless, quadruple patterning cannot achieve the target. Because CD variation of each process is piled up, there should be disadvantage in quadruple patterning of complicated process. On the contrary, EUVL of simple process has an advantage in CD uniformity.

4.2. Process costs

Second viewpoint of comparisons is process costs. Comparison will be made upon cost of ownership (CoO). EUVL single patterning is best because of its process simplicity. On the contrary, quadruple patterning is not so good by its process complexity. The estimated results of cost of ownership are shown in Fig.10.

![Cost of Ownership Comparison](image)

Fig.10. CoO comparison

Vertical axis is relative CoO, and each CoO is normalized with that of quadruple patterning. It should be noticed that these results strongly depend upon device and process flow. So, the results are not universal. In the case of our estimation, EUVL single patterning can reduce CoO by 20% from quadruple patterning. Lithography cost is highest in EUVL double patterning, it also have a slight cost advantage to quadruple patterning.

4.3. Turn around time

Third viewpoints is turn around time (TAT). In TAT discussion, period of wafer processing is focused on. TAT is shortest in EUVL single patterning, because the number of process step is smallest. Short TAT gives various advantages both in development stage and manufacturing stage. Short TAT brings short development time, so total development time can be reduced. Finally it results quick release the new products to the market. In manufacturing stage, shorter TAT makes it possible to respond to the market needs quickly. Discussion will be made about manufacturing control hereafter. TAT of wafer processing is assumed to be proportional to the number of process steps. For quantitative discussion, representative index are introduced. We apply a relative number of process steps in quadruple patterning normalized by the number of EUVL single patterning process steps. The number of critical layers and the number of “other process” is depend on device, design, structure, etc. So the value of the index also depends on device, design, structure so on. ROQ is parameterized and set to 1.05 and 1.10 as a plausible value. Manufacturing control is simulated with varying an amount of spot order. Spot order was assumed to change randomly in short term and cyclically in long term. Input wafer lot is calculated to maintain a stock of product to a target value with considering current stock and product to be output. Manufacturing manager should decide how much the input wafer lot is. He is always worrying about that because he cannot forecast how much spot order will be in the future.

Changes in stock of product with time are calculated in each technology. Figure 11 is the example of results in quadruple patterning ROQ=1.1. From those results, three values are extracted for comparison, average stock, deviation of stock and maximum stock. These comparisons in Fig.12 show

![Changes in Stock of Product](image)

Fig.11. Changes in stock of product

![Stock Comparison](image)

Fig.12. Stock comparison
that fewer stock is required in EUVL. This results means EUVL of simple process has a great advantage in manufacturing control.

4.4. Technology strategy through comparison

Through these comparisons, what can be said on technology strategy? EUVL single patterning has an advantage of cost and TAT. EUVL double patterning has a potential to extend resolution limit to 0x nm hp. So, EUVL single patterning first and when resolution limit has come, switch to EUVL double patterning. This seems to be better strategy through the comparison I have made.

5. Conclusion

EUVL applicability to mass production in 2x nm generations has been proved by recent developments. For 1x nm generations, three major lithography candidates to be applied for mass productions are discussed, quadruple patterning, EUVL single patterning and EUVL double patterning. Three candidates are compared from following viewpoints, lithography performance, process cost and turn around time. Through the comparison, EUVL is the most promising way to 1x nm generations. EUVL single patterning has an advantage of cost and TAT and EUVL double patterning has a potential to extend resolution limit to 0x nm hp.

Acknowledgements

Authors thank to S. Tanaka, T. Takaki and Y. Arisawa for fruitful discussions. And authors also would like to thank to Y. Hayashi for helpful test-site measurements.

References

1. International Technology Roadmap for Semiconductors (2009) Table B “Key Lithography-related Characteristics by Product”