Roll-to-Roll UV Imprint for Bottom-up Transistor Fabrication

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We propose a design to fabricate transistors on flexible substrates in a bottom-up fashion using R2R UV-imprint lithography. The design consists of a template composed of multilevel as well as gray level features, the later used to facilitate device interconnection. A hard mold is fabricated by LBR and a flexible Ni replica is done using Ni electroplating. The flexible stamp is used in the R2R UV imprint machine with PET as flexible substrate. Imprints were performed at a speed of 0.35m/min and show a high level of replication of the multilevel as well as gray level features.

Keywords: nanoimprint, R2R imprint, self-alignment, bottom-up transistor

1. Introduction

Flexible electronics is becoming more and more popular lately. Industries of ICs [1], paper [2] and surface texturing [3] have designated flexible electronics as the market with the highest business potential. One of the challenges of flexible electronics consists in the processing and handling of the used flexible substrates. Substrate handling is performed by approaches such as sheet-to-sheet, free handling and on roll-to-roll (R2R). R2R handling seems to be the most appropriate in terms of high volume manufacturing. Another issue of the flexible substrate is the low dimension stability with respect to humidity, temperature and handling. Several methods have been proposed to overcome the poor overlay performance of nanoimprint lithography, the most known being the SAIL (Self Align Imprint Lithography) process proposed by HP [4]. In the SAIL process, a multi-level imprint is performed on a foil prepared with a stack layer. The transistor structure was created by etching selectively thanks to the multileveled design. Nevertheless, some issues, such as the residual layer removal step and metal evaporation on foil still remain to be addressed with this approach.

2. Results and discussion

Holst developed a new approach to solve the issue of residual removal and metal deposition on foil by combining a bottom-up approach with a “smart” stamp for the lithography step [5]. The “smart” stamp concept refers

to stamps whose profile contains multi level as well as grey level parts. The slope provides means for electrical connection to the buried gate. Therefore, self-alignment of the different parts of the devices is achieved. The residual layer does not need to be removed and any materials deposited in further steps can be added in liquid phase in a bottom-up fashion.

Figure 1 shows the process flow, cross-section, top-view and tilted view, to fabricate such transistor. The first step, Figure 1a, is the only lithography step of the process, consisting of two-level, grey-level imprint. The first level consists in three contact pads for electrical connections as well as connecting lines for source and drain. The second level corresponds to the gate area. A slope, created by grey-level lithography, connects the buried gate at level two to the contact pad on level one.

The next step, Figure 1 b, is the metallization step where contact pads and connections are covered with a thin layer of metal, typically 50 nm thickness. A thin insulator layer is then deposited, Figure 1 c, on the corresponding gate area, typically with a thickness of 5nm. The last step, figure 1 d is the deposition of the semiconductor, in this case organic, on the corresponding gate area.

The fabrication techniques investigated for the process mentioned above are: 1) R2R UV-imprint of the “smart” design, 2) deposition of metallic part using ink-jet printing of nanoparticles (NPs) ink, 3) NPs sintering,

Figure 1. Scheme representing the process flow to create the smart transistor with cross-section, top-view and tilted view.

4) depositing of insulator in liquid phase, 5) depositing of liquid molecular semiconductor i.e. pentacene by ink jet printing using capillary forces to deposit the material in small areas and 6) encapsulating. All these techniques to fabricate such transistor are investigated at Holst on Foil-on-Carrier and Sheet-to-sheet fashion.[3] In this paper we will only show the first fabrication step of such a device, namely the lithography step, using R2R imprint, to pattern the foil.

The first step of the process consists in fabricating the hard mold with all the functionalities mentioned above. It was made using Laser Beam Recording lithography (LBR) on an 6 inch wafer covered with photoresist. The design consists at the 1st-level in 3 contact pads of $200 \times 200 \mu\text{m}$, depth 15 nm. These pads are connected to the source, drain and gate by $50 \mu\text{m}$ width line. Source and drain consist of $50 \times 150 \mu\text{m}$ line pads. The gate area is at the 2nd level, 50 nm deep and consists of a rectangle of $20 \times 100 \mu\text{m}$. The gate is connected to the contact pad via a “slope” made using grey-level lithography. The ‘slope’ consists of 5 discrete steps of 10, 15, 50, 90 and 100 nm. The hard mold is used to make a thin Ni replica, 50 μm thick using Ni electroplating. The flexible stamp has the conformal opposite feature than the one of the hard mold. The stamps consist of a Ni 6 inch wafer with 2 rows of transistor with different channel length. No surface treatment was applied on the stamp.

Figure 2a shows optical microscopy of the Ni stamp with the multilevel design. The three contact pads are labeled source, drain and gate at the 1st level

Figure 2. a) optical microscopy image of the flexible Ni stamp with 2 level features and grey slope and b) AFM image of the transistor design area.

with 15 nm height. A slope connects the gate contact pad to the working area that is protruding at 265 nm height. Figure 2b shows AFM imaging of the working area. The structures are protruding from the surface, leading to a positive type of stamp. This configuration is the most appropriate for high quality imprint replication. The Ni flexible stamp is then attached on the main drum of the R2R UV imprint tool.

The Roll-to-roll UV imprint tool consists of a R2R handling system provided by Coatema and a custom-made UV-imprint unit featuring an embossing drum, an exposure unit to cure the resist, and a resist dispensing system. Figure 3a shows the complete R2R UV-imprint tool. The process is as follow: Foil is unwound through the unwinding unit (a), then b) resist is applied using a drop-casting unit, c) foil with resist is put in contact with the stamp by a soft drum, resist is cured via UV illumination, foil covered with resist is removed from the

Figure 3. a) photograph of the R2R UV-imprint system, b) picture from the patterning drum consisting of a flexible stamp attached to the drum, c) scheme of the R2R UV imprint process.

stamp and d) foil with imprinted resist is wound on a drum. The foil used is 20 μm thick commercial PET foil from Agfa with a special coating to improve resist adhesion on the foil. The web speed has a range from 0.1 m/min to 2 m/min. The resist is a solvent free resist from Microresist with low viscosity less and low shrinkage. an average drop is of 8.3 μL . 1 μm thick resist thickness is obtained this way after patterning and curing the resist.

Figure 3b shows the imprinting unit. The patterning drum consists of the Ni flexible stamp attached on a 300 mm diameter drum via magnetic attachment. The illumination unit is place underneath the patterning drum and delivers a variable power up to 2 W.

A schematic version of the complete process flow can be seen on Figure 3c including post-processing that will be implemented in a further step.

Figure 4 shows the R2R imprint results using the “smart stamp”. The lack of contrast is due to the nature of the substrate, namely transparent foil and resist that are not reflective as compared to Ni. Figure 4a, b and c reveals a confocal optical image of the fifth imprint made during the run. Previous test were already performed using

the gate area and the connecting slope are clearly visible. The contact pad with a depth of 15 nm is less visible but clearly well replicated. Figure 4b shows a close-up of the top-view of the working area. The source, drain and gate area show the 2 different level. The discrete steps of the slope are highly replicated as well.

Figure 4 c and d shows 3D viewing the imprinted transistor design. To investigate the replication of the slope, AFM was used, see Figure 4d. The fidelity of the replication of the slope area, which is the most complex, is high. Both levels were replicated even though the first level is more difficult to investigate due to the low contrast of the shallow profile (15 nm). The inspection of the imprints on the foil were made by visual inspection and by optical microscopy for 1st, 5th, 10th and 20th imprints. Visual inspection and optical microscopy were also used to observe the stamp after 20 imprints and neither sticking nor damage was observed. These results indicate the high potential of R2R UV-imprint as a way to replicate 3D features on high volume fashion and as a promising candidate for R2R lithography.

3. Conclusion

Complex stamps were fabricated to allow combining all lithography steps in a single one for bottom-up transistor fabrication. The stamps have two levels as well as a slope to connect the buried gate to the contacting pad. The design was successfully replicated by Roll-to-roll UV imprint lithography.

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Figure 4. R2R UV-imprint of “smart” transistor design on foil covered with UV-curable resist, a, b) confocal microscope images of the top-view of full transistor imprint including connected contact pad and zoom-up of the working area and c) 3D image of the imprinted transistor design, d) optical image of the imprint with AFM pictures of different areas taken on the slope.

multi-level template and demonstrated high quality 3D replication [6]. The novelty here consists in having a grey-level slope to imprint. The deepest level, corresponding to