Important Challenge for Optical Lithography Extension utilizing Double Patterning Process

Hidetami Yaegshi, Kenichi Oyama, Kazuo Yabe
Shoichi Yamauchi, Arisa Hara and Sakurako Natori

Leading-edge process development center, Tokyo Electron LTD.
650 Mitsuzawa, Hosaka-machi, Nisaki-cty, Yamanashi 407-0192, Japan

Lithographic scaling has been driven by improvements in wavelength and numerical aperture historically. In the semiconductor industry, the H2O base 192 immersion technique has been main exposure tool combined with various low-k1 techniques, such like off-axis illumination, phase-shift mask and so on. The focus is now on double patterning techniques (DPT) as a means to circumvent the limitations of Rayleigh's definition. Actually, self-aligned spacer double patterning (SADP) has already been employed in high volume manufacturing of NAND flash memory devices. This paper introduces demonstration results focused on the extendibility of double patterning techniques for downward scaling and various device layouts utilizing SADP (Self-aligned Double patterning) mainly.

Key words: Double patterning, SADP, Pitch Quadrupling, 11nmhp, RDR, Resist-core

1. Introduction

There are two main types of double patterning technology: pattern-splitting type and self-aligned type (Fig-1). The pattern-splitting type suffers from a variety of problems such as the need for high overlay accuracy and improvements to pattern division, optical proximity correction (OPC), and other processes. On the other hand, the self-aligned type (SADP), which is typical of spacer processes, can easily form fine and repetitive line patterns, and it has come to be applied mainly to memory devices as a result.

SADP requires that an error budget for ensuring critical dimension (CD) controllability be clarified. This is because the SADP process incorporates etching and deposition as process steps in addition to conventional lithography. Here, it is desirable that process scheme be simplified to improve CD controllability. The double patterning technique, in particular, must consist of simple processes to avoid the problems associated with an increase in the number of process steps. Our proposed technique is reliable enough to achieve a 20-nm half-pitch (hp) with very few process steps as shown in Fig-3[1]. The remarkable feature of this process is the adoption of a SiO2 film that can be deposited at extremely low temperatures for spacer formation. Additionally, as it can be deposited at temperatures below resist Tg, it can be used as the core material in spacer formation. In short, there is no need here for newly optimizing deposition or etching processes. This SiO2 deposition technique uses atomic
layer deposition (ALD) featuring high film-thickness controllability and good step coverage. The etching process also requires high process controllability.

We have already applied this simple SADP scheme to fine pattern processing with good results. An example of ultimate down scaling is shown in Fig-2. In this demonstration, we achieved “pitch quadrupling” by repeating the SADP step two times and successfully obtained 11-nm-hp pattern resolution.

We have also used SADP application technology, which has recently come to be called “complementary lithography,” to demonstrate the formation of a 20-nm SRAM gate pattern, and have shown that this process can be useful not only for memory devices but for logic devices as well (Fig-3). [2]

![Fig-3 SADP scheme and test results](image)

a) Resist pattern (40nm hp)
b) Hard mask pattern (20nm hp)

More recently, we have taken a big leap from past demonstration results in an attempt to expand the fields that can use complementary lithography. This paper presents a number of remarkable results reflecting our ongoing pursuit of down scaling and complementary lithography.

2. Experimental Conditions

Process tools that used in this examination are listed in Table 1.

<table>
<thead>
<tr>
<th>Process step</th>
<th>Experimental condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Exposure</td>
<td>NSR s610c(Nikon) NA:1.30</td>
</tr>
<tr>
<td>Track</td>
<td>CLEAN TRACK LITHIUS pro-i+(TEL)</td>
</tr>
<tr>
<td>Resist</td>
<td>193nm resist and organic BARC</td>
</tr>
<tr>
<td>Etching</td>
<td>Tactras (Tokyo Electron LTD)</td>
</tr>
<tr>
<td>CVD</td>
<td>TELINDY PLUS (Tokyo Electron LTD)</td>
</tr>
<tr>
<td>CD measure</td>
<td>CG-4000 (Hitachi)</td>
</tr>
</tbody>
</table>

3. Results and Discussion

3.1. Scalability of SADP ~ Pitch-Quadrupling

We could examine this simple SADP scheme to fine pattern processing with good results. An example of ultimate down scaling is shown in Fig. 4[2]. In this demonstration, we achieved “pitch quadrupling” by repeating the SADP step two times and successfully obtained 11-nm-hp pattern resolution.

In order to mitigate any process variation, this complicated Pitch-Quadrupling scheme has to be simplified. We tried to omit the sacrificial film stack for core-pattern formation, and finally any additional film stack could be skipped as shown in Fig-4. After process stabilization, CD uniformity across wafer and LWR (Line-width-roughness) was measured. CD uniformity reached to 0.3nm on 3Å, and LWR achieved to 1.2nm.(Fig-5,6)

![Fig-4 Pitch-Quadrupling](image)
a) Resist pattern (45nm hp)
b) Hard mask pattern (11nm hp)

![Fig-5 Refined PQT demonstration result](image)

(PQT: Pitch Quadrupling technology)
3.2, SADP complementing techniques

3.2.1. Island pattern (SRAM gate)

We have used SADP application technology, which has recently come to be called “complementary lithography,” to demonstrate the formation of a 20-nm SRAM gate pattern, and have shown that this process can be useful not only for memory devices but for logic devices as well (Fig-5).

We present an example of the proposed spacer DP process application to the fabrication of island patterns. In this regard, the litho-etch-litho-etch (LELE) process was previously shown to be a prime candidate for DP technology that could respond to the down scaling of SRAM patterns in logic devices.[4] This process, however, is complex and requires that exposure tool have high overlay accuracy. We here present the results of our attempt at fabricating island patterns using the straightforward scaling characteristics of the spacer DP process introduced here. Process flow is shown in Fig-8. First, the spacer DP process was used to fabricate a 20-nm periodical line pattern. This was followed by the fabrication of a slit pattern orthogonal to this line pattern in a lithography step. We consider that a slit width of about 20 nm will be required for SRAM layout in the 15-nm node. However, current exposure equipment with a numerical aperture of 1.35 can only resolve slit spaces of about 45 – 50 nm. It was therefore necessary to use CD-shrink technology here. In this experiment, we employed a shrink technique based on low-temperature SiO2 film formation having a proven record as hole-shrink technology. Next, after application of this shrink technique, a pattern having 20-nm slit space was fabricated. Finally, this slit pattern was used as a mask to subject part of the underlying line pattern to an etching process, and an island pattern was formed.

![Fig-7 Spacer and cutting process for SRAM gate like pattern](image)

3.2.2. Trench Pattern

![Fig-8 Spacer and cutting process for short trench pattern](image)

3.2.3. 2D Pattern Application

Considering that SADP technology might be useful for pitch doubling not only in line patterns but also in elbow patterns, we tried applying it to the formation of complex layouts. As shown in Fig-9, a 22-nm-hp pattern was successfully formed from a 44-nm-hp elbow pattern (photo-resist) through SADP processing.[3] A complex 2D pattern was also formed by pattern cutting in a 2nd lithography step. These results demonstrate that complementary lithography using SADP can be applied to complex 2D patterns in addition to single orientation layouts.

In this test, we compared the resolution performance of two types of photo-resist in the cutting pattern. We did this because there are known examples of slit patterns in which higher optical contrast can be obtained under bright-field exposure conditions than dark-field ones. We therefore used existing positive-tone resist under dark-field conditions and negative-tone resist under bright-field conditions to compare resolution performance. The results of this comparison showed that pattern resolution performance excelled with negative-tone resist (bright-field mask) in agreement with simulation results. Although it was verified that equivalent resolution performance can be achieved with positive-tone resist by adding some insertion of shrink technique after the lithography process, the use of negative-tone resist appears to be preferable from the viewpoint of reducing process cost.(Fig-9,10,11)
3.3. DSA combined SADP

Current 193-nm water-based immersion lithography has a resolution limit near 40-nm hp, and to obtain resolutions of 20 nm and beyond, pitch-tripling and pitch-quadrupling techniques will have to be used. Currently DSA (Direct self-assembly) technique has been discussed aggressively for next generation lithography candidates.

Methodology of DSA pattern formation can be classified in two type, which are “Grapho-epitaxy” and “Chemical- epitaxy”. SADP technique is very reliable method to fabricate the guide for Grapho-epitaxy. Any size and space pattern can be fabricated using SADP as shown in Fig-12.

In this study, Poly-styrene and PMMA block copolymer was used. PS-b-PMMA was applied on topologic substrate with guide fabricated through SADP scheme and annealed under 250°C. 12nm half-pitch DSA pattern could be described between guide pattern after RIE process step. (Fig-13)[4]

3.4. Hole application

In contrast to the above two schemes, Tokyo Electron recommends a shrink method that directly deposits a SiO₂ film on a resist pattern. By virtue of using low-temperature ALD-CVD, this method features film deposition that does not damage the resist and good step-coverage controllability resulting in good shrink characteristics. Furthermore, it is known from technical presentations and reports that schemes that directly deposit film on a resist pattern are reliable and have a good track record since they use a technique that deposits the spacer film on a resist core pattern in self-aligned double patterning (SADP).

Figure 8 shows the results of transcribing holes and trenches on a tetra-ethyl-ortho-silicate (TEOS) layer for a tri-layer structure by etch shrinking, chemical shrinking, and SiO₂ shrinking. In each of these demonstrations, the process is applied to both contact-hole (CH) patterns and rectangle patterns (short-trench patterns). It can be seen from these results that processing by SiO₂ shrinking reduces the loading effect during shrinking and the effects of etching loading, which makes for stable process transcription. This property suggests that the SiO₂-shrinking scheme can be a very effective technique for cases in which various types of patterns coexist as in logic-system wiring.

3.4.1. Hole-shrink technique

In double-patterning application for hole pattern, hole shrink technique must be key elemental process step as well as line slimming in pitch-doubling for line pattern. Hole-shrink technology for contact patterns can be broadly divided into the three schemes.

The chemical assist scheme enables batch processing by a lithography process, but for 30-nm hp patterns, miniaturization and shape control become increasingly difficult. The tapered-etching scheme, meanwhile, has a cost benefit since it features the same number of process steps as existing processes, but since it achieves pattern shrinking by tapered shaping, line-width control is an issue. (Fig-14)
4.2 Double patterning for hole pattern
Achievement of our demonstration in various double patterning for hole pattern is summarized in Table-2. Each technique have pos and cos, therefore it might be employed on the kind of devise requirements. [5]

Fig-14 Linear property of SiO2 depo.

Conclusion
At present, photographic scaling has been advancing steadily in conformance with Moore’s Law, and while the industry waits for the completion of next-generation EUV tools, the 193-nm immersion process is still the prime technique. Double patterning and especially SADP is the best approach to extending the 193-nm process. The SADP process requires no high-precision overlay control as in the pattern-splitting type of double patterning represented by the LELE and LLE schemes and features simplified forming of fine patterns. With SADP, the ultimate in miniaturization has actually been achieved as described in this paper. The SADP process constitutes a technology that can be adapted even to single-orientation layouts expected to be adopted in the future.

With the development of EUV technology running late, complementary lithography has been proposed as one candidate for steadily advancing fine processing. Optimal techniques centered about SADP, which is optimal for pitch doubling, must be intelligently selected. This is our goal in the next phase of our research.

Acknowledgements
The authors would like to extend their appreciation to Tokyo Electron Leading-edge Process Development Center, Technology Development Center, Tokyo Electron AT Technical Development Center, and Tokyo Electron Kyushu Process Technology Department for their support in carrying out the experiments described in this paper.

References