Electrical Via Chain Yield for DSA Contact Hole Shrink Process

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In this study, we conducted electrical via chain yield tests for the purpose of verifying the total process performance of directed self-assembly (DSA) contact hole shrink process. DSA was utilized on the via level connecting between two metal levels. From the analysis of single via resistance data, the best process condition was determined and the via chain yield was obtained. The best yield was 74% at the via chain size of 2.3k and one chip passed the test at the via chain size of 358k. In order to find the root cause of the via chain yield degradation, the failure location was identified by absorbed electron current images and STEM images were taken. It was found that the via did not contact the lower metal level at the failure location. However, we concluded that it was not necessarily caused by DSA process because such failure mode was also observed for the via chains without DSA. Although the via chain size tested at the pre-production stage is much larger by orders of magnitude than the via chain size tested in this study, we believe that significant progress has been made in this study toward semiconductor device manufacturing using DSA contact hole shrink process.

Keyword: directed self-assembly, graphoepitaxy, block copolymer, PS-b-PMMA, hole shrink, via chain yield

1. Introduction

Now that 193 nm immersion lithography has reached its resolution limit, various double patterning techniques are being utilized in the state-of-the-art semiconductor manufacturing fabs. However, double patterning techniques are very complex in terms of design and process. Extreme ultraviolet lithography (EUV) is considered to be the most promising next-generation single patterning solution, however, it still doesn’t satisfy the cost requirement due to the low throughput resulting from insufficient source power. As an alternative lithography technique, directed self-assembly (DSA) became more attractive among patterning researchers and engineers in semiconductor industry. Process of DSA is simple and friendly to conventional lithography process. It consists of coating of blockcopolymers (BCP) on a substrate and annealing on a hot plate to induce micro-phase separation. BCP is known to present various morphologies depending on the total number of segments and the fraction of one block [1]. Many kinds of BCPs are available for research, but the most extensively researched BCP is poly(styrene-block-methyl methacrylate) (PS-b-PMMA), because the synthesis of PS-b-PMMA BCP is relatively easy and mature. In addition, it is able to present useful morphologies such as lamellae or cylinders by changing the fraction of PS thanks to modest $\chi$ parameter. However, because PS and PMMA...
are both purely organic components, it is very challenging to achieve high selectivity in reactive ion etching (RIE) and the pattern transfer process might be problematic [2]. In order to utilize DSA for semiconductor device manufacturing, very low defectivity must be guaranteed. Moreover, critical dimension uniformity (CDU) is also a matter of great importance. In order to verify the total process performance of DSA, sub-30 nm via interconnects were fabricated on a 300 mm wafer using DSA and electrically tested. In our previous paper [3], the initial test results including intra-wafer variation of single via resistance were reported and the correlation between critical dimension (CD) and via resistance was discussed. In this paper, we report on more detailed results of intra-wafer variation of single via resistance for various process conditions, and then go on to via chain yield results and failure analysis results.

2. Experimental

2.1. Fabrication Process

Details of fabrication process have been already reported in our previous paper [3]. The experimental conditions are the same unless otherwise noted. The lower metal level was fabricated using 193 nm immersion lithography and tungsten damascene process (Figure 1 (a)). A 150-nm-thick silicon oxide film was deposited on the lower metal level, and a 160-nm-thick spin-on carbon (SOC) film and a 45-nm-thick spin-on glass (SOG) film were spin-coated on it. On top of the SOG film, a 120-nm-thick positive-tone chemically amplified photoresist was spin-coated and exposed using 193 nm immersion lithography. The exposure of the via pattern was aligned to the lower metal level (Figure 1 (b)). The target CD was 90 nm in diameter. Using reactive ion etching (RIE), the via resist pattern was transferred into the SOG film (Figure 1 (c)), and then into the SOC film (Figure 1 (d)). The target CD was 70 nm in diameter. According to our previous study [4], hole open yield was 100% with the hole CD between 65 nm and 75 nm, although the sample size was as small as 45 holes/chip. The SOC pattern was used as a pre-pattern of graphoepitaxy. A PGMEA solution of PS-b-PMMA (80.5 kg/mol - 34.5 kg/mol) was spin-coated and thermally annealed in two conditions. Some wafers were processed on a hot plate at 240 °C for 60 s in air. All others were processed on a hot plate at 240 °C for 60 s in N₂ atmosphere. The annealing induced micro-phase separation of PS-b-PMMA to form cylindrical PMMA domain in the center of the pre-pattern surrounded by PS domain (Figure 1 (e)).

It must be noted that PS domain exists at the bottom of the pre-pattern. The bottom PS domain needs to be removed by (RIE) prior to oxide RIE. In this study, the removal of the central PMMA domain and the bottom PS domain was processed in one step using O₂ gas chemistry (Figure 1 (f)). Because of the RIE selectivity between PS and PMMA, the surrounding PS domain is partially lost during the PMMA removal, and it is further lost during the bottom PS removal. The remaining height of PS is critical for the success of DSA hole shrink process. Then the via pattern was transferred to the oxide film (Figure 1 (g)) followed by tungsten damascene process (Figure 1 (h)). Lastly the upper metal level was fabricated using 193 nm immersion lithography and tungsten damascene process. The upper metal exposure was aligned to the via level (Figure 1 (i)).

Figure 1. Schematic illustrations of fabrication process

2.2. Via Chain Design

The design of the via chain tested in this
study is illustrated in Figure 2. The width of the lower metal and the upper metal was 300 nm. The overlap length between the lower metal and the upper metal was 300 nm. There was a single via in the center of each overlapped area, which is connecting between the lower metal level and the upper metal level. As the upper metal exposure was aligned to the via level and the alignment marks on the via level might be affected by DSA process, the overlay accuracy between the upper metal level and the via level might be a concern. However, we have verified that the overlay accuracy didn’t change whether to use DSA or not. Moreover, the metal width and the metal overlap length are large enough. The impact on the via chain yield by overlay is absolutely zero in this study. The total number of vias in the via chain is 2.3k, 45.2k, 90.4k and 358k. As reported in the previous paper [3], the measurement of single via resistance was also available.

![Figure 2. Via chain design](image)

3. Results and Discussion

3.1. Dry Development

The process step shown in Figure 1 (f) is called “dry development”, which often contrasts with “wet development” [5]. The processing time was changed between 10 s and 16 s, and the single via resistance was measured (Figure 3). The via resistance variation was very large at 10 s, but it became smaller at 12 s and 14 s. However, it became larger again at 16 s and some vias have very small resistance comparable to the vias fabricated without DSA. In order to see the correlation between the via resistance and the via dimension, the via CD at the process step shown in Figure 1 (g) was measured (Figure 4). At 16 s, the via CD became large especially in the wafer center. It is obvious that the remaining PS film at the process step shown in Figure 1 (f) is almost lost during the dry development at 16 s. Judging from the data discussed above, the dry development was working fine between 12 s and 14 s. In this study, 12 s was chosen as a center condition for dry development. As a way of improving process margin, various solutions are proposed. One of the solutions is wet development, which is capable of removing PMMA domain without damaging PS domain. Process and material optimization is another solution. Sato et al. showed by dissipative particle dynamics simulations that it is possible to realize no bottom PS [6].

![Figure 3. Cumulative probability plot of single via resistance for each dry development time](image)

![Figure 4. Via CD along the diameter for each dry development time](image)

3.2. Annealing Atmosphere

It is a common practice to anneal BCP in nitrogen (N₂) atmosphere because oxygen in air might oxidize BCP and have bad effects on micro phase-separation. We compared...
annealing in air and annealing in N$_2$ in terms of via resistance (Figure 5). We also compared the via CD at the process step in Figure 1 (f) (Figure 6). There was no significant difference in both the via resistance and the via CD. Nevertheless, it might be escalated at higher annealing temperature or longer annealing time. In this study, annealing in N$_2$ atmosphere was chosen as a center condition.

3.3. Over Etch
In this study, the center oxide RIE time was 22 s. By extending the oxide RIE time to 29 s, via resistance variation became smaller although the via CD was almost the same (Figure 7 and 8).

3.4. Via Chain Yield
Based on the single via resistance data shown so far, the best process condition (12 s for dry development, N$_2$ for annealing atmosphere and 29 s for oxide RIE time) was determined and via chain yield was obtained. In order to see the yield impact by via dimension, another via chain whose via dimension is slightly larger was also tested and the via chain yield was obtained. The via CD is shown in Figure 9 comparing between the via chains with the standard sized vias (STD) and the via chains with the large sized vias (LRG). The difference in the via CD is merely 0.8 nm on average. The via chain yield for both via chains is shown in Figure 10. Generally, LRG shows better yield than STD. The via chain yield was 60% for STD and 74% for LRG at the via chain size of 2.3k. It lowered to 8% for STD and 15% for LRG at 45.2k. It further lowered to 3.8% for STD and 3.8% for LRG at 90.4k. At 358k which is the largest size in this study, one out of 78 chips passed the test for STD (1.3%).

3.5. Failure Analysis
In order to find the root cause of the via
chain yield degradation, the failure location was identified by absorbed electron current images (Figure 11) and STEM images were taken (Figure 12). It was found that the via did not contact the lower metal level at the failure location. However, the same failure was also found on the failure analysis for the via chains without DSA (Figure 13). Compared to STEM images at the normal location (Figure 14 and 15), the via dimension at the top didn’t change by the failure. We concluded that the failure was not necessarily
caused by DSA process. Further yield improvement is expected by process optimization.

Figure 15. STEM image of via chain at the normal location (without DSA)

4. Conclusion

In this study, we conducted electrical via chain yield tests for the purpose of verifying the total process performance of directed self-assembly (DSA) contact hole shrink process. DSA was utilized on the via level connecting between two metal levels. From the analysis of single via resistance data, the best process condition was determined to be 12 s for dry development, N₂ for annealing atmosphere and 29 s for oxide RIE time. Then the via chain yield was obtained for the best process condition. The best yield was 74% at the via chain size of 2.3k and one chip passed the test at the via chain size of 358k. In order to find the root cause of the via chain yield degradation, the failure location was identified by absorbed electron current images and STEM images were taken. It was found that the via did not contact the lower metal level at the failure location, but such failure mode was also observed for the via chains without DSA. Further investigation will be required. Although the via chain size tested at the pre-production stage is much larger by orders of magnitude than the via chain size tested in this study, we believe that significant progress has been made in this study toward semiconductor device manufacturing using DSA contact hole shrink process.

References