Readiness of EUV Lithography for Insertion into Manufacturing: The IMEC EUV Program

Eric Hendrickx, Roel Gronheid*, Jan Hermans, Gian Lorusso, Philippe Foubert, Ivan Pollentier, Anne-Marie Goethals, Rik Jonckheere, Geert Vandenberghe, and Kurt Ronse

IMEC vzw, Kapeldreef 75, B-3001 Belgium
roel.gronheid@imec.be

The EUV program at imec aims at identifying the critical issues to prepare EUV lithography for insertion into high volume IC production. The program started in 2006 with the 0.25 NA ASML Alpha Demo Tool and has since then evolved around several focus areas. 1) scanner performance, reliability and monitoring, 2) definition and verification of OPC strategies for generic and EUV specific imaging effects 3) reticle defectivity, focusing on multi-layer defects, reticle handling and reticle cleaning, 4) resist screening, focusing on identification of materials that not only simultaneously give optimal performance in terms of resolution, line width roughness and sensitivity, but that also allow adequate transfer of the EUV-fabricated patterns into the underlying layers and 5) implementation of EUV lithography into fabrication of representative device structures. Since 2011 The Alpha Demo Tool has been replaced by the ASML NXE:3100, allowing higher resolution and productivity. In this paper, selected highlights in the latest achievements of the imec EUV program will be discussed.

Keywords: EUV lithography, scanner performance, reticles, EUV resists

1. Introduction

Insertion of EUV lithography into high volume IC manufacturing has been delayed by multiple nodes. Processing-based technologies to increase pattern density by frequency multiplication, such as self-aligned double patterning [1-3] and directed self-assembly [4-5] are available and have been used to enhance resolution, bridge the gap and continue scaling, while EUV is further readied for production. Despite the delay, availability of EUV lithography for high volume manufacturing is still desired because it can provide high resolution and high pattern quality for random patterns (Figure 1). The EUV program at imec focusses on identification of critical issues for EUV process control and manufacturability. Specifically items such as scanner control, monitoring and stability, resist performance, screening and benchmarking and reticle defectivity performance, handling and cleaning have been evaluated since the ASML Alpha Demo Tool (ADT) became available in 2006 (Figure 2). The work on that instrument initially started at 40nm half pitch feature sizes, and gradually evolved to higher resolution in order to finally resolve 27nm line/space features. Since the NXE:3100 was installed at imec in 2011, the ADT has been decommissioned, and the higher lens quality and more aggressive illumination modes of NXE:3100 have allowed screening of resist materials to 22nm line/space resolution and below.

Figure 1. Estimated area requirements for a representative 14nm node logic cell layout. Assuming 193nm immersion lithography for production of this cell results in an area penalty, which could be avoided when EUV lithography can be used.
In this paper, the status and major recent achievements of the imec EUV program will be discussed [6]. Also the remaining gaps that exist for EUV to be inserted into production will be highlighted.

2. Experimental Details

All results in this paper have been obtained from exposures on the ASML NXE:3100 system that is installed at imec. This system is equipped with an Ushio Laser-assisted Discharge Produced Plasma source. The exposures were performed at 0.25NA using conventional illumination at $\sigma = 0.81$, unless noted otherwise. The EUV scanner is interfaced to a TEL CLEAN TRACK™ LITHIUS Pro™. Wafers were analyzed using a Hitachi CG-4000 or CG-5000 top-down CD SEM.

3. Results and Discussion

3.1 EUV scanner performance

EUV source power and availability continue to be the primary limitations for productivity of EUV scanners [7-8]. Upon initial installation of the NXE:3100 in the imec cleanroom, the initial EUV power provided by the Ushio source met its expectations, but the number of exposed wafers by the system lagged due to availability. As a consequence, a reliability improvement plan was defined and implemented in May 2012 (Figure 3). As can be clearly seen from the graph the system productivity significantly increased since that time allowing for more cycles of learning for EUV insertion. After the reliability improvement plan, the 4-week average uptime was higher than 50% for 19 consecutive weeks.

Figure 3. Plot of the cumulative wafer count as exposed on the NXE:3100 cluster at imec. After the May 2012 reliability improvement on the Ushio source a notable increase in the system productivity is found. By early April 2013 a total of almost 5000 wafers have been exposed.

The NXE:3100 cluster provides for low intra-wafer uniformity of a 27nm line/space test pattern [9] and in addition exhibits excellent long-term reproducibility (Figure 4). An optimized process consistently results in sub 0.9nm 3σ CDU (after correction for intrafield fingerprint) over a period of multiple weeks.
3.2 EUV reticle defectivity and handling

Avoiding particle adders during handling and use of EUV reticles is of critical importance to bring EUV lithography to production. In this respect, care needs to be taken of particle adders to both reticle front- and backside [10].

Particles on the reticle backside or on the scanner reticle clamp, result in local deformation of the EUV reticle and induce intrafield distortions (Figure 5). Since the EUV reticle clamp is in a vacuum environment, there is considerable downtime when a contaminated reticle deposits a particle on the clamp that requires manual removal. Over the 10-month period that spans the plot in Figure 5, three incidents occurred where a particle was left on the reticle clamp. In the latter two occasions, the particle was removed by cycling clean reticles, avoiding the need to break the vacuum.

Since there is currently no pellicle solution available for EUV lithography, also particles deposited on the reticle front side need to be avoided. Typically, these result in hard printing defects that are reproduced on each die. Figure 6 shows the performance of the imec EUV defect

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<th>26/06/2012</th>
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Figure 4. Wafer maps showing intra-wafer CD uniformity (after correction for intrafield fingerprint) for vertical 27nm half pitch line/space patterns as exposed on the NXE:3100. Stable performance in terms of absolute uniformity number as well as wafer signature is found over a period of multiple weeks is found.

Figure 5. Intrafield residual performance over a 10-month period shows three spikes, which are related to a particle being deposited on the EUV reticle clamp. In the last two events the particle was removed without breaking vacuum.

Figure 6. Reticle frontside particle adders over a 14-month period of defect monitor reticle use. The grey band defines an area on the reticle that is not evaluated in this test. Over 14 months of use, 20 particles were deposited on the reticle frontside. Most of these are deposited during wafer exposure. The contribution of adders from reticle handling is smaller.
monitor reticle over a 14-month period. The initial 6 months no defects have been added, but after that several instances occurred, resulting in particle deposition on the reticle front side. Interestingly, most of these are added during the exposure process, although two were identified to stem from reticle handling actions. Currently, hardware improvements on the pre-production scanner are under development to further reduce reticle frontside particle contamination.

3.3 EUV resist screening and requirements

Even though the numerical aperture of the NXE:3100 is unchanged compared to the Alpha Demo Tool, it offers improved resolution. Therefore it allows screening of more advanced EUV resists. In part the improved resolution is caused by lower aberrations of the optics and the higher outer sigma setting ($\sigma=0.81$ for the NXE:3100, compared to $\sigma=0.5$ for the ADT) for the partially coherent illumination. Most importantly, however, the availability of off-axis illumination on this system further extends its use for resist screening (Figure 7). For testing of line/space imaging performance of high resolution

Figure 7. Performance of a typical chemically amplified EUV resist at various illumination settings on the NXE:3100. The off-axis conditions allow resist screening down to 22nm line/space patterns using dipole illumination, while maintaining >100nm focus latitude.

Figure 8. Dose to clear curves using a multi-layer reticle (top) and an aluminum coated blank (bottom). The out-of-band sensitivity is determined from the ratio between both dose to clear values (2.4% in this case).
chemically amplified photoresists, Dipole-X illumination using a 60° opening angle is used, which typically gives a measurable process window for the more advanced materials. Ultimate resolution of the NXE:3100 has been demonstrated at 16nm half pitch using Dipole-X illumination with a 30° opening angle [11].

Recently, focus of the resist screening project has gone to the performance of printing 26nm half pitch contact hole patterns [12, 13]. The screening target for materials in these structures is achieved by using quasar illumination.

Besides the resist screening, there is also more fundamental work ongoing to look into the resist requirements for advanced EUV patterning. Within this frame, a methodology has been set up to quantify the sensitivity of resist to out-of-band (OoB) radiation [14]. Out-of-Band radiation is non-EUV light from the EUV lightsource, and can have spectral components from lasers used in the source or from black-body radiation emitted by the EUV plasma (mostly DUV). Hence EUV lightsources tend to produce some DUV radiation along with the EUV light, and without spectral purity filter in the EUV scanner, the DUV radiation will propagate to the waferplane and impact the resist. EUV resists may be sensitive to this radiation, mainly depending on the photo-acid generator (PAG) that is used in the material.

The methodology to probe the fraction of Out-of-Band radiation that develops the resist is the following: The dose-to-clear for a resist is determined using an EUV multilayer blank (reflecting both EUV and OoB) and an aluminum coated blank reticle (reflecting OoB only). The ratio of these two value is reported as the OoB sensitivity as a percentage. For a standard resist, an Out-of-Band percentage of 2.4% was measured by this method (Figure 8).

In Figure 9 the imaging performance is determined through the average intrafield uniformity of a state-of-the-art EUV resist (SEVR-140) and a resist with an OoB insensitive PAG. The first has an OoB sensitivity of 2.4% and the other 0.32%. Despite this substantial difference in sensitivity, there is little impact on the 3σ uniformity, which demonstrates that the Out-of-Band radiation intensity is sufficiently uniform over the exposure field and does not impact CD variation.

3.4 Implementation of EUV lithography

In order to prove the applicability of EUV lithography in a realistic device manufacturing flow, integration efforts are ongoing at imec [15]. As part of this integration exercise, the fabrication of via chains has been studied (Figure 10).

Figure 9. Average intrafield uniformity for 27nm line-space structures using SEVR-140 and a dedicated OoB insensitive resist. The substantial difference in OoB sensitivity (2.4 vs 0.32%) is not reflected in the resulting 3σ CD uniformity.

Figure 10. Cross-sectional SEM image of the 30nm via chain vehicle that is used to check yield on EUV printed contact holes.
Figure 11. Electrical yield of via chains printed with EUV lithography on the NXE:3100. Shorts are observed for some of the structures with the most aggressive 30nm and 34nm space CD. The electrical failure in these cases is supported by the top-down SEM images (see inserts).

A 30nm target CD for the via was used to connect two metal layers. Trenches of 30nm CD were printed at various space widths and the electrical yield of the resulting via chains was determined (Figure 11). All via chains are yielding as long as the space CD is 36nm or larger. At 34nm and 30nm space CD most of the chains yield, but there are shorts in 10-20% of the chains, resulting in reduced via chain resistance. Note that there is no evidence of closed contact holes, since resistance stays below 100\(\Omega\) in 100% of the measured chains.

4. Conclusions

We have discussed recent highlights of the imec EUV program. The program started in 2006 with the ASML Alpha Demo Tool, which has been replaced by the ASML NXE:3100 in 2011. This system provides excellent imaging capabilities and demonstrates good performance stability. The main remaining challenges for EUV lithography are the availability of a reliable and high power EUV source and in the reticle infrastructure. Regarding to the last aspect, not only the availability of low defectivity mask blanks is critical. Also keeping EUV masks clean on both front- and backside is crucial. Examples are given of random occurrences of particle adders on either side of the mask. Strategies for mitigating such events are under development. The availability of off-axis illumination on the imec NXE:3100 makes the system well suited for resist screening in preparation for higher NA EUV scanners. The current resist screening work focuses on 22nm half pitch line/space structures with Dipole illumination and 26nm half pitch contact holes using Quasar™ illumination. Finally, an example of the EUV implementation work is discussed. Yielding 30nm via chains are printed using EUV lithography, without observing closed contact holes.

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References