Fabrication of Imprint Mold with Nanotrench Patterns by Edge Lithography

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SiO$_2$ nanoline with extremely high aspect ratio could be fabricated by the edge lithography, however, such a high aspect nanoline was fragile. Since nanotrench pattern was stronger than nanoline pattern, a new process was developed for obtaining the Si nanotrench from the SiO$_2$ nanoline in order to obtain a strong nanoimprint mold. A resist nanotrench pattern is fabricated by using only the resist coating and the resist etching. The process is much simpler than the lift-off process. The Si wafer is etched by the modified Bosch process. The fabricated Si trench width and depth are 35 nm and 260 nm, respectively. The Si trench pattern is replicated to polystyrene (PS) film on a silicon wafer by thermal nanoimprint lithography. The PS nanoline, whose width and height are 28 nm and 360 nm, is successfully fabricated.

Keywords: nanoimprint, Si mold, edge lithography, nanoline, nanotrench

1. Introduction

Nano-scale patterns around 10 nm will be required for micro electric device fabrication in near future. Moreover, it is expected that such nanopatterns will achieve various important applications. For example, the efficiency of organic solar cells can be greatly increased by using nanostructures smaller than 20 nm [1]. Therefore, it is of critical importance to develop a cost-effective process for fabricating nanopatterns. Nanoimprint lithography (NIL) is a powerful method for nanopattern fabrication [2, 3]. However, since the mold pattern is directly replicated in the resist film, the dimensions of the mold pattern must be equal to those of the required pattern. The mold pattern is usually fabricated by electron beam lithography (EBL). Although nanopatterns can be fabricated by EBL, the cost of mold fabrication often becomes very expensive because of the long writing time required. Moreover, it is difficult to obtain nanopatterns with high aspect ratio by EBL. Edge lithography is a powerful method for the fabrication of nanoscale patterns [4, 5]. We previously proposed the modified edge lithography technique [6–8], and using this method we were able to fabricate the 25 nm width SiO$_2$ lines with a high aspect ratio of 28 on the silicon wafer [6]. Narrow line patterns with extremely high aspect ratio can be obtained by the edge lithography, however, the nanoline patterns must be too fragile to be used as the NIL molds. When the nanoline patterns are changed to nanotrench patterns, the nanotrench patterns must be stronger than the nanoline patterns and the wafer with the nanotrench patterns can be used as the NIL molds. The changing process of the nanoline patterns (positive tone) into the nanotrench patterns (negative tone) is named as the “tone change” in this paper. The tone change can be often done by the lift-off process. When the lift-off process is used for the patterns by edge lithography, the evaporated metal on the SiO$_2$ lines should be removed. SiO$_2$ can be easily removed by hydrofluoric (HF) acid. Although we tried the Cr lift-off process by using HF acid, Cr patterns after the lift-off were greatly damaged, because the native oxide was formed on the Si wafer and a large part of the Cr pattern even on the Si region must be removed [6].

The new tone change process is proposed in this paper. The main part of the process is the resist nanotrench fabrication from the SiO$_2$ nanoline. The process consists of only the resist coating and the resist etching. It is much simpler than the lift-off process. By using the fabricated resist pattern, the Si nanotrench patterns with high aspect ratio is fabricated. The fabricated trench patterns are transferred to the polystyrene film.
2. Experiments

2.1. Edge lithography process

Since we have already presented the edge lithography process in the previous paper [6], the edge lithography is briefly explained in this section. The process flow is shown in Fig. 1.

(a) Initial patterns for the edge lithography are fabricated on a (100) Si wafer by the modified Bosch process, where the deposition step by C₆F₈ plasma and the etching step by Ar+SF₆+CHF₃ plasma are alternately repeated. The top and bottom of the step pattern are named as IP_{top} and IP_{bottom}, respectively. (b) The patterned Si wafer is oxidized by the dry oxidation at 900 ºC. In the previous paper, the wet oxidation at 900 ºC was used. Since the precise control of the SiO₂ thickness can be easily carried out for the dry oxidation, the dry oxidation is used in this study. When the oxidation time is 4 min, the SiO₂ film thickness becomes about 20 nm. After the oxidation, the SiO₂ film is removed by the reactive ion etching (RIE) of the CHF₃ plasma at the pressure of 1.5 Pa. (c) A conventional positive photoresist (Tokyo Ohka, TSMR V50), whose viscosity is 10 mPas, is spin-coated. The resist thickness on the IP_{top} becomes smaller than that on the IP_{bottom}. The resist is etched by the O₂ RIE at the pressure of 2 Pa. The resist on the IP_{top} is removed but that on the IP_{bottom} must remain. Then, the IP_{top} surface appears, and the IP_{bottom} surface is covered by the resist. (d) The step pattern of the IP_{top} is etched by the SF₆ plasma at the pressure of 13 Pa. Since main etching species are F radicals, the damage for the SiO₂ and the resist films are small. (e) Finally, the residual resist is removed. The narrow SiO₂ lines are obtained on the Si wafer. Since the SiO₂ line height is as high as the initial pattern height, it is easy to obtain a high aspect pattern.

2.2. Tone change process

The process flow of the tone change process is shown in Fig. 2. (a) The process is started from the Si wafer with SiO₂ nanolines. (b) The conventional photoresist (TSMR V50) is spin-coated on the Si wafer with the SiO₂ nanolines. The Si wafer surface is completely covered by the photoresist, but the resist thickness on the SiO₂ line is thin. (c) The photoresist film is removed by the O₂ RIE. It is important that the resist on the SiO₂ nanoline is removed but the resist on the Si wafer remains. (d) After the O₂ RIE, the Si wafer is dipped into HF acid for an hour. When the SiO₂ nanolines is removed, the resist trench patterns are obtained. Then, the tone change process is carried out. Note that the proposed tone change process consists of only the resist coating and the resist etching. It is much simpler than the lift-off process. (e) The Si wafer is etched by Bosch process. Finally, Si mold with high aspect nanotrench pattern is obtained.

The Si wafer with nanotrench patterns is used as the mold for the thermal NIL. After applying a conventional anti-sticking treatment (OPTOOL DSX supplied by Daikin Industries LTD.), the mold is pressed into PS film on a Si wafer. The molecular weight of the PS polymer used in this study is 350 kg/mol. The imprint pressure and temperature are 8 MPa and 180 ºC. The press time is 10 min.

3. Results and Discussions

The initial pattern fabrication is very important. The etching condition is given by the "IP etching"
When the etched line width is greater than 100 nm, deep Si patterns with vertical side walls can be fabricated by using the etching condition [9]. The SEM image of the fabricated pattern after the IP etching (Fig. 1(d)) is shown in Fig.3. The SiO$_2$ line width and height are 20nm and 200nm, respectively. The left side of the SiO$_2$ pattern is the IP$_{\text{bottom}}$ region, and the photoresist remains. The broken line shows the boundary between the resist and the Si wafer.

Next, the results for the “tone change” process are shown. The photoresist is coated on the fabricated Si wafer. The resist thickness is 420 nm for a flat Si wafer under our coating condition. The initial resist thickness is about 2 times as large as the SiO$_2$ nanoline height. The resist thickness is reduced by the O$_2$ RIE. Figure 4 shows the SEM picture after the O$_2$ RIE. The resist thickness is reduced to 200 nm and the SiO$_2$ nanoline appears.

Figure 5 shows the SEM picture after HF acid dipping. The SiO$_2$ nanoline is removed and the resist trench of 20 nm width is obtained. The Si wafer is etched by the fabricated resist mask. First, we use the same etching condition for the initial pattern etching as shown by the “IP etching” in Table 1. However, Si under the resist nanotrench can be hardly etched by this condition. It is considered that the very narrow trench opening is closed by fluorocarbon layer during the deposition step [10]. The etching condition is changed to the “Trench” in Table 1. Comparing to the “IP etching”, the deposition step time is decreased and the bias power for the deposition step, which controls the incident ion energy, is increased in order to reduce the fluorocarbon layer deposition. Figure 6 shows the Si etching result. The trench width and depth are 35 nm and 260 nm, respectively. Although the trench width is slightly increased from the resist mask pattern, the deep trench pattern can be successfully fabricated.

The fabricated Si pattern is replicated to the PS film on a Si wafer by the thermal NIL. Figure 7 shows the fabricated PS pattern. A very narrow PS pattern can be fabricated. The PS pattern width and height are 28nm and 360nm, respectively. Since the width and depth of the Si trench pattern is 35nm and 280nm, the PS pattern width is reduced and pattern height is enlarged by the imprint process. The PS pattern must be stretched during the demolding process [11].

Table 1. Si etching conditions for both “IP etching” and “trench” etching.

<table>
<thead>
<tr>
<th>Recipe name</th>
<th>Step name</th>
<th>P$_{\text{ANT}}$ (W)</th>
<th>P$_{\text{BIAS}}$ (W)</th>
<th>Gas (sccm)</th>
<th>Pressure (Pa)</th>
<th>Time (s)</th>
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<tbody>
<tr>
<td>IP etching</td>
<td>Deposition</td>
<td>600</td>
<td>40</td>
<td>C$_4$F$_8$=100</td>
<td>2.0</td>
<td>5</td>
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<tr>
<td></td>
<td>Etching</td>
<td>600</td>
<td>70</td>
<td>SF$_6$/CHF$_3$/Ar=25/25/75</td>
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<td>8</td>
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<tr>
<td>Trench</td>
<td>Deposition</td>
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<td>50</td>
<td>C$_4$F$_8$=100</td>
<td>2.0</td>
<td>2</td>
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<td></td>
<td>Etching</td>
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4. Conclusions

A new process is developed in order to change SiO$_2$ nanoline fabricated by the edge lithography into resist nanotrench pattern. The new process consists of only the resist coating and the resist etching. Si trench pattern is fabricated by using the resist trench pattern. The fabricated trench width and depth are 35 nm and 260 nm, respectively. The fabricated Si trench is replicated to the PS film by the thermal NIL. The PS nanoline, whose width and height are 28 nm and 360 nm, is successfully fabricated.

Fig. 5 Resist nanotrench after HF acid dipping in “tone change” process (Fig. 2(d))

Fig. 6 Si nanotrench fabricated by “tone change” process (Fig. 2(e))

Fig. 7 PS pattern replicated from Si trench mold shown by Fig. 6.

References