Enabled Scaling Capability with Self-aligned Multiple patterning process

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One of most promising technique for the extension of 193nm immersion lithography must be Self-Aligned Multiple Patterning (SAMP) at the present. We have studied this SAMP in several aspects, which are scaling capability, mitigation of process complexity, pattern fidelity, affordability and so on. On the other hand, Gridded Design Rule (GDR) concept with Single directional layout (1D layout) extended the down-scaling with 193-immersion furthermore and relieve the process variation and process complexity, represented in Optical proximity effect (OPE), by simplification of layout design. In 1D layout fabrication, key process steps might be edge placement control on grating line and controllability of hole-shrink technique for line-cutting.

This paper introduces current demonstration results on pattern transfer fidelity control and hole-shrink technique as combined with unique pattern shape repair approach.

Key words: SAMP, Multiple-patterning, 1D layout, SAOP, LER, Smoothing, Hole shrink

1. Introduction

Optical projection technique has been driving the lithographic scaling with unceasing evolution of wave length (\(\lambda\)) and numerical aperture (NA) historically. Although the delay of EUV (Extreme Ultra Violet) tool for HVM (High Volume Manufacturing) is concerned, down-scaling proceeds unceasingly with the extension approach of 193 immersion. One of most promising technique for extension of 193nm water immersion lithography must be Self-Aligned Multiple Patterning (SAMP) at the present. In 193 immersion technology era continuing optical lithographic scaling, we have been suffering with a lot of process problems like Optical proximity effect (OPE), narrow ED (Exposure -Defocus)-window, Edge placement error (EPE) and so on. 1D layout in GDR (Gridded Design Rule) concept, which was introduced by Tela-Innovations Inc, relieve these problem greatly. This design concept is comprised of one directional periodical line pattern with any length, and fabrication scheme is classified in grating line formation step and line-cutting step. In the discussion of pattern fidelity, EPE within designated tolerance have been inspected and fixed in random layout design. On the other hand, 1D layout can mitigate the pattern verification scheme complexity, and focal points are LER (Line Edge Roughness)/LPR (Line Placement Roughness) on grating-line and line-cutting width accuracy.

In this paper, we would introduce the management technique for pattern fidelity control in 1D layout.

2. Experimental

2.1 Grating line formation

![SAMP Process scheme](image)

Fig. 1 SAMP Process scheme

Resist pattern were prepared utilizing with commercially available 193nm resist on Si-ARC and Spin-on carbon (SoC). Resist was patterned by 193 immersion exposure with 1.30 N.A. and typical TMAH aq. resist developing. The line pattern pitch was shrunk through SAMP. As shown...
in Fig. 1, firstly pattern pitch was divided through SADP flow with SiO₂ spacer film deposited by ALD (Atomic Layer Deposition) on resist pattern, and subsequently spacer pattern was transferred onto SoC layer. Secondary SoC pattern was split through same scheme as above SADP (Self-aligned Double patterning), and then SAQP (Self-aligned Quadruple Patterning) was executed. Final feature size achieved sub-20nm.

2.2 Resist pattern smoothing/LER reduction
For line-edge-roughness (LER) suppression, argon (Ar) plasma treatment to resist pattern was used. In this step, resist pattern was ashed on just pattern surface region slightly and it compacted by polymer scission or side-chain decomposition by UV irradiation from Ar plasma. Enough resist pattern height did not remain to etch the under layer, therefore, Si enclosed film was formed to improve etching durability against etched under layer. These 2 steps treatment were processed in typical RIE (Reactive Ion Etching) processing chamber (Fig. 2) [5].

Fig. 2 Resist smoothing process flow

2.3 Hole shrink process
Several hole-shrink methods, like chemical assist method, tapered etching, conformal deposition, were already known well. Individual controllability of shrink amount on major/minor sections might be required in this study. Therefore, we used organic film deposition method in etching processing module with fluorocarbon type gas as shown in Fig. 3. As deposited film on resist surface and hole bottom was removed by alternated etching process, vertical deposition film remained on just sidewall of hole pattern. Thickness of deposition can be controlled by just processing time and it took around 15 seconds processing time for 20nm thickness.

Fig. 3 Hole-shrink schematic procedure

3. Result and Discussion
3.1 Scaling with SAMP
Theoretically, SAMP technique enables eternal scaling through the repetition of spacer generation process step. As shown in Fig. 4, miniaturized final pattern feature size achieved 5.5nm hp through SAOP (Self-aligned Octuplet Patterning) [6]. As we reported before, organic material was used mainly for core pattern to fabricate spacer pattern such as photo-resist pattern or etched carbon pattern. The combination of carbon core-pattern and SiO₂ spacer was applicable, however, the other spacer material was needed, because sub-10nm geometric pattern easily collapsed and more rigid material was needed.

Fig. 4 demonstration result toward sub-10nm hp

This result represented that SAMP was most credible method to fabricate periodical line pattern.

3.2 LER suppression
In SAMP scheme, atomic layer deposition (ALD) is utilized to form vertical spacer pattern, in order to obtain the conformal deposition property [7]. Therefore, pattern surface roughness was transferred to spacer film precisely. As shown in Table 1, line edge roughness (LER) on core pattern was transferred to next spacer pattern and almost same amount LER progressed on final pattern. In this examination, resist pattern was used for core pattern [8], however, it can’t be used always in several cases.

Various post-litho. smoothing techniques have been investigated over the year, however, in many cases, pattern profile changed and it affected on subsequent etching performance directly as shown in Fig. 5.
For the reason, resist height decreased in smoothing step and enough thickness did not remain enough to etch under layer. In order to maintain the smoothed LER through etching, SiO2 film was placed on smoothed resist pattern. Etching selectivity/durability was improved and reduced LER on resist pattern was kept after etching (shown in Fig. 6).

At the same time, we found out remarkable properties changing in smoothing process. In several previous studies, LER between high and middle frequency region was reduced mainly. On the other hand, LER in low frequency region was also reduced in this study as shown in Fig. 8. The same phenomenon was observed under different illumination conditions and on the different type of resist [9].

3.3 Newly found benefits of smoothing

In this LER reduction/PR(Photo-resist) smoothing study, several remarkable improvements on lithographic performance were found out, thus it would be introduced in Fig. 9-12.

Indicated performance improvements were mask error factor (MEEF), ED-window, local-CD Uniformity, and Line placement roughness (LPR) as much as LER reduction.
The authors assume that Fig. 13 might be sufficient evidence to derive these improvements. CD transfer ratio under nominal etching condition is approximately “1” (red line). On the other hand, the slope of approximate line (blue line) is getting flat and CD distribution after etching was getting narrow under smoothing added condition.

Historically, no etching engineer has never check lithography related performance and lithographer have not taken care them after etching. We believe that lithographic view observation is quite important in any process step.

3.4 Edge Placement control in 1D layout fabrication

The final photoresist pattern seems to suffer edge placement variation or surface roughness, known as line-CD variation, line edge roughness (LER), line placement roughness (LPR) or line pitch walking. The random variation in patterned feature causes the pattern placement error after pitch shrink with Self-aligned Multiple Patterning (SAMP) as shown in Fig. 14.

As mentioned above, “Resist-Smoothing” is quite useful to repair the several variations in core-pattern fabrication.

3.5 Hole shrink technique for line-cutting

In 1D Layout patterning, rectangular shaped holes with several lengths are used. Resolution limit of hole pattern under 193nm-immersion might be about 110nm, therefore, slit (minor section) width on rectangular hole must be narrowed by any hole-shrink technique and shrinking amount on major or minor sections might be controlled individually. In this study, organic film deposition for hole-shrink was selected because it was able to be processed in same chamber for subsequent etching step and vertical side wall angle was relatively obtained as shown in Table 2.

Dimensionally optimized result was shown...
To obtain the narrow slit for line-cutting, we examined controllability of hole-shrink. In most thick deposition case, 15nm slit was attained as shown in Table 3(right picture). More remarkably, shrink amount on minor (Y) section is bigger than major (X) section and X section was relatively constant. It is quite valuable to achieve higher controllability of line-cutting placement under tough tolerance towards 10nm technology node and beyond.

3.6 Smoothing effect on hole pattern
LER on major section of rectangular hole and circle edge roughness (CER) are also serious problem for line-cutting accuracy. We tried to smooth them utilizing same approach as on line pattern [10].

Table 3 Controllability of shrink amount

<table>
<thead>
<tr>
<th>Condition</th>
<th>X (202.1nm)</th>
<th>Y (50.8nm)</th>
<th>X/Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>Condition-1</td>
<td>269.9nm</td>
<td>35.2nm</td>
<td>7.6</td>
</tr>
<tr>
<td>Condition-2</td>
<td>258.7nm</td>
<td>29.4nm</td>
<td>8.8</td>
</tr>
<tr>
<td>Condition-3</td>
<td>241.2nm</td>
<td>19.9nm</td>
<td>15.2</td>
</tr>
</tbody>
</table>

Although Top surface of post-litho. resist pattern became quite rough as shown on tilted picture (left-side) in Table 4, it was smoothed successfully and moreover drastic pattern profile change or thickness-loss was not found.

In this test, we also confirmed the combining effect with subsequent hole shrink process. It can be seen in Fig. 16 that smoothing process contributed to achieve higher accuracy to cut the under grating-line.

3.7 1D layout fabrication
Pattern fidelity has been suffered by edge placement variation historically and it has been corrected by mainly illumination condition and OPC on mask. Especially, edge placement error (EPE) on random layout design was getting serious problem after 65nm technology node. Newly designed single directional (1D) layout dissolved several problems related to EPE.

Focal points for this fidelity control study are listed as following,

①LER/LPR on grating-line
②Pattern registration of hole pattern for line-cutting

As mentioned above, these two bigger problems were mitigated through our proposed robust solutions like resist smoothing for line and hole pattern, pattern transfer control and hole-shrink technique.
The demonstration results, utilizing these our proposed unique techniques on 1D layout fabrication, were introduced in Fig. 18 in conformity with general processing scheme as shown in Fig. 17[11]. The hole pattern for line-cutting, which was placed upper the grating line, was shrunk successfully, and subsequently grating lines were cut on designated part accurately.

It is the evidence that the complementary technique with our proposed processes accomplished square pattern formation without over cutting across next line. It might be understood easily as compared with the result in Fig. 19 (left-picture).

Fig. 18 Process result to fabricate 1D layout

Fig. 19 Pattern feature comparison
a) Fault result induced lithographic condition
b) Successful result with narrow width cutting

4. Conclusion

In this study, we demonstrated 1D (Single directional) layout towards sub-10nm technology node utilizing smart “Complementary Technique” with mainly adopted Self-aligned Multiple Patterning (SAMP).

Finally, fabrication of gate level design on 5nm node was executed successfully.

Key components in Photolithographic scaling have been exposure tool, photo-mask and resist material, and for sustainable scaling, comprehensive approach such like we introduce in this paper would be potential option with consolidation etching, deposition tool and cleaning tool.

References