Opportunities and Challenges in Scaling

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One of the most promising techniques for the extension of 193nm immersion lithography must be Self-Aligned Multiple Patterning (SAMP)[1,2,3] at present. We have studied this SAMP from several aspects, which are scaling capability, mitigation of process complexity, pattern fidelity, affordability and so on. On the other hand, Gridded Design Rule (GDR) concept with single directional layout (1D layout) [4] extended the down-scaling with 193-immersion further and relieved the process variation and process complexity, represented in Optical Proximity Effect (OPE), by simplification of layout design. In 1D layout fabrication, key process steps might be edge placement control for grating lines and controllability of hole-shrink technique for line-cutting.

This paper introduces current demonstration results on pattern transfer fidelity control and hole-shrink technique as combined with an unique pattern shape repair approach.

Key words: SAMP, multiple-patterning, 1D layout, SAOP, LER, smoothing, hole shrink

1. Introduction

Photolithography technology using the optical projection technique continues to progress to support the demand for scaling in semiconductor devices. Extreme ultraviolet (EUV) exposure technology at 13.5 nm is a promising candidate for next-generation exposure technology to replace existing 193 nm water-based immersion lithography, but EUV tool for high volume manufacturing has yet to be perfected. There is consequently much talk about the risks involved in migrating next-generation exposure technology to mass production, but the scaling down of feature sizes in device processes nevertheless continues to advance steadily (Figure 1).

Here, the approach used to achieve further scaling has been adopted multi-patterning technology using existing 193 nm immersion lithography, and this technology has come to be used widely from memory devices to logic devices. Multi-patterning can be broken down into pattern-split techniques, such as litho-etch-litho-etch (LELE) and litho-etch-litho-etch (LELE), and self-aligned techniques, such as self-aligned double patterning (SADP) and self-aligned quadruple patterning (SAQP). These techniques can achieve a level of scaling finer than the 40 nm half-pitch (hp) resolution limit of 193 nm immersion technology. In addition, there is currently a strong move in the industry to make a change in device-circuit design from the random type to single directional (1D) layout with the aim of improving pattern fidelity and process stability, both of which can hold back advances in scaling technologies.

2. Overview of Multi-patterning

Multi-patterning techniques can be broadly divided into pattern-split type and self-aligned type. Typical example of the former type is the litho-etch-litho-etch (LELE) technique, which, as the name implies, aims to achieve narrow pitches by repeating the conventional lithography and etching process. The pattern-split type
has the ability of splitting the pattern as desired even in the case of random patterns like metal lines, but because it involves several cycles of the exposure process, it raises concerns about drops in overlay accuracy. In contrast, the self-aligned type, which was originally referred to as self-aligned double patterning (SADP), has the great advantage of being able to narrow the pitch with only one exposure process thereby eliminating overlay accuracy as a matter of concern (Figure 2). It is applicable to drawing a periodical pattern over a large area as in the cell section of a memory device, and because of this feature, it was adopted early on for use in NAND FLASH memory. The SADP technique can be used to perform 1/2, 1/4, and 1/8 pitch narrowing by repeating the same process, and for this reason, it is now called self-aligned multi-patterning (SAMP).

3. SADP and Extendibility

As shown in Figure 3, the SADP technique first lays down a film with excellent step coverage on top of a core pattern and uses an etch-back process to remove the upper portion of the film above the pattern and the bottom portion of the film, then, using the sidewalls of the core pattern left over by the above process, it forms a secondary spacer pattern to shrink the pitch. This core pattern is also called a mandrel pattern, and the secondarily formed pattern for pitch shrinking is called a spacer pattern. In addition, the space between two spacer patterns (sidewalls) formed on the position of the core pattern is called “core space” while the space between spacer patterns formed on the adjacent space of the core pattern is called “gap space.” These spaces are given different names because the critical dimensions of each fluctuate due to different factors. In this evaluation, we used a resist pattern for the core material and silicon oxide (SiO₂) as spacer material because of its ability to form thin films at low temperatures. We also reduced the scale of processing by omitting an etching process in the formation of the core pattern. This pitch-narrowing technique should, in theory, be able to scale down feature size indefinitely by repeating the same process. As shown in Figure 4, process demonstrations have shown that the SADP technique can be used to achieve up to 1/8 pitch narrowing (SAOP: pitch octupling), which means that scaling as far as the sub-10 nm region is realistically possible [3].

Fig. 4. 5.5 nm hp patterning result with SAOP

At present, only EUV and electron-beam-exposure technologies have the resolution performance to surmount the limiting resolution of 193 nm immersion technology, but their scaling ability has not yet broken into the sub-20 nm region. However, they can be used in combination with SADP to form fine patterns on the order of 10 nm by a relatively simple process (Figures 5 and 6) [5]. Furthermore, we point out here that while line patterns are used in front-end-of-line (FEOL) processing as in gates, trench patterns are used in back-end-of-line (BEOL) processing as in metal line. In the SADP process demonstrations described above, we introduced the formation of line patterns, but as shown in Figure 7, trench reversals can easily be achieved by depositing an additional embedded layer.

Fig. 5. SADP with EUV resist mandrel

Fig. 6. SADP with e-beam resist mandrel

Fig. 7. Negative-tone SADP result
The SADP process makes use of thin-film technology having excellent step coverage and film-thickness uniformity in order to form 2D patterns, so CD uniformity (CDU) in the spacer pattern is relatively stable and line width roughness (LWR) can theoretically approach zero. On the other hand, SADP can also have adverse effects in that inferior features in core material in micro regions can be faithfully passed on as typified by line edge roughness (LER). On inspecting the behavior of LER in each process step of SAQP, it was found that LER distribution on a power spectral density (PSD) chart was faithfully passed on at each process step (Figure 8). Thus, to reduce LER on secondary and tertiary narrow-pitch patterns, it is essential that LER on the core material be reduced to the utmost. The effect of using resist with low LER as core material was examined and it was found that LER could be drastically reduced on a 12 nm hp patterns in the SAQP process (Figure 9) [6]. Although resist patterns generally take the role of a mask for underlayer etching, they do not necessarily have to have etching durability when used as a core material. On developing resist material specifically for use as the core material, we were able to achieve a great reduction in LER by ignoring etching durability. We consider our proven technique that ensures good performance in a secondary pattern by raising the performance of the core material to be more efficient than performing smoothing using a plasma treatment.

4. Applicability to 1D Layout

A major paradigm change has occurred in device pattern design to extend the life of 193 nm immersion technology. Based on the concept of “gridded design rules” born out of the idea of “restricted design rules,” single directional (1D) layout is a type of design that excludes irregular patterns, i.e., consists only of uniform grid-shaped patterns. It is a design promoted by Tela Innovations, Inc. in US mainly for logic devices.

The fabrication process in 1D layout design consists of two main steps: form grid lines of half-pitch and perform line cutting as needed (Figure 10).

In the manufacture of logic devices belonging to the 32 nm-node generation and beyond, grid patterns with a pitch smaller than the limiting resolution (38 nm hp) of 193 nm immersion technology are required, so at this point in time, the approach is to form grid lines by pitch shrinking using SADP. After forming the desired grid pattern, the process moves to the line-cutting step. This step forms holes or block patterns above the grid lines and then uses an etching process to form lines or spaces at any point in the grid pattern. The results of forming 1D design at the metal and gate levels and using cut patterns resolvable by 193 nm-immersion single exposure are shown in Figure 11. These results show that designs of the 16 nm-node generation can be resolved. Additionally, when using electron-beam direct writing tool in the formation of cut patterns, block patterns finer than 20 nm hp can be resolved demonstrating that patterns applicable to the 11 nm-node generation can be resolved (Figure 12) [7].
In the scaling down of 1D design, 28 nm-hp cut patterns are needed to fabricate designs corresponding to the 10 nm-node generation, so divided exposure processing (that is, LELE) must be performed at least twice. A major issue here is whether sufficient overlay accuracy can be attained between lines and cut patterns and between divided cut patterns. To resolve this issue, we proposed the “grid & trim” technique that first forms a hole pattern of equal pitch on the grid lines and then forms an upper-layer pattern that partially obscures the dense hole pattern. This upper-layer mask pattern opens up only that portion of the hole pattern needed for line cutting (Figure 13) [8]. The biggest advantage of this process method is that it dramatically eases the requirements for overlay accuracy compared to using the above LELE technique. Results of a resolution test for 10 nm-node-equivalent gate patterns are shown in Figure 14. Patterns for various critical levels (FIN, gate, contact, and metal) of the 10 nm-node generation have also been successfully formed [9].

5. Pattern Fidelity Control

A major mission of the photolithography area is to improve the resolution fidelity of resist patterns resolved at the wafer level by optical projection technique. Here, the divergence exhibited by the pattern shape when comparing the contours of the resist pattern with the device pattern on the mask is defined as edge placement error (EPE). Source mask optimization (SMO) and computational lithography are now being established as ultimate functions for observing and correcting EPE (Figure 15) [10].

Although the appearance of 1D layout design greatly eased the burden of ensuring fidelity in pattern resolution, further advances in scaling have come to demand higher levels of process accuracy. In this section, we point out key issues and their solutions in achieving pattern fidelity in 1D design.
CDU can easily break down in the case of $S_2$ and $S_4$ among the different types of space CDs, and it is also heavily dependent on the CD values of the initial pattern. Although pattern pitch on the mask is invariable, the line-and-space ratio is not, and this ratio is directly linked to variation in $S_2$ and $S_4$. It can therefore be seen that CD management is vital in the lithography process [11].

Next, we describe how a failure in the line-cut process can affect pattern accuracy using a representative example (Figure 17). Accuracy in line cutting can be improved in several ways. These include achieving good resolution performance in separating hole patterns, ensuring uniformity in the hole-minor-axis CD corresponding to the cut width, and ensuring a wide margin for the hole-major-axis CD so that holes do not protrude into neighboring patterns. In addition, hole-shrink technology is essential when the cut width is required to be below the limiting resolution of 193 nm immersion technology. In this regard, LER on the hole minor-axis directly affects cutting accuracy, so it must be reduced before the hole-shrink process. The effect of LER reduction processing on a hole pattern is shown in Figure 18. The overlay accuracy of exposure equipment can also contribute greatly to improving overall cutting accuracy, but some sort of measure is needed to improve the accuracy of detecting overlay marks [12].

6. Applicability to Hole Patterns

As described above, SADP is a robust technique for doubling the pitch of line patterns, but it can also be applied to hole patterns in the following way. First, we deposit spacer material on an equal-pitch pillar pattern so that the thickness of the deposited film reaches a point at which a “dimple” is generated at the center of four adjacent pillars. Then, by etching back the upper portion of the spacer material to the point that the top of the pillar pattern appears, we transform the pit and the pillar-pattern section into a hole pattern with a narrow pitch $1/\sqrt{2}$ that of the original pitch (Figure 19) [13].

In addition to this technique, Cross-SADP is considered to be a reliable candidate technology for achieving even finer hole patterns beyond 20 nm hp. Cross-SADP first forms a spacer pattern by SADP and then performs SADP processing again on the upper layer of that spacer pattern but in an orthogonal direction thereby forming a grid pattern. It then uses this pattern as an etching mask to perform underlayer processing. In this way, Cross-SADP can resolve a hole pattern having a narrow pitch which is 1/2 pitch of the initial (core) pattern (Figure 20) [14].
7. Additional Technologies

7-1 LER Suppression

As an index of resist patterning performance, LER plays a major role in device scaling, and many LER-reduction processes have come to be proposed. In this regard, a smoothing effect can often appear in medium- to high-frequency regions, but a reduction effect has not been observed for LER that has significant fluctuation in the 1 μm⁻¹-to-several-100 nm⁻¹ low-frequency region. However, the smoothing process introduced in this paper revealed a smoothing effect even in the low-frequency domain (Figure 21). This smoothing process, moreover, has the effect of leveling off the surface of the resist pattern by irradiating the pattern with Argon plasma.

Fig. 21 LER reduction in low frequency region

This phenomenon of reducing LER uniformly from high- to low-frequency regions appears even when changing aerial contrast at the time of resist resolution. On comparing a pattern resolved under high-, middle-, and low-optical-contrast conditions, it can be seen that LER changes uniformly across all frequency regions (Figure 22). Conversely, we can say that this smoothing process can be expected to give the same effect as improvement of image contrast. Comparing the mask error enhancement factor (MEEF) before and after smoothing in an actual experiment, we found a large improvement effect (Figure 23). We were also able to show that this smoothing process could contribute to improvements in on-chip CD variation and line placement roughness (LPR) (Figures 24 and 25). This advantage of being able to greatly reduce key factors that affect pattern fidelity in SAMP simply through a smoothing process should be seen as a noteworthy effect in the formation of 1D layouts [15].

Fig. 22. LER trend with aerial contrast

Fig. 23. MEEF improvement by PR smoothing

Fig. 24. On-chip CD variation improvement

Fig. 25. LPR (Line placement roughness) trend

7-2 ALD: Atomic Layer Deposition

ALD (Atomic layer deposition) is a film-formation technique that deposits one molecular layer at a time. In contrast to standard film-formation techniques that are dependent on material supply control and reaction control, ALD has excellent step-coverage characteristics and film-thickness uniformity (Figure 26). It is said that ALD is the most optimal technique for forming film with spacer material in each process cycle of SAMP. In addition, ALD can be used to form films at very low temperatures below the
glass-transition point \((T_g)\) of resist material thereby preventing pattern deformation from heat. This feature can be exploited to achieve a narrow-pitch pattern even for irregular patterns like those shown in Figure 27 while faithfully maintaining pattern shape. The ALD technique also features diversity in film selection as it can be used to form a variety of films from \(\text{SiO}_2\) to metallic films such as \(\text{TiO}\) and \(\text{AlO}\). In short, ALD enables film selection from a wide range of options in accordance with the etching environment.

The use of ALD is not limited to the formation of spacer patterns—it is also useful in hole shrinking for pattern cutting in the case of a 1D layout. Taking advantage of its excellent step-coverage characteristics, ALD can be used to form film of equal thickness along both the major axis and minor axis of an elliptical hole so that hole dimensions can be shrunk while maintaining the initial shape of the hole pattern. The chemical assist method, in contrast, does not achieve a linear shrink ratio along both the major and minor axes and consequently results in a defect in which shrinkage occurs only along the major axis. Furthermore, on comparing behavior in the vertical direction between ALD and chemical assist, a similar phenomenon occurs when using chemical assist in that the sidewall angle (SWA) of a hole pattern changes when performing hole shrinking resulting in poor resolution at the time of underlayer transcription. When using ALD, however, only CD shrinkage is performed while sufficiently maintaining SWA in the vertical direction thereby minimizing this problem (Figure 28). In the above ways, ALD is becoming essential in a wide range of SAMP applications.

![Fig. 27. Pitch-shrink of random shape pattern](image1)

![Fig. 28. Liner property of shrink amount of ALD](image2)

### 8. Conclusion

Scaling in the manufacturing of semiconductor devices has come to be supported by advances in photolithography technology. Looking to the future, we can expect even more advances in photolithography, but at present, multi-patterning using 193 nm immersion lithography is finding widespread use as an alternative technology that can contribute greatly to even higher levels of integration in semiconductor devices in combination with 1D layout. However, given increasingly complicated processes and sharp jumps in cost impact with this approach, the ideal solution would be one based on the optical reduction projection method as in the past.

We anticipate the appearance of EUV technology as a next-generation lithography technology that will achieve a complementary convergence with etching and film-growing techniques developed with multi-patterning technology.

Key components in photolithographic scaling have been exposure tool, photo-mask and resist material, and for sustainable scaling, comprehensive approach such like we introduce in this paper would be potential option with consolidation etching, deposition tool and cleaning tool.

### References

6. Hidetomi Yaegashi, Kenichi Oyama, Arisa Har, Sakurako Natori, Shohei Yamauchi, “Overview: Continuous evolution on
double-patterning process”, *Proc. SPIE.*, 8325 (2012) 83250B.