Hexagonal Hole Array Patterning for Memory Applications

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This paper describes progress in the development of the recently proposed CHIPS flow for hexagonal hole array patterning. The CHIPS flow provides a versatile and low-cost route for patterning of dense hexagonal hole arrays which are specifically relevant for DRAM applications. In this paper, it is demonstrated that the required pre-pattern may be printed using single exposure 193nm immersion lithography. Furthermore, strategies for definition of the array edge are proposed and results on transferring the hexagonal hole array pattern into an inorganic underlayer are described.

Keywords: directed self-assembly, chemo-epitaxy, cylindrical phase block copolymer, DRAM patterning

1. Introduction

DRAM devices have been scaling in dimension according to Moore’s law along with other IC products such as micro-processor units (MPU) and flash memory. One of the most critical layers in a DRAM device is the storage array. Typically, the pattern in this layer consists of a dense array of hexagonal pillars that each act as a capacitor in which bits are stored by capacitive charge. The density of the pillars determines the information density that can be stored on a unit area of the DRAM chip and is therefore a critical parameter for the performance of the device. Currently, the typical method for patterning the storage node level is by cross-bar patterning of line/space arrays. The dense line/space arrays that are required for the current DRAM technology nodes are typically generated though sidewall spacer patterning techniques such as self-aligned double patterning (SADP) or self-aligned quadruple patterning (SAQP) [1]. This approach has a high contribution to the total cost in the DRAM manufacturing process, because of the multiple deposition and etch steps that are required for the sidewall spacer patterning and because of the two lithography steps that are needed to print the two cross-bar arrays that ultimately result in the desired cylinder pattern.

Directed self-assembly (DSA) of cylindrical phase block copolymer (BCP) materials provides a very attractive alternative route for more efficient patterning of hexagonal arrays. Cylindrical phase BCPs by nature form a densest packing of cylinders of the minority block, resulting in a hexagonal array. On an appropriate substrate the cylinders orient vertically while the hexagonal packing is maintained (Figure 1).

Figure 1. Top-down SEM images of unaligned cylindrical phase BCP materials with two different molecular weights on a near-neutral substrate.

If a pre-pattern with a pitch commensurate to the BCP and appropriate surface energy properties is used, the cylinders of the BCP align spontaneously in the hexagonal packing while the
positioning of the array may be controlled through the pre-pattern. This approach has originally been demonstrated using e-beam for pre-patterning on wafer coupons [2]. In earlier work, we have been able to integrate this approach on 300mm wafer substrates, using EUV lithography for pre-patterning, in a flow that was termed the HONEYCOMB flow [3,4]. We found that frequency multiplication was difficult to achieve in the HONEYCOMB flow when using 193 nm immersion lithography for pre-patterns due to the limited CD control that is available for the pre-pattern spots in the desired CD range. For this purpose the CHIPS flow (Figure 2) was recently proposed and a proof of concept of this approach has been demonstrated [5]. In this flow, the pre-pattern structures are defined as pillars (in contrast to the previous flows where they were defined as holes) which allows better CD control through the subsequent trim etch step. In doing this, the CHIPS flow follows a similar strategy as the LiNe flow [6-10] does for line/space patterning. The frequency multiplication that is enabled by the CHIPS flow, allows the use of 193nm immersion lithography for pre-pattern generation.

In this paper, continued progress on development for the CHIPS flow is reported. For early demonstrations of the flow, double line exposure was used to define the pillar array pre-pattern. Here, we will demonstrate that the flow also works with a single exposure for pre-pattern generation. Second, strategies for array edge definition will be discussed. Finally, progress on transferring the pattern into an underlying stack will be demonstrated.

2. Experimental Details

All exposures were executed on an ASML NXT:1950i 193 nm immersion scanner at 1.35 NA using dipole illumination. The DSA specific steps were processed off-line on a Tokyo Electron CLEAN TRACK ACT™ 12. Plasma etch processing steps for photoresist and PMMA mat trim in the chemo-epitaxy flow were carried out with an N₂/O₂ plasma on the TEL Tactras™ platform at imec. Photoresist was stripped after trim etch by rinsing with BASF Orgasolv photoresist stripper.

For the PS-b-PMMA BCP, natural pitch and optimal processing conditions for film thickness and anneal conditions were determined by independent self-assembly experiments on un-
patterned neutral surfaces. A film thickness of 40 nm and an anneal at 250°C for 5 minutes under nitrogen atmosphere was established as the optimum processing conditions for the BCP AZEMBLY™ PME-825 resulting in a natural half pitch of ~22.5nm. The anneal drives out remaining solvent after spin coating and promotes micro-phase separation and self-assembly of the block copolymer molecules.

We use a cross-linkable PMMA mat (X-PMMA) as the under-layer in our chemo-epitaxy process. This X-PMMA film was spin coated 8 nm thick and annealed at 250°C for 3 minutes under nitrogen atmosphere to drive out the solvent and activate the cross-linker. Additionally, we use a PS-PMMA random co-polymer with majority PS content and a terminal functional group that grafts to the substrate on thermal anneal as a backfill brush. This material was coated at > 20 nm film thickness and annealed at 220°C for 3 minutes under nitrogen atmosphere for grafting. Finally, ungrafted brush material was removed with organic solvent rinse. Final grafted brush thickness was measured at 6 to 8 nm.

For PMMA removal from assembled BCP films to open the contact holes, a wet development technique was used in the CLEAN TRACK ACT™ 12. DUV exposure was followed by organic solvent development.

SEM imaging of photoresist patterns and BCP patterns for critical dimension (CD) and local CD uniformity (LCDU) measurement was performed using a Hitachi CG-5000 top-down CD-SEM. Defect analysis was performed using manual analysis of SEM images that were systematically collected from a patterned array area using a KLA-Tencor eDR-7100 defect review SEM.

3. Results and Discussion

3.1 Single-exposure pre-patterning

In our initial demonstration of the CHIPS flow [5] double exposure was used to pattern hexagonal or rectangular arrays of pillars. While this method of implementing the CHIPS flow is expected to provide a significant cost reduction through simplification of the patterning process compared to double sidewall patterning, an even more significant cost reduction will come when the pre-pattern can be fabricated through a single exposure. The pre-pattern needs to be commensurate to our target final half pitch of 22.5nm. This means that for the hexagonal pre-pattern with 4X density multiplication, pillar structures are needed where the center-to-center distance for a pillar to its nearest neighbor equals 90nm (45nm half pitch). This is on the very edge of what can be expected to print using 193nm immersion lithography. Source-mask optimization (SMO) was performed to print these type of pre-pattern structures with highest possible fidelity (Figure 3). Nevertheless the simulated normalized image log-slope (NILS) for printing this type of structure on our NXT:1950i...
after SMO does not exceed 1.1. Typically at NILS values of 1 and lower patterns will not be resolved properly, so the hexagonal 45nm pitch pillar array is uncomfortably close to this edge. The simulations also show that at slightly more relaxed pitch the printing quality will be expected to increase rapidly and a decent process window for pillar printing may be expected. However, since we are targeting a 22.5nm final half pitch this is not an option in our case.

The NXT:1950i in the configuration that is available at imec uses XY-polarization for the simulations that are discussed in Figure 3. However, simulations also indicate that specifically for the hexagonal pillar array structures, TE polarization is expected to provide a ~35% increase in NILS (from 1.1 to 1.5). This polarization mode will soon be available at imec and will be used for future work on single exposure pre-pattern formation for CHIPS.

Results for double and single exposure pre-patterning for 4X density multiplication DSA are compared in Figure 4. Hexagonal (top) and rectangular (middle) pre-patterns are formed by double exposure. In the case of the hexagonal pre-pattern this typically results in elongated pillars for double exposure. For the single exposure hexagonal pre-pattern (bottom) the pillars are round, but significant scumming is observed even at best dose. The exposure latitude for pre-pattern formation is very small in this case (results not shown). Nevertheless, from all 3 pre-patterning options very similar pattern quality may be obtained after the CHIPS DSA process. In all cases a single grain structure with high open hole rate is achieved and the final patterns are indistinguishable from each other.

Preliminary defect results have been obtained in order to investigate the primary defect modes. Local pattern misalignment (resulting in grain boundaries) and closed holes were found to be the predominant defect modes (Figure 5). For both defect modes, the density was found to be significantly higher for the single exposure pre-pattern compared to the double exposure. This can easily be understood from the better pattern fidelity that is seen in the case of the double exposure scheme for pre-pattern generation. For that reason, the single exposure defectivity is expected to improve once it is generated with TE polarized illumination. In general, improvements in the chemical pre-pattern are expected to improve the defect performance of the CHIPS flow.

Figure 4. Top-down SEM images for double exposure hexagonal (top) and rectangular (middle) as well as single exposure hexagonal (bottom) hole array pre-patterns (left). Images on the right give the corresponding post CHIPS DSA structures at 22.5nm half pitch (4X density multiplication).

Figure 5. Sample top-down SEM images for the predominant defect modes as observed in the CHIPS flow; grain boundaries (left) and single closed holes (right).
3.2 Array edge control

For a DRAM device, logic structures are present in the periphery outside the memory storage array. Typically, these structures are patterned separately, but a well-defined edge of the memory array is required. In principle, this may be done through a separate cut-exposure, but DSA may provide a more elegant (and lower cost) solution through flipping of the BCP orientation at the edge. Schematically, this is depicted in Figure 6. If a strongly preferential wetting layer for one of the blocks is present immediately outside the pre-pattern array, the BCP will flip orientation and form cylinders parallel to the substrate. In the case of the CHIPS flow, an unpatterned X-PMMA surface immediately outside the patterned array area will act as a preferential wetting layer for the PMMA block of the BCP. A similar approach has been demonstrated for lamellar phase BCP systems, where the flipping of orientation has been shown to be a function of both dimension and guide strength of the preferentially wetting material [11, 12]. In the case of cylinders, these features will be unguided on the preferentially wetting substrate and initially form random patterns (fingerprints). As long as these patterns are not transferred into the underlying substrate when the memory array is patterned, this approach could provide a solution for defining the array edge.

Orientation control of the 45nm pitch BCP material was first verified on unpatterned substrates (Figure 7). The results confirm that the X-PMMA substrate is preferentially wetting resulting in fingerprint patterns that are formed by the parallel cylinders (left). In contrast, an appropriate neutral layer results in perpendicularly oriented cylinders and a random hole pattern (right).

In order to verify whether this approach also works at an array edge, an appropriate mask structure is needed. A test structure that is used for such evaluation is depicted in Figure 8 (top). A dark border is present immediately outside the patterned array area such that a large area of resist is present there, which protects the X-PMMA during the subsequent etch step. It should be noted that the test structure requires the single exposure scheme for pre-pattern formation as discussed in the previous section. The final result after DSA (Figure 8, bottom right) demonstrates the proof of concept of using BCP orientation control for edge definition. Within the array a single grain of vertically aligned cylinders is observed resulting in hole patterns. Outside the array an abrupt transition to a fingerprint pattern is observed as expected from parallel oriented cylinders. The degree of perfection however clearly needs improvement, since the transition is not yet restricted to a single row. Nevertheless, the pattern fidelity is remarkable given the rather poor definition of the edge after the lithography step (Figure 8, bottom left). At this stage no optical proximity correction (OPC) has been done on the test pattern. Given the aggressive pattern dimensions, it is not surprising that the proximity effects near the edge are significant and result in rather poor edge definition. It is expected that a
better definition of the edge after lithography will also result in improvement of the edge definition post-DSA.

Figure 8. Top: Test structure for investigating BCP orientation control near the pillar array edge. Bottom: Top-down SEM images of post-lithography pre-pattern of the edge (left) and post-DSA BCP pattern (right).

3.3 Pattern transfer
In contrast to lamellar phase BCP systems, cylindrical phase materials do form structures (fingerprints) when they are oriented parallel to the substrate. In order to apply the array edge definition approach as outlined in the previous section it needs to be verified whether these fingerprint patterns transfer into the underlying substrate during dry etch or not. An initial test was performed using an unoptimized etch recipe for transfer of the BCP pattern into silicon oxide (Figure 9).

Figure 9. Top-down SEM images of the array edge after the DSA process (left) and after dry etch into silicon oxide (right).

The uniformity of the pattern inside the array evidently needs further improvement, but that is not the focus of this initial study. More importantly, the results demonstrate that the initial fingerprint pattern is not transferred in the dry etch process, which is a requirement for considering this approach for implementation. Infrequent opening of individual holes is observed in the array edge area. Further process optimization in either dry etch and/or the DSA process is expected to resolve this.

4. Conclusions
In this paper, recent process improvements on the CHIPS flow for printing regular, dense hexagonal hole arrays are reported. Feasibility of printing the pre-pattern through a single exposure lithography step has been demonstrated. As part of this development a source-mask optimization has been performed to maximize the printing performance of the pre-pattern structures. Further improvement of this single exposure scheme is expected with optimized polarization control. Next, an approach is introduced for patterning the hexagonal array edge through orientation control of the block copolymer. A proof of concept demonstration has been successful and further improvement is expected once mask structures with appropriate optical proximity correction are available. Finally, it has been demonstrated that under appropriate etch conditions the horizontally oriented cylinders do not transfer into the underlying substrate. This allows usage of BCP orientation control for edge definition in a patterning process for hexagonal hole arrays.

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References


